

Abstract

Reset and watchdog system for a microprocessor, and appliance comprising such a microprocessor and such a system

A system comprising a microprocessor (2) and a reset and watchdog circuit (4), the microprocessor (2) generating a first pulse train (P1) to indicate a correct operation of the microprocessor (2) and the reset and watchdog circuit (4) generating a reset signal (RST) in response to an irregularity in the occurrence of the first pulse train
5 (P1).

The first pulse train (P1) is a substantially synchronous software copy of a second pulse train (P2) which is to be received by the microprocessor (2) and which is preferably a limited a.c. mains voltage signal (M), which copy is generated by an appropriate programming of the microprocessor (2). The reset and watchdog circuit (4)
10 receives the first pulse train (P1) and the second pulse train (P2) and supplies the reset signal (RST) in response to a disturbed synchronism between the occurrence of the first pulse train (P1) and the second pulse train (P2).

(Figure 1)