

LOW RESISTANCE LINER

CROSS REFERENCE TO RELATED PATENTS AND APPLICATIONS

[0001] This application claims priority to and the benefit of the filing date of U.S. Non-Provisional Patent Application No. 18/508,387, filed November 14, 2023, which application
5 is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present invention relates generally to methods of processing a substrate, and, in particular embodiments, to low resistance liner.

BACKGROUND

10 [0003] Generally, a semiconductor device, such as an integrated circuit (IC) is fabricated by sequentially depositing and patterning layers of dielectric, conductive, and semiconductor materials over a substrate to form a network of electronic components and interconnect elements (e.g., transistors, resistors, capacitors, metal lines, contacts, and vias) integrated in a monolithic structure. Process flows used to form the constituent structures of semiconductor
15 devices often involve depositing and removing a variety of materials while a pattern of several materials may be exposed in a surface of the working substrate.

[0004] The minimum dimension of features in a patterned layer is shrunk periodically to roughly double the component density at each successive technology node, thereby reducing the cost per function. Innovations in patterning, such as immersion deep ultraviolet (i-DUV)
20 lithography, multiple patterning, and 13.5 nm wavelength extreme ultraviolet (EUV) optical systems have brought some critical dimensions down close to ten nanometers. As the miniaturization progresses further, new problems are emerging in copper (Cu) wiring. That is, the wiring width used in the device has become even small than the mean free path of electrons in a Cu material, causing an increase in resistance value due to scattering. Therefore, new

wiring materials for metal interconnects with superior material properties and their fabrication techniques may be desired at increasingly smaller scales.

SUMMARY

[0005] In accordance with an embodiment of the present invention, a method of
5 processing a substrate includes forming an amorphous silicon (a-Si) liner over the substrate,
where the substrate includes a dielectric layer and a conductive layer, and the a-Si liner
covers a surface of the dielectric layer and a surface of the conductive layer. The method
includes converting the a-Si liner into a silicon-containing layer including a metal; and
depositing the metal over the silicon-containing layer using the silicon-containing layer as a
10 seed layer for the depositing, where the metal deposited over the silicon-containing layer and
the conductive layer are electrically connected.

[0006] In accordance with an embodiment of the present invention, a method of
processing a substrate includes forming an amorphous silicon (a-Si) liner over a surface of
the substrate, where the surface includes a conductive line and a dielectric layer, and the
15 substrate includes a pattern of conductive lines formed within the dielectric layer. The
method includes depositing ruthenium (Ru) over the a-Si liner using a vapor deposition
process, where a portion of the a-Si liner reacts with a portion of Ru to form RuSi at an initial
stage of the vapor deposition process, and where Ru is deposited over RuSi.

[0007] In accordance with an embodiment of the present invention, a method of
20 processing a substrate includes forming a recess in a dielectric layer of the substrate; filling
the recess with ruthenium (Ru) using a chemical vapor deposition (CVD) process; and
planarizing a surface of the substrate, where the surface after the planarizing includes the
dielectric layer and Ru. The method includes forming an amorphous silicon (a-Si) liner over

the surface; and depositing Ru over the a-Si liner using a physical vapor deposition (PVD) process.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] Figures 1A-1E illustrate cross sectional views of an example substrate during an example process of semiconductor fabrication comprising metal deposition with a silicon liner at various stages in accordance with various embodiments, wherein Figure 1A illustrates an incoming substrate, Figure 1B illustrates the substrate after a silicon liner formation, Figure 1C illustrates the substrate after a metal deposition, Figure 1D illustrates the substrate after patterning the metal, and Figure 1E illustrates the substrate after dielectric-on-dielectric (DoD) deposition;

[0010] Figure 2 illustrates film resistivity of conventional liner materials (TiN and TaN) and ruthenium silicide (RuSi);

[0011] Figure 3 illustrates film resistivity of Ru/TiN layer stack and Ru/RuSi layer stack;

[0012] Figures 4A-4C illustrate process flow charts of methods of metal deposition with a silicon liner in accordance with various embodiments, wherein Figure 4A illustrates an embodiment process flow, Figure 4B illustrates an alternate embodiment process flow, and Figure 4C illustrate another alternate embodiment process flow.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0013] This application relates to a method of processing a substrate, more particularly to low resistance liner. Techniques herein may be applied to and useful in fabricating metal interconnects in semiconductor devices at small scale. As device feature size continues to

scale down, minimizing the electrical resistance has become a significant challenge especially for tight metal pitch. For example, the interconnect-RC delay of conventional copper (Cu) lines and tungsten (W) contacts may be limiting the speed of digital circuits. New materials are being introduced at the 10 nm nodes and below to replace dense Cu lines and W contacts.

5 Ruthenium (Ru) metal is a leading candidate for replacing copper and tungsten in these and other applications. However, there are unique technical challenges for the application of Ru metal in metal interconnects. One of them is the vertical resistance of a Ru/liner stack. In a conventional fabrication process of metal interconnect using Ru, an adhesion layer such as titanium nitride (TiN) and tantalum nitride (TaN) may be used to improve Ru adhesion to the
10 surface. The inherent resistivity of the liner material and the interface between Ru and the liner may often result in increased vertical electrical resistance. It is, therefore, desirable to have a new method of forming a Ru/liner stack with low electrical resistance.

[0014] Embodiments of the present application disclose methods of forming a metal/liner stack with low resistance. In various embodiments, the methods may comprise forming a
15 silicon liner (e.g., amorphous silicon) and vapor depositing a metal (e.g., Ru) over the silicon liner. During the vapor deposition or a separate annealing treatment, the silicon liner may react to form a metal silicide (e.g., RuSi) layer which may be a final form of the liner underlying the deposited metal. The inherent resistivity of the metal silicide can be at least an order of magnitude lower than conventional liner materials, making an excellent alternative
20 liner material for metal deposition. The inventors of this application experimentally demonstrated that the metal deposition over the silicon liner is enabled with sufficient adhesion. The methods of metal deposition can therefore be advantageously applied in metal interconnect fabrication processes and may be used to form a metal via or metal line.

[0015] In the following, Figures 1A-1E illustrate steps of a process of the metal
25 deposition with a silicon liner in accordance with various embodiments. Example film

resistivity data obtained for a RuSi liner and a Ru/RuSi stack are illustrated in Figures 2-3.

Several embodiment process flows of metal deposition are described referring to Figures 4A-

4C. All Figures in the disclosure, including the aspect ratios of features, are not to scale and for illustration purposes only. Although various embodiments of this disclosure primarily

5 describe metal deposition particularly using ruthenium (Ru), the methods of deposition may be applied to deposit any appropriate metals, alloys, or other conductive materials as long as the silicon liner may be formed prior to the metal deposition. Accordingly, the term “metal” or “metal deposition” in this disclosure is not limited to a pure metal but used to include any conductive material (e.g., alloy and compounds) comprising at least one metal element.

10 Further, any list that presents possible compositions, conditions, or process variations includes any reasonable combination thereof, and thus the term “or” used in the list does not indicate any exclusive selection of a particular composition, condition, or process variation.

[0016] Figures 1A-1E illustrate cross sectional views of an example substrate 100 during an example process of semiconductor fabrication comprising metal deposition with a silicon
15 liner at various stages in accordance with various embodiments.

[0017] In Figure 1A, the substrate 100 may be a part of, or include, a semiconductor device, and may have undergone a number of steps of processing following, for example, a conventional process. The substrate 100 accordingly may comprise layers of semiconductors useful in various microelectronics. For example, the semiconductor structure may comprise
20 the substrate 100 in which various device regions are formed.

[0018] In one or more embodiments, the substrate 100 may be a silicon wafer, or a silicon-on-insulator (SOI) wafer. In certain embodiments, the substrate 100 may comprise a silicon germanium wafer, silicon carbide wafer, gallium arsenide wafer, gallium nitride wafer and other compound semiconductors. In other embodiments, the substrate 100 comprises

heterogeneous layers such as silicon germanium on silicon, gallium nitride on silicon, silicon carbon on silicon, as well layers of silicon on a silicon or SOI substrate. In various embodiments, the substrate 100 is patterned or embedded in other components of the semiconductor device.

5 [0019] As illustrated in Figure 1A, the substrate 100 may further comprise a first dielectric layer 110, interlayer dielectric (ILD) 120, a first conductive fill 130, and a second conductive fill 140. In various embodiments, the structure illustrated in Figure 1A may be a part of a metal interconnect at an intermediate stage of a back-end-of-line (BEOL) process. Accordingly, in certain embodiments, the first conductive fill 130 may be a metal line (e.g.,
10 M1 layer) and the second conductive fill 140 may be a via, where the ILD 120 is formed for via formation. In certain embodiments, the first dielectric layer 110, the ILD 120, or both may comprise silicon oxide or a low-k dielectric such as fluorosilicate glass (FSG) or carbon-doped silicon oxide (CDO). In one or more embodiments, the first conductive fill 130, the second conductive fill 140, or both may comprise aluminum (Al), copper (Cu), tungsten (W),
15 ruthenium (Ru), or osmium (Os). In one or more embodiments, the first conductive fill 130, the second conductive fill 140, or both may comprise molybdenum (Mo), niobium (Nb), nickel (Ni), or cobalt (Co).

[0020] In various embodiments, a series of materials deposition and patterning with photolithography and subsequent pattern transfers may be performed using conventional
20 methods to form the structure of Figure 1A. For example, a first recess (i.e., trench) may be formed in the first dielectric layer 110, the formed recess feature may be filled with the first conductive fill 130, the ILD 120 may be deposited over the substrate 100, a second recess (i.e., via) may be formed in the ILD 120, and the second recess may be filled with the second conductive fill 140.

[0021] In certain embodiments, the second conductive fill 140 may be deposited over the substrate using a vapor deposition technique such as atomic layer deposition (ALD), physical vapor deposition (PVD), chemical vapor deposition (CVD), or plasma-enhanced CVD (PECVD), followed by planarization to flatten the top surface. In one or more embodiments, chemical mechanical planarization (CMP) may be used for the planarization. In various
5 embodiments, the first conductive fill 130 may comprise a metal line and it may have a critical dimension (CD) less than 50 nm, and in certain embodiments, less than 20 nm. In one or more embodiments. Accordingly, in certain embodiments, the second conductive fill 140 may comprise a metal via and it may have a CD less than 50 nm, and in one embodiment,
10 less than 20 nm. Further, the metal via made of the second conductive fill 140 may have an aspect ratio (AR) between 2:1 and 100:1 in one embodiment.

[0022] In one or more embodiments, the second conductive fill 140 may comprise ruthenium (Ru), and chemical vapor deposition (CVD) may be used for its deposition. For example, a Ru precursor, ruthenium carbonyl ($\text{Ru}_3(\text{CO})_{12}$) may be flowed into the deposition
15 chamber containing the substrate 100, where ($\text{Ru}_3(\text{CO})_{12}$) may be thermally decomposed on the surface and a high-purity thin Ru film may be formed within the recess 125. In one or more embodiments, the process conditions for Ru deposition may be as follows: the pressure within the deposition chamber in a range of 0.1 mTorr to 1 Torr, preferably in a range of 10 mTorr to 500 mTorr, and the substrate temperature in a range of 120°C to 300°C, preferably
20 in a range of 130°C to 250°C. In various embodiments, the process temperature may be kept below 400°C to be within a typical thermal budget in back-end-of-line (BEOL) processes.

[0023] In other embodiments, the Ru deposition may be performed using a Ru pentadienyl compound such as (cyclopentadienyl) (2,4-dimethylpentadienyl) ruthenium, bis(cyclopentadienyl) (2,4-methylpentadienyl) ruthenium, (2,4-dimethylpentadienyl)
25 (ethylcyclopentadienyl) ruthenium, or bis (2,4-methylpentadienyl) (ethylcyclopentadienyl)

ruthenium. When using these precursors, the CVD may also use a reducing gas in addition to the Ru precursor.

[0024] Further, as illustrated in Figure 1A, a liner 135 may be inserted at interfaces between the dielectric materials (e.g., the first dielectric layer 110 and ILD 120) and the
5 conductive materials (e.g., the first and second conductive fills 130 and 140). The liner 135 may be a barrier layer to prevent diffusion of atoms across the interfaces, an adhesion layer to improve adhesion of fill material over the surface, or a combination thereof. In certain embodiments, the liner 135 may comprise titanium, titanium nitride, tantalum, tantalum nitride, tungsten, molybdenum, cobalt, or a combination thereof. In certain embodiments, the
10 thickness of the liner 135 may be in a range of 0.1 nm to 10 nm. The liner 135 may be formed by, for example, ALD, PVD, CVD, or PECVD.

[0025] Continuing the process to fabricating the metal interconnect, the next step may be another metal deposition (e.g., Ru) over the substrate to form a next metal line. In conventional methods, another liner such as titanium nitride or tantalum nitride, similar to the
15 liner 135 may be used for better metal adhesion. In various embodiments, however, the methods of metal deposition may use a silicon liner instead of conventional metal nitride materials as further described below (Figures 1B-1E).

[0026] Figure 1B illustrates a cross sectional view of the substrate 100 after a silicon liner formation.

20 [0027] In various embodiments, a silicon liner 145 comprising silicon (Si) may be deposited over the top surface of the substrate 100 (e.g., exposed surfaces of the ILD 120 and the second conductive fill 140) using a vapor deposition technique such as ALD, PVD, CVD, or PECVD. In various embodiments, the process temperature may be kept below 400°C to be within a typical thermal budget in back-end-of-line (BEOL) processes. In certain

embodiments, the silicon liner 145 may comprise amorphous silicon (a-Si). In certain embodiments, the silicon liner 145 may have a thickness between 0.1 nm to 10 nm.

[0028] Although Figures 1A-1E illustrates embodiments with the silicon liner 145 formed over a flat surface, in other embodiments, it may be conformally formed over a patterned, non-flat surface. In various embodiments, the silicon liner 145 may advantageously improve the adhesion of a conductive material deposited in a subsequent deposition step (Figure 1C).

[0029] In certain embodiments, a pre treatment step such a surface cleaning process may be performed prior to the next step described below.

[0030] Figure 1C illustrates a cross sectional view of the substrate 100 after a metal deposition.

[0031] After the silicon liner formation, the metal deposition step may be performed. In various embodiments, the silicon liner formation of Fig. 1B and the metal deposition of Fig. 1C may be performed in the same process chamber. In various embodiments, this deposition step may not be limited to a pure metal, and any alloys or conductive materials may be used. An electrically conductive material (referred to as conductive material 160 in this disclosure) may be deposited using a vapor deposition process to over the substrate 100, covering the silicon liner 145 formed in Figure 1B. In various embodiments, the conductive material 160 may comprise ruthenium (Ru). In certain embodiments, the Ru deposition may be performed by a PVD process such as sputtering deposition. In certain embodiments, the Ru deposition may also be performed by a CVD process including plasma enhanced CVD provided the underlying silicon liner 145 and the conductive material 160 are deposited in the same chamber without exposure to atmosphere. In various embodiments, the metal deposition process may be performed at a temperature between 200°C and 350°C. In one embodiment

with the sputtering deposition of Ru, a Ru target may be bombarded with energized argon ions (Ar^+) to deposit a Ru film over the substrate 100.

[0032] In alternate embodiments, the conductive material 160 may comprise aluminum (Al), copper (Cu), cobalt (Co), tungsten (W), osmium (Os), molybdenum (Mo), niobium (Nb), or nickel (Ni).

[0033] In various embodiments, silicon (e.g., a-Si) of the silicon liner 145 may react during the metal deposition to form metal silicide (e.g., RuSi), referred to as a reacted liner 155 in this disclosure. The reacted liner 155 may comprise silicon and the metal of the conductive material 160. The formation of the metal silicide in the reacted liner 155 may substantially decrease the resistivity of the silicon liner 145, and may be advantageous as a stable, final form of the liner left in the metal interconnects with minimal electrical resistance. Further, although not wishing to be limited by any theory, the formation of the metal silicide may be a self-limiting process and the initial thickness of the silicon liner 145 may determine the thickness of the reacted liner 155. The self-limiting feature may be beneficial in controlling the thickness of the liner thickness and ensuring that only a small portion of the metal is used for the metal silicide without substantially affecting the efficiency of metal deposition to form a conductive pattern.

[0034] The process temperature for the metal deposition may provide sufficient thermal energy to induce the reaction for metal silicide formation. In certain embodiments, an optional post-deposition annealing treatment may be performed. For example, the substrate 100 may be heated to a temperature between 200°C and 350°C using an inert gas flow. The annealing treatment may have several purposes. First, it may be beneficial to ensure the metal silicide formation in the silicon liner 145 in case the metal deposition alone was not sufficient for the reaction to complete, for example, when a relatively lower

temperature is used for the metal deposition. Further, the annealing treatment may improve the crystallinity of the conductive material 160 by increasing the grain diameter of crystals and reducing the grain boundaries within the reacted liner 155. The better crystallinity may advantageously reduce the resistivity and also help the performance of the subsequent etch process by reducing line edge roughness (LER) and line width roughness (LWR). It may also remove impurities such as, for example, carbon or oxygen in the conductive material 160. The optional annealing treatment may be performed using a gas containing H₂ gas, for example, a forming gas (H₂+Ar or H₂+N₂).

[0035] Although the reacted liner 155 is illustrated as a uniform layer in Figure 1C, in certain embodiments, it may comprise more than one composition. For example, the chemical composition of the reacted liner 155 may depend on the underlying layer (e.g., the second conductive fill 140 and the ILD 120), and it may comprise a metal silicate (e.g., RuSi_xO_y) selectively formed over the second ILD 170 as well as metal silicide (e.g., RuSi) selectively formed over the second conductive fill 140.

[0036] Figure 1D illustrates a cross sectional view of the substrate 100 after patterning the metal.

[0037] After the metal deposition, the conductive material 160 may be patterned, for example, to form a metal line. The patterning may be performed using a subtractive etch of the conductive material 160 with an etch mask. In various embodiments, a plasma etch process based on oxygen etch chemistry may be used. In one or more embodiments, dioxygen (O₂) may be used in the plasma etch process. In Figure 1D, in certain embodiments, a patterned portion of the conductive material 160 may be a metal line aligned to the metal via of the second conductive fill 140 and perpendicular to the lower metal line of the first

conductive fill 130. It should be noted that the illustrated pattern of the conductive material 160 is for example only, and any other reasonable patterning may be performed.

[0038] As mentioned above, the crystallinity of the conductive material 160 may affect the etch performance. In particular, during the patterning of the conductive material 160, line edge roughness (LER) and line width roughness (LWR) need to be controlled to be within the acceptable limit. A sidewall of the conductive material 160 where these parameters may be important is indicated by a dotted circle in Figure 1D. A higher crystallinity with less grain boundaries in the conductive material 160 may be preferable, which may be enabled by the use of metal silicide instead of conventional metal nitride liner materials.

10 [0039] Figure 1E illustrates a cross sectional view of the substrate 100 after dielectric-on-dielectric (DoD) deposition.

[0040] After the patterning of the conductive material 160, a second interlayer dielectric (ILD) 170 may be formed to further proceed the metal interconnect fabrication process. In various embodiments, the second ILD 170 may be selectively grown over the ILD 120 using
15 a dielectric-on-dielectric (DoD) deposition technique.

[0041] The process flow described above referring to Figures 1A-1E applies the silicon liner prior to depositing the conductive material 160 over the layer stack structure of the substrate 100, advantageously replacing a conventional metal nitride adhesion layer. The position and surface level where the silicon liner is applied in Figures 1A-1E are for example
20 only, and in various embodiments, the methods of silicon liner and metal deposition can also be applied to other levels where a liner may be used for metal deposition. In certain embodiments, a portion or the entirety of the liner 135 in Figure 1A may also potentially be replaced with a silicon liner, and the silicon liner can advantageously be used for a seed layer and adhesion layer to deposit the first conductive fill 130, the second conductive fill 140, or

both. Further, in other embodiments, any metal via or metal lines for a metal interconnect structure may be formed using the silicon liner in the same way as described above in the prior embodiments.

[0042] Figure 2 illustrates film resistivity of conventional liner materials (TiN and TaN) and ruthenium silicide (RuSi).

[0043] Figure 3 illustrates film resistivity of Ru/TiN layer stack and Ru/RuSi layer stack.

[0044] The inventors of this application demonstrated the superior electrical conductivity of metal silicide compared to conventional liner materials by experimentally investigating the film resistivity of the bulk materials and layer stacks. First, ruthenium silicide (RuSi), titanium nitride (TiN), and tantalum nitride (TaN) were examined for their film resistivity. In Figure 2, the film resistivity for the three materials were plotted in a logarithmic scale. The RuSi film exhibited a film resistivity more than one order, nearly two orders, of magnitude smaller than those of TiN and TaN, supporting that RuSi can be an attractive candidate as a liner material where low resistance is desired. Next, in order to investigate any effect of the seed layer on the property of the metal deposited, the film resistivity of film stacks were also examined using Ru/TiN layer stack and Ru/RuSi layer stack. As illustrated in Figure 3, the two samples exhibited comparable film resistivity, indicating that there is no substantial adverse effect of the RuSi liner on the conductivity of the Ru metal formed over the liner. It should be noted that the measurements were conducted for film resistivity and the current flows primarily through the top Ru portion of the layer stack.

[0045] Further, in a separate experiment of tape test, the inventors of this application confirmed the metal adhesion over the RuSi liner was sufficiently strong and therefore RuSi can be indeed used as an adhesion layer for the Ru deposition.

[0046] Grazing incidence X-ray diffraction (GIXRD) measurements were also performed to characterize the phases of Ru metal grown on the RuSi liner. Compared to the Ru metal grown on the TiN liner, the Ru metal on the RuSi liner exhibits a preferred orientation of crystal growth evidenced by a less number of peaks from different phases. This trend is common in both the out-of-plane and the in-plane measurements. As previously described above, the better crystallinity, as opposed to polycrystalline with many phases and grain boundaries, may advantageously reduce the resistivity and also help the performance of the subsequent etch process by reducing line edge roughness (LER) and line width roughness (LWR). The GIXRD data suggests that the RuSi may result in a better quality of Ru deposited than a conventional metal nitride liner regardless of whether an optional annealing treatment is performed.

[0047] Figures 4A-4C illustrate process flow charts of methods of metal deposition with a silicon liner in accordance with various embodiments. The process flow can be followed with the figures (e.g., Figures 1A-1C) discussed above and hence will not be described again.

[0048] In Figure 4A, a process flow 60 starts with forming an amorphous silicon (a-Si) liner over a substrate comprising a dielectric layer and a conductive layer, where the a-Si liner covers a surface of the dielectric layer and a surface of the conductive layer (block 610, Figure 1B). Subsequently, the a-Si liner may be converted into a silicon-containing layer comprising a metal (block 620, Figure 1C). The metal may then be deposited over the silicon-containing layer using the silicon-containing layer as a seed layer for the depositing, where the metal deposited over the silicon-containing layer and the conductive layer are electrically connected (block 630, Figure 1C). In certain embodiments, the conversion of the a-Si liner and the metal deposition may be performed as a single step of a vapor deposition process.

[0049] In Figure 4B, another process flow 62 starts with forming an amorphous silicon (a-Si) liner over a surface of the substrate, where the surface may comprise a conductive line and a dielectric layer, and where the substrate comprises a pattern of conductive lines formed within the dielectric layer (block 612, Figure 1B). Subsequently, ruthenium (Ru) may be deposited over the a-Si liner using a vapor deposition process, where a portion of the a-Si liner reacts with a portion of Ru to form RuSi at an initial stage of the vapor deposition process, and where Ru is deposited over RuSi (block 632, Figure 1C).

[0050] In Figure 4C, another process flow 64 starts with forming a recess in a dielectric layer of a substrate (block 602) and filling the recess with ruthenium (Ru) using a chemical vapor deposition (CVD) process (block 604), followed by planarizing a surface of the substrate, where the surface after the planarizing may comprise the dielectric layer and Ru (block 606, Figure 1A). Subsequently, an amorphous silicon (a-Si) liner may be formed over the surface (block 614, Figure 1B). Ru may then be deposited over the a-Si liner using a physical vapor deposition (PVD) process (block 634, Figure 1C).

[0051] Example embodiments of the invention are described below. Other embodiments can also be understood from the entirety of the specification as well as the claims filed herein.

[0052] Example 1. A method of processing a substrate includes forming an amorphous silicon (a-Si) layer over the substrate, where the substrate includes a dielectric layer and a conductive layer, and the a-Si liner covers a surface of the dielectric layer and a surface of the conductive layer. The method includes converting the a-Si liner into a silicon-containing layer including a metal; and depositing the metal over the silicon-containing layer using the silicon-containing layer as a seed layer for the depositing, where the metal deposited over the silicon-containing layer and the conductive layer are electrically connected.

[0053] Example 2. The method of example 1, further including, after the depositing, patterning the metal by performing a subtractive dry etch process.

[0054] Example 3. The method of one of examples 1 or 2, where the converting includes: exposing the a-Si liner to a vapor including the metal; and heating the substrate to a
5 temperature between 200°C and 350°C to react the metal with the a-Si liner.

[0055] Example 4. The method of one of examples 1 to 3, where the converting and the depositing are performed as a single process including exposing the substrate to a vapor including the metal.

[0056] Example 5. The method of one of examples 1 to 4, where the single process is
10 performed at a temperature between 200°C and 350°C.

[0057] Example 6. The method of one of examples 1 to 5, where the conductive layer includes aluminum (Al), copper (Cu), cobalt (Co), tungsten (W), ruthenium (Ru), osmium (Os), molybdenum (Mo), niobium (Nb), or nickel (Ni).

[0058] Example 7. The method of one of examples 1 to 6, where the metal includes
15 ruthenium (Ru).

[0059] Example 8. The method of one of examples 1 to 7, where the silicon-containing layer includes a metal silicide.

[0060] Example 9. The method of one of examples 1 to 8, where the silicon-containing layer includes a metal silicide formed over the conductive layer and a metal silicate formed
20 over the dielectric layer.

[0061] Example 10. A method of processing a substrate includes forming an amorphous silicon (a-Si) layer over a surface of the substrate, where the surface includes a conductive line and a dielectric layer, and the substrate includes a pattern of conductive lines formed

within the dielectric layer. The method includes depositing ruthenium (Ru) over the a-Si liner using a vapor deposition process, where a portion of the a-Si liner reacts with a portion of Ru to form RuSi at an initial stage of the vapor deposition process, and where Ru is deposited over RuSi.

- 5 [0062] Example 11. The method of example 10, where the a-Si liner has a thickness between 1 nm and 5 nm.

- [0063] Example 12. The method of one of examples 10 to 11, where the pattern of conductive lines has a pitch size between 5 nm and 20 nm. 13. The method of one of examples 1 to 11, where the vapor deposition process is performed at a temperature between
10 200°C and 350°C.

 [0064] Example 14. The method of one of examples 10 to 13, where the vapor deposition process is an atomic layer deposition (ALD) process, a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or a plasma-enhanced CVD (PECVD) process.

- 15 [0065] Example 15. The method of one of examples 10 to 14, where the a-Si liner is formed by an atomic layer deposition (ALD) process, a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or a plasma-enhanced CVD (PECVD) process.

- [0066] Example 16. A method of processing a substrate includes forming a recess in a
20 dielectric layer of the substrate; filling the recess with ruthenium (Ru) using a chemical vapor deposition (CVD) process; and planarizing a surface of the substrate, where the surface after the planarizing includes the dielectric layer and Ru. The method includes forming an amorphous silicon (a-Si) layer over the surface; and depositing Ru over the a-Si liner using a physical vapor deposition (PVD) process.

[0067] Example 17. The method of example 16, further including, after depositing Ru, patterning the PVD-deposited Ru to form a portion of a metal interconnect for a device component fabricated over the substrate.

[0068] Example 18. The method of one of examples 16 or 17, further including, after
5 depositing Ru, performing an annealing process to increase the crystallinity of the PVD-deposited Ru.

[0069] Example 19. The method of one of examples 16 to 18, where the PVD process induces a reaction of the a-Si liner to a layer including RuSi, and where the layer acts as a seed layer for the Ru deposition.

10 [0070] Example 20. The method of one of examples 16 to 19, where the PVD process is performed at a temperature between 200°C and 350°C.

[0071] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other
15 embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

WHAT IS CLAIMED IS:

1. A method of processing a substrate, the method comprising:
forming an amorphous silicon (a-Si) liner over the substrate, the substrate comprising a dielectric layer and a conductive layer, the a-Si liner covering a surface of the dielectric layer and a surface of the conductive layer;
converting the a-Si liner into a silicon-containing layer comprising a metal; and
depositing the metal over the silicon-containing layer using the silicon-containing layer as a seed layer for the depositing, wherein the metal deposited over the silicon-containing layer and the conductive layer are electrically connected.
2. The method of claim 1, further comprising, after the depositing, patterning the metal by performing a subtractive dry etch process.
3. The method of claim 1, wherein the converting comprises:
exposing the a-Si liner to a vapor comprising the metal; and
heating the substrate to a temperature between 200°C and 350°C to react the metal with the a-Si liner.
4. The method of claim 1, wherein the converting and the depositing are performed as a single process comprising exposing the substrate to a vapor comprising the metal.
5. The method of claim 4, wherein the single process is performed at a temperature between 200°C and 350°C.
6. The method of claim 1, wherein the conductive layer comprises aluminum (Al), copper (Cu), cobalt (Co), tungsten (W), ruthenium (Ru), osmium (Os), molybdenum (Mo), niobium (Nb), or nickel (Ni).

7. The method of claim 1, wherein the metal comprises ruthenium (Ru).
8. The method of claim 1, wherein the silicon-containing layer comprises a metal silicide.
9. The method of claim 1, wherein the silicon-containing layer comprises a metal silicide formed over the conductive layer and a metal silicate formed over the dielectric layer.
10. A method of processing a substrate, the method comprising:
 - forming an amorphous silicon (a-Si) liner over a surface of the substrate, the surface comprising a conductive line and a dielectric layer, the substrate comprising a pattern of conductive lines formed within the dielectric layer; and
 - depositing ruthenium (Ru) over the a-Si liner using a vapor deposition process, wherein a portion of the a-Si liner reacts with a portion of Ru to form RuSi at an initial stage of the vapor deposition process, and wherein Ru is deposited over RuSi.
11. The method of claim 10, wherein the a-Si liner has a thickness between 1 nm and 5 nm.
12. The method of claim 10, wherein the pattern of conductive lines has a pitch size between 5 nm and 20 nm.
13. The method of claim 10, wherein the vapor deposition process is performed at a temperature between 200°C and 350°C.
14. The method of claim 10, wherein the vapor deposition process is an atomic layer deposition (ALD) process, a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or a plasma-enhanced CVD (PECVD) process.

15. The method of claim 10, wherein the a-Si liner is formed by an atomic layer deposition (ALD) process, a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or a plasma-enhanced CVD (PECVD) process.
16. A method of processing a substrate, the method comprising:
 - forming a recess in a dielectric layer of the substrate;
 - filling the recess with ruthenium (Ru) using a chemical vapor deposition (CVD) process;
 - planarizing a surface of the substrate, the surface after the planarizing comprising the dielectric layer and Ru;
 - forming an amorphous silicon (a-Si) liner over the surface; and
 - depositing Ru over the a-Si liner using a physical vapor deposition (PVD) process.
17. The method of claim 16, further comprising, after depositing Ru, patterning the PVD-deposited Ru to form a portion of a metal interconnect for a device component fabricated over the substrate.
18. The method of claim 16, further comprising, after depositing Ru, performing an annealing process to increase the crystallinity of the PVD-deposited Ru.
19. The method of claim 16, wherein the PVD process induces a reaction of the a-Si liner to a layer comprising RuSi, and wherein the layer acts as a seed layer for the Ru deposition.
20. The method of claim 16, wherein the PVD process is performed at a temperature between 200°C and 350°C.