Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a substrate;

forming a first conductive layer over the substrate;

forming a first insulating layer over the substrate ~~and first conductive layer;~~

~~removing a portion of the first insulating layer to expose the first conductive layer;~~

forming a second conductive layer over the first conductive layer and first insulating layer;

forming an under bump metallization (UBM) layer around a bump formation area over a major surface of the second conductive layer and over side surfaces of the second conductive layer with respect to the major surface, the second conductive layer being exposed in the bump formation area;

forming a second insulating layer over the UBM layer and second conductive layer;

~~removing a portion of the second insulating layer over the bump formation area and a portion of the UBM layer;~~ and

forming a bump over the second conductive layer in the bump formation area, the bump contacting the UBM layer to seal a contact interface between the bump and second conductive layer.

2. The method of claim 1, wherein forming the UBM layer includes:

forming a third conductive layer over the second conductive layer; and

forming a fourth conductive layer over the third conductive layer, the fourth conductive layer being in contact with the bump.

3. The method of claim 2, wherein the fourth conductive layer includes a material selected from the group consisting of aluminum, titanium, chromium, titanium nitride, and titanium tungsten.

4. The method of claim 1, wherein forming the UBM layer includes:

forming a third conductive layer over the second conductive layer;

forming a fourth conductive layer over the third conductive layer; and

forming a fifth conductive layer over the fourth conductive layer, the fifth conductive layer being in contact with the bump.

5. The method of claim 1, wherein the second insulating layer contacts the bump.

~~6. The method of claim 1, wherein the UBM layer covers the second conductive layer outside the bump formation area.~~

~~7~~6. The method of claim 1, further including forming a seed layer over the first conductive layer and first insulating layer prior to forming the second conductive layer.

~~8~~7. A method of making a semiconductor device, comprising:

providing a substrate;

forming a first conductive layer over the substrate;

forming a first insulating layer over the substrate;

forming a second conductive layer over the first conductive layer and first insulating layer;

forming a multi-layer metallization pattern around an interconnect formation area over the second conductive layer, the second conductive layer being exposed in the interconnect formation area;

forming a second insulating layer over the multi-layer metallization pattern and contacting the second conductive layer ~~outside~~within the interconnect formation area; and

forming an interconnect structure over the second conductive layer in the interconnect formation area.

~~9~~8. The method of claim ~~8~~7, wherein forming the multi-layer metallization pattern includes:

forming a third conductive layer over the second conductive layer; and

forming a fourth conductive layer over the third conductive layer, the fourth conductive layer being in contact with the interconnect structure.

~~10~~9. The method of claim ~~9~~8, wherein the fourth conductive layer includes a material selected from the group consisting of aluminum, titanium, chromium, titanium nitride, and titanium tungsten.

1~~1~~0. The method of claim ~~8~~7, wherein forming the multi-layer metallization pattern includes:

forming a third conductive layer over the second conductive layer;

forming a fourth conductive layer over the third conductive layer; and

forming a fifth conductive layer over the fourth conductive layer, the fifth conductive layer being in contact with the interconnect.

121. The method of claim 87, wherein the interconnect structure includes a bump.

132. The method of claim 87, wherein the multi-layer metallization pattern covers the second conductive layer outside the interconnect formation area.

143. The method of claim 87, further including forming a seed layer over the first conductive layer and first insulating layer prior to forming the second conductive layer.

154. A method of making a semiconductor device, comprising:

providing a substrate;

forming a first conductive layer over the substrate;

forming a multi-layer metallization pattern around an interconnect formation area over the first conductive layer;

forming a first insulating layer over the multi-layer metallization pattern and over the first conductive layer outside the ~~interconnect formation area~~ multi-layer metallization pattern; and

forming an interconnect over the first conductive layer in the interconnect formation area.

165. The method of claim 154, further including:

forming a second conductive layer over the substrate prior to forming the first conductive layer;

forming a ~~first~~second insulating layer over the substrate; and

forming a seed layer over the ~~first~~second conductive layer and ~~first~~second insulating layer.

1~~7~~6. The method of claim 1~~5~~4, wherein forming the multi-layer metallization pattern includes:

forming a second conductive layer over the first conductive layer; and

forming a third conductive layer over the second conductive layer, the third conductive layer being in contact with the interconnect.

1~~8~~7. The method of claim 1~~5~~4, wherein forming the multi-layer metallization pattern includes:

forming a second conductive layer over the first conductive layer;

forming a third conductive layer over the second conductive layer; and

forming a fourth conductive layer over the third conductive layer, the fourth conductive layer being in contact with the interconnect.

1~~9~~8. The method of claim 1~~5~~4, wherein the interconnect includes a bump.

~~20~~19. A semiconductor device, comprising:

a semiconductor die;

a first conductive layer formed over the semiconductor die;

a first insulating layer formed over the semiconductor die;

a second conductive layer formed over the first conductive layer and first insulating layer;

a multi-layer metallization pattern formed around an interconnect formation area over the second conductive layer;

a second insulating layer formed over the multi-layer metallization pattern and over the second conductive layer outside the ~~bump formation area~~ multi-layer metallization pattern; and

an interconnect structure formed over the second conductive layer in the interconnect formation area.

2~~1~~0. The semiconductor device of claim ~~20~~19, further including:

a third conductive layer formed over the second conductive layer; and

a fourth conductive layer formed over the third conductive layer, the fourth conductive layer being in contact with the interconnect structure.

2~~2~~1. The semiconductor device of claim ~~20~~19, further including:

a third conductive layer formed over the second conductive layer;

a fourth conductive layer formed over the third conductive layer; and

a fifth conductive layer formed over the fourth conductive layer, the fifth conductive layer being in contact with the interconnect structure.

2~~3~~2. The semiconductor device of claim ~~20~~19, wherein the interconnect structure includes a bump.

2~~4~~3. The semiconductor device of claim ~~20~~19, wherein the multi-layer metallization pattern covers the second conductive layer outside the interconnect formation area.

254. The semiconductor device of claim 2019, further including a seed layer formed over the first conductive layer and first insulating layer prior to forming the second conductive layer.