

Description

The present invention relates generally to DC stabilization systems for use in color television receivers, and particularly to systems for stabilizing the DC levels of the respective color signal drives for a color kinescope in which protection is afforded against error introduction during the vertical sync interval of the received signals.

A well known technique for DC stabilization in television systems uses some form of keyed clamp circuit to clamp the received signal to a reference level during the "backporch" segment of the signal's horizontal retrace intervals. In conventional arrangements for developing line rate keying pulses for such keyed clamp circuits, which arrangements operate in response to horizontal flyback pulses derived from the receiver's deflection circuits, and/or in response to a differentiated version of a composite sync signal separated from the received signal, the train of developed keying pulses includes pulse components appearing during the vertical sync interval. Keying of the clamp circuit in response to such pulse components can introduce a DC error that may not be fully dissipated by the beginning of the display of the top of the television picture, with a consequence of an undesirable vertical shading of the displayed picture.

The present invention is directed to a DC stabilization system for color television receivers employing DC level control loops with voltage comparators keyed by line rate keying pulses with "backporch" timing, wherein the source of line rate keying pulses is rendered responsive to field rate pulses in such manner as to prevent keying of the voltage comparators during at least some of the line intervals occupied by the vertical synchronizing component. The keying prevention can aid in eliminating or reducing the visibility of the aforementioned vertical shading effect.

The protection afforded against error introduction during the vertical sync interval by a DC stabilization system in accordance with the present invention is of special importance in color television receivers of the type incorporating apparatus for automatic control of color kinescope biasing.

An illustrative arrangement for automatic control of color kinescope biasing in a color television receiver is that described in US-A-4,263,622. In the Hinn arrangement, a control period, occupying a period of several successive line intervals within a post-sync portion of each vertical blanking interval, is set aside for monitoring a black level current produced by an electron gun under reference signal conditions, for detection of departures from a desired current level, and for readjustment of gun bias to oppose the undesired departures. During a portion of the control period, the color kinescope grid receives a conduction-enhancing pulse; bias control is based upon information derived as indicative of the change in cathode current level introduced by the grid pulsing. An advantageous system for utilization

of the above-described Hinn approach in maintenance of an appropriate bias relationship among the color kinescope's gun trio (in the face of aging and other parameter variations) is described in US-A-4,484,228 of R. P. Parker.

In color television receivers employing automatic kinescope bias (AKB) control circuits of the type exemplified by the structures of the aforementioned Hinn and Parker patents, the residue of DC level errors built up during a vertical sync interval may, at the onset of the AKB control interval shortly thereafter, be of sufficient magnitude as to result in erroneous bias settings by the AKB control circuits. In instances where the resultant bias errors are not matched, an undesired background coloring can be a consequence. Where, however, a DC stabilization system in accordance with the present invention is employed, the above-noted keying prevention within the vertical sync interval lessens the problem of erroneous bias settings by the subsequent AKB control circuits.

In a DC stabilization system in accordance with an illustrative embodiment of the present invention, a trio of control loops is provided, each including a keyed voltage comparator for comparing a respectively different one of a set of color signals with a common reference voltage during "backporch" keying periods defined by the output pulses provided by a source of line rate keying pulses. In the first control loop, the keyed comparator's output is used to adjust the DC level of a luminance signal input to signal combining means which form the set of color signals. In the second control loop, the keyed comparator's output is used to adjust the DC level of a first color-difference signal input to the signal combining means. In the third control loop, the keyed comparator's output is used to adjust the DC level of a second color-difference signal input to the signal combining means. The source of line rate keying pulses is rendered responsive to field rate pulses (e.g., vertical sync pulses, or vertical drive pulses) indicative of the timing of the appearance of the received signal's vertical synchronizing component. The response to the field rate pulse is such as to bar the keying of the loop's comparators during all, or a major portion of, the received signal's vertical sync interval.

Illustratively, the keying pulse source comprises a sandcastle pulse encoding/decoding system, with the sandcastle pulse encoder subject to field rate keying to effect the desired comparator keying pulse deletions.

In the accompanying drawing:

FIGURE 1 illustrates, partially schematically and partially by block representation, a portion of a color television receiver incorporating a DC stabilization system in accordance with an embodiment of the present invention;

FIGURE 1a illustrates, partially schematically and partially by block representation, an additional receiver circuitry which may be desirably associated with the system of FIGURE 1; and

FIGURE 2 shows, partially schematically and

partially by block representation, an illustrative circuit arrangement for implementing the function of a backporch gating pulse source in the system of FIGURE 1.

In the system of FIGURE 1, luminance signals appearing at terminal L are applied to the input of luminance signal processing circuits 13. Illustratively, the luminance signals appearing at terminal L may comprise the luminance signal output of comb filter apparatus (of the type shown in US-A-4,096,516 — Pritchard, for example), employed in a color television receiver to separate the luminance and chrominance components of a received composite signal. The output of the luminance signal processing circuits 13, appearing at terminal Y, is supplied as a luminance signal input to a trio of signal combiners 25, 27 and 29.

Chrominance signals appearing at terminal C are applied to the input of chrominance signal processing circuits 15. Illustratively, the chrominance signals appearing at terminal C may comprise the chrominance signal output of the receiver's comb filter apparatus referred to above. The chrominance signal processing circuits 15 include a suitable detection system for recovering a pair of color-difference signals from the received chrominance component. Illustratively, the color-difference signal outputs of the processing circuits 15 comprise I color-difference signals appearing at terminal ICD, and Q color-difference signals appearing at terminal QCD.

The respective Q and I color-difference signal outputs of processing circuits 15 are applied as signal inputs to respective differential amplifiers 19 and 21. Differential amplifiers 19 and 21 also receive control inputs from apparatus to be described subsequently. Matrix circuits 23, illustratively of the general form disclosed in US-A-4,272,778 — Harwood, et al., receive as inputs push-pull versions of the Q color-difference signal, developed by differential amplifier 19 at terminals +Q and -Q, and push-pull versions of the I color-difference signal, developed by differential amplifier 21 at terminals +I and -I. Matrix circuits 23 provide appropriate combinations of the input signals to develop a trio of different color-difference signal outputs.

A G-Y color-difference signal, appearing at matrix output terminal G-Y, is supplied to signal combiner 25 for combination with the luminance signal from terminal Y to form a green color signal at combiner output terminal G. A B-Y color-difference signal, appearing at matrix output terminal B-Y, is supplied to signal combiner 27 for combination with the luminance signal from terminal Y to form a blue color signal at combiner output terminal B. An R-Y color-difference signal, appearing at matrix output terminal R-Y, is supplied to signal combiner 29 for combination with the luminance signal from terminal Y to form a red color signal at combiner output terminal R.

Before considering the DC stabilization system elements of the FIGURE 1 arrangement, it is appropriate to consider the FIGURE 1a showing of

apparatus for utilizing the respective color signals at the combiner output terminals R, B and G. As shown in FIGURE 1a, a trio of kinescope drivers 73, 74 and 75 are provided, responsive respectively to the red color signal appearing at terminal R, the blue color signal appearing at terminal B, and the green color signal appearing at terminal G.

Display of color images in response to the trio of color signals is effected on the viewing screen of a color kinescope 77, incorporating an electron gun assembly comprising individually energized cathode electrodes 78R, 78B and 78G and a commonly energized control grid structure 79. The red content of the display color image is determined by control of the intensity of an electron beam emanating from cathode 78R, which is driven by the output of kinescope driver 73. The blue content of the displayed color image is determined by control of the intensity of an electron beam emanating from cathode 78B, which is driven by the output of kinescope driver 74. The green content of the displayed color image is determined by control of the intensity of an electron beam emanating from cathode 78G, which is driven by an output of kinescope driver 75.

The FIGURE 1a apparatus also includes automatic kinescope bias control circuits 76, which desirably operate in the manner described in the aforementioned US-A-4,484,228. Thus, the bias control circuits 76 includes means for supplying a conduction-enhancing pulse to the kinescope control grid 79 during a predetermined portion of the bias control interval (which interval, illustratively, occupies a period of seven-lines duration during a post-sync portion of each vertical blanking interval of the received signal). The bias control circuits 76 are responsive to inputs derived from the respective drivers (73, 74, 75) for sensing beam current changes induced by the grid pulsing, and develop therefrom respective DC outputs for application to the respective drivers (73, 74, 75) to suitably control the biases of the respective kinescope cathodes (78R, 78B, 78G), to which the driver outputs are DC coupled.

The manner in which the DC levels of the respective color signal inputs to the drivers (73, 74, 75) are controlled will now be explained, with reference to a stabilization system illustrated in FIGURE 1, which includes a trio of keyed voltage comparators 31, 33 and 35. Each of the comparators 31, 33 and 35 is enabled only during keying periods established by keying pulses delivered to terminal K from a pulse source (50) to be explained subsequently.

Comparator 31 accepts the green color signal from terminal G for comparison with a reference input derived from a reference voltage terminal RV, and develops its output across a storage capacitor 32. The red color signal at terminal R is subject to comparison with the same reference voltage (from terminal RV) in comparator 33, which develops its output across storage capacitor 34. The blue color signal at terminal B is

also subject to comparison with the reference voltage appearing at terminal RV in comparator 35, which develops its output across storage capacitor 36.

A DC potential is developed across capacitor 32 which is representative of the difference, if any, existing between the green signal and reference inputs to comparator 31 during the aforementioned keying periods, and is held during the intervals between successive keying periods. This DC potential is supplied as an input to differential amplifier 19, to modify the DC level of the Q color-difference signal inputs to matrix circuits 23 in a direction tending to reduce the difference between the inputs of comparator 31. Similarly, the DC potential stored across capacitor 34 (representative of the difference, if any, existing between the red signal and reference inputs to comparator 33 during the keying periods) is supplied as an input to differential amplifier 21, to modify the DC level of the I color-difference signal inputs to matrix circuits 23 in a direction tending to reduce the difference between the inputs of comparator 33.

The DC potential stored across capacitor 36, which is representative of the difference, if any, existing between the blue signal and reference inputs to comparator 35 during the keying periods, is utilized as a control input to the luminance signal processing circuits 13 to modify the DC level of the luminance signal input to combiners 25, 27, 29 in a direction tending to reduce the difference between the inputs of comparator 35.

In the system of FIGURE 1, the keying pulses delivered to terminal K are developed by a field-rate blanked backporch gating pulse source 50. The train of pulses provided by source 50 comprise keying pulses recurring at a line rate with a timing permitting coincidence with a backporch segment of those horizontal retrace intervals that occur during the active scan periods that intervene between successive vertical blanking intervals. The operation of the control loops utilizing the keyed comparators (31, 33, 35) stabilizes the blanking levels of the respective color signals (which are exhibited during such backporch segments) at the level of the common reference voltage available at terminal RV.

A field-rate blanking of keying pulses developed by source 50 occurs, however, during the portion of each vertical blanking interval occupied by the vertical synchronizing component (a serrated vertical sync pulse, of a three-line duration) to effect an interruption of keying pulse appearances at terminal K. The reason for interrupting keying pulse appearances during the vertical sync interval is that the keying periods that would otherwise be provided during such interval will coincide, not with exhibitions of the blanking level of the received signal, but rather with exhibitions of the sync peak level of the received signals. The consequence of a build-up of an erroneous correction voltage on the respective storage capacitors (32, 34, 36) is avoid-

able by eliminating comparator keying during the vertical sync interval.

Ideally, the field-rate blanking of keying pulse development by source 50 should eliminate every instance of comparator keying during the vertical sync interval to maximize protection against error. In practice, however, it has been found that adequate protection against the adverse effects of keying within the vertical sync interval can be achieved with a form of field rate blanking that permits an initial instance of comparator keying at the beginning of the vertical sync interval while barring comparator keying during the remainder of the vertical sync interval.

A particular example of a circuit arrangement for implementing the function of the field-rate blanked backporch gating pulse source 50 of the FIGURE 1 system is presented in FIGURE 2. In particular, FIGURE 2 shows a color television receiver portion incorporating a trilevel sandcastle pulse encoding/decoding system, in which an output of a sandcastle decoder supplies keying pulses to terminal K of the FIGURE 1 system, and in which the desired field-rate blanking of backporch keying pulses is achieved by apparatus associated with the sandcastle pulse encoder.

Where a multiplicity of keying functions with different timing requirements are subject to performance within a common integrated circuit, a savings in terminal count may be realized by externally forming a composite multilevel keying waveform for delivery to a single input terminal of the integrated circuit, and including within the integrated circuit, level-sensitive decoder circuits for extracting respective keying waves of different timing from the delivered composite waveform (which is viewable as having a sandcastle-like profile). In color television receivers of the type considered here (incorporating AKB control circuits), use of sandcastle pulses of a trilevel form has been found appropriate, as explained in EP-A-0,147,981 and EP-A-0,147,982 corresponding to US-A-4,558,355 entitled respectively "Trilevel Sandcastle Pulse Encoder" and US-A-4,549,202 "Trilevel Sandcastle Pulse Encoding/Decoding System". In Figure 2, a trilevel sandcastle pulse encoding/decoding system of the Hettiger type is subject to modification to implement the aims of the present invention.

In FIGURE 2, the receiver's sync separator 81 accepts, as an input, luminance signals from terminal L of the FIGURE 1 system. At the separator output terminal CS appears a composite sync waveform (separated from the remainder of the received signal). Signals from terminal CS are commonly applied to an integrating circuit 82 and to a differentiating circuit 83. Separated vertical synchronizing pulses, formed by integration of the composite sync waveform, appear at the integrating circuit output terminal V_s. Separated horizontal synchronizing pulses, formed by differentiation of the composite sync waveform, appear at the differentiating circuit output terminal HS. Signals from terminals V_s and HS are supplied to the receiver's

deflection circuits 84 to synchronize the development therein of respective field and line scanning waveforms (used in deflection of the beams of color kinescope 77 of FIGURE 1a). Available at respective output terminals VD, HD, HF, VB and HB of the deflection circuit 84 are, respectively, a train of vertical drive pulses, a train of horizontal drive pulses, a train of horizontal flyback pulses, a train of vertical retrace blanking pulses, and a train of horizontal retrace blanking pulses.

Signals from terminals HB and VB of the deflection circuits 84 are supplied to a retrace blanking pulse generator 85 which forms composite retrace blanking waves at its output terminal RB. The composite retrace blanking waves illustratively comprise a train of negative-going retrace blanking pulse components, inclusive of relatively wide pulse components, recurring at a field rate, which encompass the recurring periods of vertical retrace of the beams of color kinescope 77, and narrower pulse components, recurring at a line rate, which encompass periods of horizontal retrace of said beams lying outside of the vertical retrace blanking intervals. The signals at terminal RB are applied to the base electrode of an NPN transistor 90, disposed with its emitter electrode grounded, and with its collector electrode linked by a resistor 91 to a terminal P. A resistor 92 is connected between terminal P and the positive terminal (+V_s) of an operating potential supply.

Signals from the differentiating circuit output terminal HS and from terminal HF of the deflection circuits 84 are supplied as inputs to a burst gating pulse generator 86. The burst gating pulse generator 86 may illustratively be of the type disclosed in a US-A-4,581,630 of R. Fernsler et al. The output of generator 86 at its output terminal BG illustratively comprises a train of negative-going burst gating pulse components (narrower in width than the horizontal retrace blanking pulse components) which continuously recur at a line rate, and which are timed to coincide with back-sweep segments of the horizontal blanking portions of those line intervals that lie outside the vertical blanking interval. It will be noted that the train of pulses at terminal BG includes pulse components falling within the vertical sync interval. The pulses at terminal BG are supplied to the base electrode of an NPN transistor 93, disposed with its emitter electrode grounded, and with its collector electrode connected to terminal P via a resistor 94.

For the purposes of the present illustrative embodiment of the invention, the emitter-collector path of transistor 93 is shunted by the emitter-collector path of another NPN transistor 101 (disposed with its emitter electrode grounded, and with its collector electrode directly connected to the collector electrode of transistor 93). Vertical sync pulses (of positive-going form) from terminal V_s are applied to the base electrode of transistor 101.

Signals from terminals VD and HD of deflection circuits 84 are supplied as inputs to logic circuits 87. The logic circuits 87 function to develop a

kinescope bias control interval timing pulse output at output terminal A, for delivery as a keying input to the AKB interval pulse generator 88. The aforementioned copending Parker US-A-4,484,228 discloses a suitable arrangement for implementing the function of logic circuits 87. Illustratively, the train of pulses at terminal A comprise recurring field rate pulses timed to occupy a seven-line period within a post-sync portion of the vertical blanking interval of the received signals, which period defines the automatic kinescope bias (AKB) control interval. During each pulse appearance at terminal A, generator 88 is keyed to function as a low impedance voltage source, effectively clamping its output terminal (J) to a predetermined positive DC level. Terminal J is linked to the previously mentioned terminal P by a resistor 95 (shunted by a speed-up capacitor 96), which exhibits an impedance which is large relative to the output impedance of generator 88 in its keyed state. Between pulse appearances at terminal A, generator 88 is effectively open-circuited to exhibit an output impedance which is large relative to the impedance exhibited by resistor 95.

The circuitry of FIGURE 2 thus far described cooperates to develop a sandcastle pulse of trilevel form at terminal J in a manner now to be explained. In the initial explanation, the effect of the operation of transistor 101 will not be considered.

During each AKB control interval, terminal J is clamped to a positive level determined by the output of generator 88 and is substantially unaffected by the voltage excursions appearing at terminal P. The voltage provided by generator 88 functioning as a keyed low impedance voltage source establishes the middle pulse level of the trilevel sandcastle pulses. During periods outside the recurring AKB control intervals, the open-circuiting of generator 88 permits terminal J to follow excursions at terminal P. These excursions vary between a retrace blanking pulse level (lower than the middle pulse level), a burst gating pulse level (higher than the middle pulse level), and a base level (lower than the retrace blanking pulse level). The manner in which these levels are established at terminal P will now be explained.

During periods when negative-going pulse components are absent from both of the terminals RB and BG (e.g., during active scan times), transistors 90 and 93 are both strongly conducting. The voltage level at terminal P under these circumstances (i.e., the base level) is determined by the voltage division ratio of a voltage divider formed by resistor 92 in series with the parallel combination of resistors 91 and 94 across the operating potential supply terminals.

During portions of the retrace blanking intervals not overlapping with the burst gating intervals, transistor 90 is cut off while transistor 93 remains strongly conducting. The voltage level at terminal P under these circumstances (i.e., the low, retrace blanking, pulse level) is determined by the voltage division ratio of a voltage divider formed by

resistor 92 in series with resistor 94 across the operating potential supply terminals.

During each burst gating interval (always overlapping a retrace blanking interval portion), transistors 90 and 93 are both cut off. The voltage level at terminal P under these circumstances (i.e., the high, burst gating, pulse level) is determined by the undivided output potential of the operating potential supply associated with terminal $+V_s$.

The trilevel sandcastle pulses at terminal J are coupled via resistor 97 to terminal SC, which is illustratively an input terminal of the integrated circuit upon which circuits of the FIGURE 1 system are realized. Signals at terminal SC are supplied as a signal input to a voltage comparator 98. Comparator 98 (a part of an on-chip sandcastle pulse decoder) serves to compare the incoming sandcastle pulses with a reference voltage from terminal VR. The level of the reference voltage at terminal VR is selected to lie between the middle (AKB) and high (burst gating) pulse levels of the trilevel sandcastle pulses. An on-chip keying circuit 99 responds to the output of comparator 98 by delivering a keying pulse to terminal K of the FIGURE 1 system whenever comparator 98 indicates that the reference voltage at terminal VR has been exceeded by the level of the sandcastle pulse train.

As thus far explained (i.e., without consideration of the operation of transistor 101), the sandcastle pulse encoder will permit excursions at terminal P to the high burst gating pulse level during the vertical sync interval, and such excursions will be translated by the decoder 98—99 into keying pulses appearing at terminal K during the vertical sync interval. This is not the result when the operation of transistor 101 is additionally considered, however. During each vertical sync pulse appearance, transistor 101 is rendered strongly conducting by the signal from terminal V_s . During such periods, the effect of a cut off of transistor 93 does not result in a rise of the potential at terminal P to the high, burst gating, pulse level. That is, conduction by transistor 101 continues the connection of voltage divider 92/94 across the operating potential supply terminals so as to maintain the low (retrace blanking) pulse level. The absence of excursions to the high burst gating pulse level at terminal P during the vertical sync interval results in a concomitant failure of keying circuit 99 to deliver keying pulses to terminal K during such absence.

In practical realizations of integrating circuit 82, the rise of the output at terminal V_s may not be fast enough to ensure prevention of a first keying pulse development during the vertical sync interval, but prevention is assured throughout the remainder of the vertical sync interval. As suggested by the dotted-line in FIGURE 2, an alternative to the use of the signals at terminal V_s for driving transistor 101 is the use of the vertical drive pulses at terminal VD for driving transistor 101. Yet another manner of implementing the principles of the present invention is presented in

EP-A-145,491 corresponding to US-A-4,583,121 entitled "Backporch Gating Pulse Generator Subject to Disabling During Vertical Sync Interval".

In EP-A-145,491, transistor 101 is not required, as the desired suppression is provided by generator 86 (via a modification of the burst gating pulse generator of the aforementioned Fernsler, et al. application).

Claims

1. A color television receiver for displaying color images in response to composite video signals inclusive of respective image-representative luminance and chrominance signal components and line-rate and field-rate deflection synchronizing components, said image-representative components being absent during a vertical blanking portion of each field interval and during horizontal blanking portions of line intervals lying outside of said vertical blanking portions, said field rate deflection synchronizing component appearing during a succession of line intervals within each of said vertical blanking portions said receiver including a luminance signal channel for processing said luminance signal component, a chrominance signal channel for processing said chrominance signal component and recovering therefrom first and second color-difference signals, a signal combining means responsive to said first and second color-difference signals and said processed luminance signal components for forming first, second, and third color signals and a DC stabilization system, the DC stabilization system being characterized by:

- a source (50) of line rate keying pulses;
- a first (35, 13, 25, 27, 29) control loop for controlling the DC level of said first color signal formed by said signal combining means;
- a second (31, 19, 23) control loop for controlling the DC level of said second color signal formed by said signal combining means; and
- a third (33, 21, 23) control loop for controlling the DC level of said third color signal formed by said signal combining means and wherein each of said control loops includes a keyed voltage comparator (31; 33; 35) for comparing a respectively different one of said color signals with a common reference voltage (RV) during recurring keying periods defined by the line rate keying pulses provided by said source; and
- said source (50) of line rate keying pulses is rendered responsive to field rate pulses indicative of the timing of the appearance of said field rate deflection synchronizing component in such manner as to prevent keying of said voltage comparator during at least some of said succession of line intervals.

2. A receiver in accordance with Claim 1, wherein the timing of said line rate keying pulses provided by said source (50) is such as to coincide with the backporch segments of the horizontal blanking portions of said line intervals lying outside said vertical blanking portions.



resistor 92 in series with resistor 94 across the operating potential supply terminals.

During each burst gating interval (always overlapping a retrace blanking interval portion), transistors 90 and 93 are both cut off. The voltage level at terminal P under these circumstances (i.e., the high, burst gating, pulse level) is determined by the undivided output potential of the operating potential supply associated with terminal +V_s.

The trilevel sandcastle pulses at terminal J are coupled via resistor 97 to terminal SC, which is illustratively an input terminal of the integrated circuit upon which circuits of the FIGURE 1 system are realized. Signals at terminal SC are supplied as a signal input to a voltage comparator 98. Comparator 98 (a part of an on-chip sandcastle pulse decoder) serves to compare the incoming sandcastle pulses with a reference voltage from terminal VR. The level of the reference voltage at terminal VR is selected to lie between the middle (AKB) and high (burst gating) pulse levels of the trilevel sandcastle pulses. An on-chip keying circuit 99 responds to the output of comparator 98 by delivering a keying pulse to terminal K of the FIGURE 1 system whenever comparator 98 indicates that the reference voltage at terminal VR has been exceeded by the level of the sandcastle pulse train.

As thus far explained (i.e., without consideration of the operation of transistor 101), the sandcastle pulse encoder will permit excursions at terminal P to the high burst gating pulse level during the vertical sync interval, and such excursions will be translated by the decoder 98—99 into keying pulses appearing at terminal K during the vertical sync interval. This is not the result when the operation of transistor 101 is additionally considered, however. During each vertical sync pulse appearance, transistor 101 is rendered strongly conducting by the signal from terminal V_s. During such periods, the effect of a cut off of transistor 93 does not result in a rise of the potential at terminal P to the high, burst gating, pulse level. That is, conduction by transistor 101 continues the connection of voltage divider 92/94 across the operating potential supply terminals so as to maintain the low (retrace blanking) pulse level. The absence of excursions to the high burst gating pulse level at terminal P during the vertical sync interval results in a concomitant failure of keying circuit 99 to deliver keying pulses to terminal K during such absence.

In practical realizations of integrating circuit 82, the rise of the output at terminal V_s may not be fast enough to ensure prevention of a first keying pulse development during the vertical sync interval, but prevention is assured throughout the remainder of the vertical sync interval. As suggested by the dotted-line in FIGURE 2, an alternative to the use of the signals at terminal V_s for driving transistor 101 is the use of the vertical drive pulses at terminal VD for driving transistor 101. Yet another manner of implementing the principles of the present invention is presented in

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Claims

1. A color television receiver for displaying color images in response to composite video signals inclusive of respective image-representative luminance and chrominance signal components and line-rate and field-rate deflection synchronizing components, said image-representative components being absent during a vertical blanking portion of each field interval and during horizontal blanking portions of line intervals lying outside of said vertical blanking portions, said field rate deflection synchronizing component appearing during a succession of line intervals within each of said vertical blanking portions said receiver including a luminance signal channel for processing said luminance signal component, a chrominance signal channel for processing said chrominance signal component and recovering therefrom first and second color-difference signals, a signal combining means responsive to said first and second color-difference signals and said processed luminance signal components for forming first, second, and third color signals and a DC stabilization system, the DC stabilization system being characterized by:

a source (50) of line rate keying pulses;
a first (35, 13, 25, 27, 29) control loop for controlling the DC level of said first color signal formed by said signal combining means;

a second (31, 19, 23) control loop for controlling the DC level of said second color signal formed by said signal combining means; and

a third (33, 21, 23) control loop for controlling the DC level of said third color signal formed by said signal combining means and wherein

each of said control loops includes a keyed voltage comparator (31; 33; 35) for comparing a respectively different one of said color signals with a common reference voltage (RV) during recurring keying periods defined by the line rate keying pulses provided by said source; and

said source (50) of line rate keying pulses is rendered responsive to field rate pulses indicative of the timing of the appearance of said field rate deflection synchronizing component in such manner as to prevent keying of said voltage comparator during at least some of said succession of line intervals.

2. A receiver in accordance with Claim 1, wherein the timing of said line rate keying pulses provided by said source (50) is such as to coincide with the backporch segments of the horizontal blanking portions of said line intervals lying outside said vertical blanking portions.



3. A receiver in accordance with Claim 1 or 2, wherein the output of the keyed comparator (35) of said first control loop is used to adjust the DC level of the luminance signal input to said signal combining means (25, 27, 29), the output of the keyed comparator (31) of said second control loop is used to adjust the DC level of said first color-difference signal input to said signal combining means, and the output of the keyed comparator (33) of said third control loop is used to adjust the DC level of said second color-difference signal input to said signal combining means.

4. A receiver in accordance with any one of Claims 1 to 3 wherein said receiver includes a color kinescope (77) having a plurality of beam intensity control electrodes (78R, 78B, 78G) for controlling the intensity of respective ones of a plurality of electron beams tracing a raster of scanning lines upon a viewing screen, each of said control electrodes receiving a respectively different one of said color signals; and means (76) for automatically controlling the biases on the respective control electrodes during periodic bias control intervals encompassing a plurality of line intervals falling subsequent to said succession of line intervals within each of said vertical blanking portions,

the line rate keying pulses provided by said source (50) being subject to interruption during said plurality of subsequent line intervals.

5. A receiver in accordance with Claim 4, wherein:

said luminance signal channel, said chrominance signal channel, and said signal combining means are realized on a common, monolithic integrated circuit;

said source of line rate keying pulses includes a trilevel sandcastle pulse encoder, external to said integrated circuit, for forming a train of trilevel sandcastle pulses in response to a first train (RB) of monolevel pulses encompassing periods of retrace for said beams, to a second train (BG) of monolevel pulses, each of the pulses of said second train overlapping in time a portion of a pulse of said first train, and to a third train (AKB) of monolevel pulses timed to coincide with said periodically recurring bias control intervals said train of trilevel sandcastle pulses exhibiting the highest of its three pulse levels during said backporch segments and exhibits the middle one of said three pulse levels throughout said bias control interval,

a voltage comparator (98), realized on said integrated circuit, for comparing said train of trilevel sandcastle pulses with a reference voltage (VR) of a level intermediate said highest and said middle one of said pulse levels, and

means (99), realized on said integrated circuit and responsive to an output of said voltage comparator, for forming said line rate keying pulses when the level of said trilevel sandcastle pulse train exceeds said reference voltage; and

said trilevel sandcastle pulse encoder includes means (101) responsive to said field rate pulses (VS) for barring excursions of said trilevel sand-

castle pulse train to said highest level during at least some of the line intervals in said succession of line intervals.

6. A receiver in accordance with Claim 5, wherein said trilevel sandcastle pulse encoder includes:

a source (+V_s) of DC potential;

first (92) and second (94) resistors; and a first transistor (93) having a base electrode connected to receive said second train (BG) of monolevel pulses, and an emitter-collector path disposed in series with said first and second resistors across said source of DC potential;

the level exhibited by said train of trilevel sandcastle pulses during periods outside of said bias control intervals is determined in accordance with the voltage appearing at the junction of said first and second resistors; and

said excursion barring means includes a second transistor (101) having a base electrode connected to receive said field rate pulse (VS), and an emitter-collector path connected in shunt with the emitter-collector path of said first transistor.

7. A receiver in accordance with Claim 6, wherein said first transistor (93) is cut off in response to an appearance of a pulse (BG) of said second train, and said second transistor (101) is rendered conducting during at least a portion of each period of appearance of said vertical synchronizing component in response to said field rate pulses (VS).

Patentansprüche

1. Farbempfänger zur Wiedergabe von Farbbildern aufgrund eines Videosignalgemisches, welches bilddarstellende Leuchtdichte- und Farbsignalkomponenten sowie zeilenfrequente und bildfrequente Ablenksynchronkomponenten enthält, welche während eines Vertikalaustabschnittes jedes Halbbildintervalls und während außerhalb der Vertikalaustabschnitte liegender Horizontalaustabschnitte der Zeilenintervalle fehlen, wobei die halbbildfrequente Ablenksynchronkomponente während einer Folge von Zeilenintervallen innerhalb jedes Vertikalaustabschnittes auftreten, wobei Teile des Empfängers einen Leuchtdichtesignalkanal zur Verarbeitung der Leuchtdichtesignalkomponente, einen Farbsignalkanal zur Verarbeitung der Farbsignalkomponente und Gewinnung erster und zweiter Farbdifferenzsignale aus dieser sowie eine Signalkombinationsschaltung enthalten, die bei Zuführung der ersten und zweiten Farbdifferenzsignale und der verarbeiteten Leuchtdichtesignalkomponenten ein erstes, zweites und drittes Farbsignal bildet, und mit einem Gleichspannungsstabilisierungssystem, das gekennzeichnet ist durch eine Quelle (50) zeilenfrequenter Tastimpulse, eine erste Regelschleife (35, 13, 25, 27, 29) zur Regelung des Gleichspannungspegels des von der Signalkombinationsschaltung gebildeten ersten Farbsignals, eine zweite Regelschleife (31, 19, 23) zur Rege-



lung des Gleichspannungspegels des von der Signalkombinationsschaltung gebildeten zweiten Farbsignals, und

eine dritte Regelschleife (33, 21, 23) zur Regelung des Gleichspannungspegels des von der Signalkombinationsschaltung gebildeten dritten Farbsignals,

wobei jede dieser Regelschleifen einen getasteten Spannungsvergleicher (31; 33; 35) zum Vergleich jeweils eines anderen der drei Farbsignale mit einer gemeinsamen Bezugsspannung (RV) während wiederkehrender Tasterperioden enthält,

welche durch von der Quelle gelieferte zeilenfrequente Tastimpulse bestimmt sind,

und wobei die Quelle (50) der zeilenfrequenten Tastimpulse auf das zeitliche Auftreten der halbbildfrequenten Ablensynchronimpulse anzeigende halbbildfrequente Impulse derart ansprechbar gemacht wird, daß ein Tasten des Spannungsvergleichers während mindestens einiger der aufeinanderfolgenden Zeilenimpulse verhindert wird.

2. Empfänger nach Anspruch 1, bei dem die von der Quelle (50) gelieferten zeilenfrequenten Impulse zeitlich derart liegen, daß sie mit den Schwarzschnittern der außerhalb der Vertikalaustastabschnitte liegenden Zeilenintervalle zusammenfallen.

3. Empfänger nach Anspruch 1 oder 2, bei dem das Ausgangssignal des getasteten Vergleichers (35) der ersten Regelschleife zur Einstellung des Gleichspannungspegels des Leuchtdichteingangssignals für die Signalkombinationsschaltung (25, 27, 29) benutzt wird, das Ausgangssignal des getasteten Vergleichers (31) der zweiten Regelschleife zur Einstellung des Gleichspannungspegels des ersten Farbdifferenzeingangssignals zur Signalkombinationsschaltung benutzt wird und das Ausgangssignal des getasteten Vergleichers (33) der dritten Regelschleife zur Einstellung des Gleichspannungspegels des zweiten Farbdifferenzeingangssignals zur Signalkombinationsschaltung benutzt wird.

4. Empfänger nach einem der Ansprüche 1 bis 3, mit einer Farbbildröhre (77), die eine Mehrzahl von Strahlintensitätssteuerelektroden (78R, 78B, 78G) zur Steuerung der Intensität je eines von mehreren Elektronenstrahlen aufweist, welche ein Raster von Abtastlinien auf einem Bildschirm schreiben und deren jeder ein jeweils anderes der drei Farbsignale zugeführt wird, ferner mit einer Schaltung (76) zur automatischen Regelung der Vorspannungen der jeweiligen Steuerelektroden während periodischer Vorspannungsregelintervalle, die eine Mehrzahl von Zeilenintervallen umfassen, welche ihrerseits anschließend an die Folge von Zeilenintervallen innerhalb jedes der Vertikalaustastabschnitte fallen, wobei die von der Quelle (50) gelieferten zeilenfrequenten Tastimpulse während der Mehrzahl aufeinanderfolgender Zeilenintervalle unterbunden sind.

5. Empfänger nach Anspruch 4, bei dem der Leuchtdichtesignalkanal, der Farbsignalkanal und die Signalkombinationsschaltung auf

einer gemeinsamen monolithischen integrierten Schaltung ausgebildet sind,

die Quelle zeilenfrequenter Tastimpulse einen außerhalb der integrierten Schaltung befindlichen Dreipegel-Sandburg-Impulscodierer enthält zur Bildung eines Zuges dreipegeliger Sandburg-Impulse aufgrund eines ersten Zuges von Strahlrücklaufperioden umfassenden einpegeligen Impulsen, eines zweiten Zuges (BG) einpegeliger Impulse, deren jeder sich zeitlich mit einem Teil eines Impulses des ersten Zuges überlappt, und aufgrund eines dritten Zuges (AKB) einpegeliger Impulse solcher zeitlicher Lage, daß sie mit den periodisch wiederkehrenden Vorspannungsregelintervallen zusammenfallen, wobei der dreipegelige Sandburg-Impulszug den höchsten seiner drei Impulspegel während der Schwarzschnittern und den mittleren seiner drei Impulspegel über das Vorspannungsregelintervall aufweist,

in der integrierten Schaltung ein Spannungsvergleicher (98) ausgebildet ist zum Vergleichen des dreipegeligen Sandburg-Impulszuges mit einer Bezugsspannung (VR), deren Pegel zwischen dem höchsten und dem mittleren der Impulspegel liegt,

in der integrierten Schaltung eine Schaltung (99) ausgebildet ist, die aufgrund eines Ausgangssignals des Spannungsvergleichers die zeilenfrequenten Tastimpulse erzeugt, wenn der Pegel des dreipegeligen Sandburg-Impulszuges die Bezugsspannung übersteigt und

der Dreipegel-Sandburg-Impulscodierer eine Schaltung (101) enthält, die aufgrund der halbbildfrequenten Impulse (VS) einen Pegelanstieg des Dreipegel-Sandburg-Impulszuges auf den höchsten Pegel während mindestens einiger der Zeilenintervalle in deren Aufeinanderfolge verhindert.

6. Empfänger nach Anspruch 5, bei dem Dreipegel-Sandburg-Impulscodierer enthält eine Gleichspannungspotentialquelle ($+V_s$),

einen ersten (92) und einen zweiten (94) Widerstand und einen ersten Transistor (93), dessen Basis der zweite einpegelige Impulszug (BG) zugeführt wird und dessen Emitter-Kollektor-Strecke in Reihe mit dem ersten und dem zweiten Widerstand über die Gleichspannungspotentialquelle geschaltet ist,

wobei der während außerhalb der Vorspannungsregelintervalle liegender Perioden auftretende Pegel des Dreipegel-Sandburg-Impulszuges in Übereinstimmung mit der am Verbindungspunkt des ersten und zweiten Widerstandes auftretenden Spannung bestimmt wird und die den Impulspegelanstieg verhindernde Schaltung einen zweiten Transistor (101) enthält, dessen Basis die halbbildfrequenten Impulse (VS) zugeführt werden und dessen Emitter-Kollektor-Strecke parallel zur Emitter-Kollektor-Strecke des ersten Transistors liegt.

7. Empfänger nach Anspruch 6, bei dem der erste Transistor (93) aufgrund des Auftretens eines Impulses (BG) des zweiten Impulszuges gesperrt wird und der zweite Transistor (101)



während zumindest eines Teils jeder Periode des Auftretens der Vertikalsynchronkomponente in Abhängigkeit von den halbbildfrequenten Impulsen (V_s) leitend gemacht wird.

Revendications

1. Un récepteur de télévision couleur pour visualiser des images en couleur en réponse à des signaux vidéo composés qui sont constitués de composantes respectives de signaux de luminance et de chrominance représentatifs de l'image et des composantes de synchronisation de déviation à fréquence de ligne et à fréquence de trame, les composantes représentant l'image étant absentes pendant une partie de suppression verticale de chaque intervalle de trame et pendant des parties de suppression horizontale d'intervalles de ligne s'étendant hors des parties de suppression verticale, la composante de synchronisation de déviation à fréquence de trame apparaissant pendant une succession d'intervalles de ligne dans chacune des parties de suppression verticale, le récepteur comprenant un canal du signal de luminance pour traiter la composante du signal de luminance, un canal du signal de chrominance pour traiter la composante du signal de chrominance et retrouver de celle-ci des premier et second signaux de différence de couleur, un moyen de combinaison de signaux répondant aux premier et second signaux de différence de couleur et aux composantes de signaux de luminance traités pour former des premier, second et troisième signaux de couleur et un système de stabilisation en courant continu, le système de stabilisation en courant continu étant caractérisé par:

une source (50) d'impulsions de verrouillage à fréquence de ligne;

une première boucle de contrôle (35, 13, 25, 27, 29) pour contrôler le niveau en courant continu du premier signal de couleur formé par le moyen de combinaison de signaux;

une seconde boucle de contrôle (31, 19, 23) pour contrôler le niveau en courant continu du second signal de couleur formé par le moyen de combinaison de signaux; et

une troisième boucle de contrôle (33, 21, 23) pour contrôler le niveau en courant continu du troisième signal de couleur formé par le moyen de combinaison de signaux et en ce que

chacune desdites boucles de contrôle comprend un comparateur de tension verrouillé (31; 33; 35) pour comparer l'un des signaux de couleur respectivement différents à une tension de référence commune (RV) pendant des périodes de verrouillage récurrentes définies par les impulsions de verrouillage à fréquence de ligne produites par ladite source; et

ladite source (50) d'impulsions de verrouillage à fréquence de ligne répond aux impulsions de fréquence de trame indicatives du temps d'apparition de la composante de synchronisation de déviation de fréquence de trame, de manière à empêcher le verrouillage du comparateur de ten-

sion pendant au moins certains des intervalles de ligne de la succession d'intervalles de ligne.

2. Un récepteur selon la revendication 1, où la période des impulsions de verrouillage de fréquence de ligne produites par la source précitée (50) est définie de façon à coïncider avec les segments du palier noir arrière de suppression des parties de suppression horizontale des intervalles de ligne précitées s'étendant hors des parties de suppression verticale.

3. Un récepteur selon la revendication 1 ou 2, où la sortie du comparateur verrouillé (35) de la première boucle de contrôle précitée est utilisée pour ajuster le niveau en courant continu du signal de luminance appliqué au moyen de combinaison de signaux (25, 27, 29) précité, la sortie du comparateur verrouillé (31) de la seconde boucle de contrôle précitée est utilisée pour ajuster le niveau en courant continu du premier signal de différence de couleur précité appliqué au moyen de combinaison de signaux, et la sortie du comparateur verrouillé (33) de la troisième boucle de contrôle précitée est utilisée pour ajuster le niveau en courant continu du second signal de différence de couleur précité appliqué au moyen de combinaison de signaux.

4. Un récepteur selon l'une des revendications 1 à 3, où il comprend un tube-image couleur (77) ayant un certain nombre d'électrodes de contrôle d'intensité (78R, 78B, 78G) pour contrôler l'intensité des faisceaux d'électrons respective d'une pluralité de faisceaux d'électrons traçant une image de ligne de balayage sur un écran de visualisation, chacune des électrodes de commande recevant l'un des signaux de couleur respectivement différents; et un moyen (76) pour contrôler automatiquement les polarisations sur les électrodes de commande respectives pendant des intervalles de contrôle de polarisation périodique englobant un certain nombre d'intervalles de ligne tombant en subséquence à la succession précitée d'intervalles de ligne dans chacune des parties de suppression verticale, les impulsions de verrouillage de fréquence de ligne produites par la source (50) précitée étant soumises à interruption pendant la pluralité d'intervalles de lignes subséquentes.

5. Un récepteur selon la revendication 4, où:

le canal du signal de luminance précité, le canal du signal de chrominance précité et le moyen de combinaison de signaux précités sont réalisés sur un circuit intégré monolithique commun;

la source précitée d'impulsions de verrouillage de fréquence de ligne comprend un codeur d'impulsions en chateau de sable à trois niveaux, extérieur au circuit intégré, pour former un train d'impulsions en chateau de sable à trois niveaux en réponse à un premier train (RB) d'impulsions à un seul niveau englobant des périodes de retour des faisceaux, à un second train (BG) d'impulsions à un seul niveau, chacune des impulsions du second train chevauchant dans le temps une partie d'une impulsion du premier train, et à un troisième train (AKB) d'impulsions à un seul niveau synchronisées pour coïncider avec les



intervalles de contrôle de polarisation périodiquement récurrents, ledit train d'impulsions en chateau de sable à trois niveaux présentant le niveau le plus élevé de ces trois niveaux d'impulsions pendant les segments du palier noir arrière de suppression et présente le niveau médian des trois niveaux d'impulsions tout le long de l'intervalle du contrôle de polarisation,

un comparateur de tensions (98), réalisé sur le circuit intégré, pour comparer le train d'impulsions en chateau de sable à trois niveaux à une tension de référence (VR) d'un niveau intermédiaire au niveau le plus élevé et au niveau médian des niveaux d'impulsions, et

un moyen (99), réalisé sur le circuit intégré et répondant à une sortie du comparateur de tension pour former les impulsions de verrouillage de fréquence de ligne lorsque le niveau du train d'impulsions en chateau de sable à trois niveaux excède la tension de référence; et

un codeur d'impulsions en chateau de sable à trois niveaux comprend un moyen (101) répondant aux impulsions de fréquence de trame (VS) pour empêcher des excursions du train d'impulsions en chateau de sable à trois niveaux au niveau le plus élevé pendant au moins certains des intervalles de ligne dans ladite succession d'intervalles de ligne.

6. Un récepteur selon la revendication 5, où le codeur d'impulsions en chateau de sable à trois niveaux comprend:

une source ($+V_s$) de potentiel en courant continu;

des première (92) et seconde (94) résistances; et un premier transistor (93) ayant une électrode de base reliée pour recevoir le second train précité (BG) d'impulsions à un seul niveau, et un trajet émetteur-collecteur disposé en série avec les première et seconde résistances à travers la source de potentiel en courant continu;

le niveau présenté par le train d'impulsions en chateau de sable à trois niveaux pendant les périodes hors des intervalles de contrôle de polarisation précités est déterminé selon la tension apparaissant à la jonction des première et seconde résistances; et

le moyen empêchant les excursions comprend un second transistor (101) ayant une électrode de base reliée pour recevoir l'impulsion de fréquence de trame (VS), et un trajet émetteur-collecteur relié en shunt avec le trajet émetteur-collecteur du premier transistor.

7. Un récepteur selon la revendication 6, où le premier transistor précité (93) est coupé en réponse à une apparition d'une impulsion (BG) du second train précité, et le second transistor précité (101) est rendu conducteur pendant au moins une partie de chaque période d'apparition de la composante de synchronisation verticale précitée en réponse aux impulsions de fréquence de trame précitées (VS).