

SYNCHRONIZING PULSE SEPARATOR

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This invention relates
to synchronizing circuits for video display apparatus
5 such as for use with standard and non-standard
signal sources.

A video display apparatus, such as a television
receiver, may receive a composite video signal that
contains audio and video information, as well as line and
10 field rate synchronizing information. The synchronizing
information is used to properly trigger the horizontal and
vertical deflection circuits that cause scanning of the
electron beam or beams of a cathode ray tube in order to
produce the desired raster on the cathode ray tube display
15 screen. The synchronizing (sync) information is extracted
from the composite video signal by a sync separator
circuit. The sync separator circuit operates by sampling
the composite video signal at a voltage level normally
occupied only by the synchronizing information. Further
20 processing separates the horizontal rate and vertical rate
sync signals for application to their respective
deflection circuitry.

The sync separator in a television receiver is
typically designed to respond to a video information
25 signal from a "standard" signal source, such as an
over-the-air broadcast or a cable TV signal, that is
intended to produce scanned rasters having alternating
fields of line-interlaced video information. The
synchronizing information is configured to trigger the
30 deflection circuits in an appropriate manner to produce
the proper interlace of the lines of successive video
fields. When the video display apparatus operates as a
computer monitor or is intended to produce a video game
display, for example, the video signal from these
35 "non-standard" signal sources may be of a form that
provides noninterlaced fields of information. The sync
information generated by a nonstandard signal source may
cause the sync separator to operate improperly, with the
resultant occurrence of an undesirable visible effect,

comprises: a charging path for said capacitor including a diode and a first resistor connected in series between said source of potential and said second terminal of said transistor to which said capacitor is connected; and a
5 discharging path for said capacitor separate from said charging path and including a second resistor connected between said second terminal of said transistor to which said capacitor is connected and a point of reference potential.

10 An embodiment of the present invention, given by way of non-limitative example, will now be described with reference to the accompanying drawings, in which FIGURE 1 is a block and schematic diagram of a portion of a video display apparatus incorporating a sync separator embodying
15 the present invention; and

FIGURE 2 illustrates waveforms useful in understanding the operation of the circuitry of FIGURE 1.

Referring to FIGURE 1, there is shown a portion of a video display apparatus incorporating a tuner 10 that
20 illustratively receives an input signal from either an antenna 11 or an alternate signal source 12, such as a computer or a video game. The signal from antenna 11 or signal source 12 is applied to tuner 10 via a user accessible input terminal strip 13. Tuner 10 demodulates the
25 input signal and applies the resultant signal to intermediate frequency (IF) processing circuitry 14 which

- 1 portion of the video signal exceeding the V_{SAT} voltage level, designated 69 in FIGURE 2A. Noise signal components 29 present in the composite video signal are of insufficient amplitude to render transistor 27
- 5 conductive. As can be seen by the capacitor 26 voltage waveform 34 of FIGURE 2A, capacitor 26 charges during the presence of the sync pulses, such as horizontal sync pulses 35 or vertical sync pulse 38, for example, and discharges via resistor 28 between sync pulses when
- 10 transistor 27 is nonconductive, so that the average voltage across capacitor 26 has a level designated V_{AVE} .

- The output signal at collector terminal 33 of transistor 27, shown in FIGURE 2B, is applied to differentiator circuit 40 and integrator circuit 41, as
- 15 shown in FIGURE 1. Differentiator circuit 40, comprising capacitor 42 and resistor 43, produces horizontal or line rate sync pulses, as shown in FIGURE 2C, which are applied to horizontal deflection circuit 44 in order to trigger the operation of horizontal deflection circuit 44.
- 20 Horizontal deflection circuit 44, which receives power from a source of voltage $+V_2$, produces horizontal deflection current, via terminals H and H', in a horizontal deflection winding 45, located on the neck of CRT 21. Horizontal deflection circuit 44, which may be of
- 25 a conventional resonant retrace type, produces horizontal rate flyback or retrace pulses that are used to derive the high voltage or ultor potential $+HV$ for CRT 21.

- Integrator circuit 41, comprising resistor 46 and capacitor 47, integrates the output pulses of transistor
- 30 27 to form a vertical sync pulse signal as shown in FIGURE 2D, which is applied to vertical deflection circuit 50. Vertical deflection circuit 50 is designed to be triggered by the sync pulse signal shown in FIGURE 2D when it reaches a voltage level designated 52, which corresponds
- 35 to a time t_1 in FIGURE 2D. Vertical deflection circuit 50, which receives power from a source of voltage $+V_3$, generates vertical deflection current, via terminals V and V', in a vertical deflection winding 51, also located on the neck of CRT 21. The sync signals from differentiator

- 1 the time of triggering results in a visible vertical
jitter of the display video information on display screen
24 of CRT 21.

An aspect of the present invention is embodied in
5 a compensation circuit 57 which is coupled between
the $+V_1$ supply and the base terminal 30 of transistor
27. Compensation circuit 57 comprises the series
combination of a diode 60 and a resistor 61 with diode 60
poled such that its anode terminal is coupled to the $+V_1$
10 supply. Compensation circuit 57 clamps the base bias
voltage of transistor 27 to a level approximating that
established by the presence of a composite video signal
incorporating equalizing pulses. During the time
transistor 27 is nonconductive, current flow through diode
15 60 and resistor 61 acts to provide charging current to
capacitor 26 with the result that the average voltage
across capacitor 26 remains substantially constant. The
bias voltage on the base of transistor 27 remains at a
level sufficient to prevent noise signal components in the
20 video signal from rendering transistor 27 conductive.
When transistor 27 is rendered conductive by the
occurrence of a sync pulse, the current conducted by
transistor 27 is much greater than the current conducted
by compensation circuit 57 in order to prevent
25 interference of compensation circuit 57 with the operation
of the sync separator. Diode 60 may be replaced by a
transistor connected in a diode configuration, or by the
series combination of two diodes, either of the same type
or with one diode being a schottky diode, for example,
30 while maintaining the desirable operation of compensation
circuit 57. The voltage drop across diode 60 or its
equivalent is selected to be slightly less than the
base-emitter voltage of transistor 27 in order to allow
diode 60 to conduct.

- 35 The sync separator of the present embodiment,
therefore, provides jitter-free, noise immune operation
for video signals that do not include equalizing pulses
without degrading the sync separator operation when
equalizing pulses are present in the video signal.

a discharging path for said capacitor separate from said charging path and including a second resistor connected between said second terminal of said transistor to which said capacitor is connected and a point of reference potential.

2. A synchronizing pulse separator for a video display apparatus as recited in Claim 1 wherein said capacitor and said one end of said charging path are connected to said second terminal of said transistor without intervening elements.

3. A synchronizing pulse separator for a video display apparatus substantially as herein described with reference to the accompanying drawings.
