CLAIMS

1. A computer system comprising:

a first partition and a second partition;

the first partition comprising:

a first CPU,

a first memory module comprising:

at least one memory address range for program code, wherein the program code comprises computer-executable code, and wherein the memory address range for program code is hardware-protected from alteration by a hardware switch;

at least one memory address range for first partition data; and

at least one memory address range for data read from the second partition; and

wherein the first CPU is hardware-configured to execute only the computer-executable code in the memory address range for program code; and

the second partition comprising:

a second CPU,

a second memory module, and

at least one communication module configured to couple to a network; and

wherein the first CPU is configured to access the second memory module;

wherein the first CPU is configured to read data from the second partition into only the at least one memory address range for data read from the second partition; and

wherein the second CPU is restricted from accessing the first CPU or the first memory module.

2. The computer system of claim 1, wherein the at least one memory address range for program code is configured by hardware circuitry.

3. The computer system of claim 2, wherein the hardware circuitry comprises at least one field-programmable gate array.

4. The computer system of claim 1, wherein the first memory module comprises:

a first memory unit comprising the at least one memory address range for program code;

a second memory unit comprising the at least one memory address range for first partition data; and

a third memory unit comprising the at least one memory address range for data read from the second partition.

5. The computer system of claim 1, wherein the program code comprises an operating system.

6. The computer system of claim 1, comprising at least one data store.

7. The computer system of claim 1,

wherein the ability of the first CPU to access the second memory module is implemented by hardware circuitry; and

wherein the restriction on the second partition from accessing the first CPU or the first memory module is implemented by hardware circuitry.

8. The computer system of claim 1, wherein a hardware feature, utilizing an external device connected directly to the first partition, is configured to enable a user to command the first CPU to take control of an input/output device of the second partition.

9. The computer system of claim 1, further comprising:

a bus,

wherein the first partition is interconnected to the second partition through the bus;

wherein the first CPU is configured to execute a pull command through the bus to read the data from the second partition and write the data only to the at least one memory address range for data read from the second partition;

wherein the first CPU is configured to execute a push command through the bus to write data to the second partition;

wherein the first partition cannot accept a push command from the second partition or a pull command from the second partition; and

wherein the restriction on the second partition from accessing the first CPU or the first memory module is implemented by hardware circuitry.

10. The computer system of claim 1, wherein the hardware switch comprises at least one external physical switch which is configured to be turned on or off, wherein the first CPU can modify data stored in the at least one memory address range for program code only when the external physical switch is on.

11. The computer system of claim 1, comprising:
at least one external physical switch which is configured to be turned on or off;
wherein the first CPU is configured to modify contents of the at least one memory address range for program code only when the external physical switch is on.

12. The computer system of claim 1, wherein:
the ability of the first CPU to access the second memory module is implemented in a virtual partition configuration; and
the restriction on the second CPU from accessing the first CPU or the first memory module is implemented in a virtual partition configuration.

13. The computer system of claim 1,
wherein the first partition comprises at least one input/output module; and
wherein a plurality of input/output devices are coupled to at least one input/output module.

14. The computer system of claim 1, further comprising a chip comprising the first partition and the second partition.

15. The computer system of claim 1, further comprising a first chip comprising the first partition and a second chip comprising the second partition.

16. The computer system of claim 1, wherein a hardware feature, utilizing an external device connected directly to the first partition, is configured to enable the first CPU to write data to the

second partition from the at least one memory address range for program code, the at least one memory address range for first partition data, or the at least one memory address range for data read from the second partition.

17. A computer system comprising:

a first partition comprising:

a first CPU; and

a first memory module comprising:

a first memory address range, wherein the first memory address range comprises program code, wherein the program code comprises computer-executable code, and wherein the program code is hardware-protected from alteration by a hardware switch; and

a second memory address range;

wherein the first CPU is hardware-configured to execute only the computer-executable code in the first memory address range; and

a second partition comprising:

a second CPU;

a second memory module; and

at least one communication module configured to couple to a network; and

wherein the first CPU is configured to access the second memory module;

wherein the first CPU is configured to read data from the second partition into only the second memory address range; and

wherein the second CPU is restricted from accessing the first CPU or the first memory module.

18. The computer system of claim 17, wherein the first memory address range is configured by hardware circuitry.

19. The computer system of claim 18, wherein the hardware circuitry comprises at least one field-programmable gate array.

20. The computer system of claim 17, wherein the first memory module comprises:

a first memory unit comprising the first memory address range; and
a second memory unit comprising the second memory address range.

21. The computer system of claim 17, wherein the program code comprises an operating system.

22. The computer system of claim 17, comprising at least one data store.

23. The computer system of claim 17,
wherein the ability of the first CPU to access the second memory module is implemented by hardware circuitry; and
wherein the restriction on the second partition from accessing the first CPU or the first memory module is implemented by hardware circuitry.

24. The computer system of claim 17, wherein a hardware feature, utilizing an external device connected directly to the first partition, is configured to enable a user to command the first CPU to take control of an input/output device of the second partition.

25. The computer system of claim 17, further comprising:
a bus,
wherein the first partition is interconnected to the second partition through the bus;
wherein the first CPU is configured to execute a pull command through the bus to read the data from the second partition and write the data only to the second memory address range;
wherein the first CPU is configured to execute a push command through the bus to write data to the second partition;
wherein the first partition cannot accept a push command from the second partition or a pull command from the second partition; and
wherein the restriction on the second partition from accessing the first CPU or the first memory module is implemented by hardware circuitry.

26. The computer system of claim 17, wherein the hardware switch comprises at least one external physical switch which is configured to be turned on or off, wherein the first CPU is configured to modify data stored in the first memory address range only when the external physical switch is on.

27. The computer system of claim 17, comprising:
at least one external physical switch which is configured to be turned on or off;
wherein the first CPU is configured to modify contents of the first memory address range only when the external physical switch is on.

28. The computer system of claim 17, wherein:
the ability of the first CPU to access the second memory module is implemented in a virtual partition configuration; and
the restriction on the second CPU from accessing the first CPU or the first memory module is implemented in a virtual partition configuration.

29. The computer system of claim 17,
wherein the first partition comprises at least one input/output module; and
wherein a plurality of input/output devices are coupled to at least one input/output module.

30. The computer system of claim 17, further comprising a chip comprising the first partition and the second partition.

31. The computer system of claim 17, further comprising a first chip comprising the first partition and a second chip comprising the second partition.

32. The computer system of claim 17, wherein a hardware feature, utilizing an external device connected directly to the first partition, is configured to enable the first CPU to write data to the second partition from the first memory module.

33. A computer system comprising:

a first partition and a second partition;

the first partition comprising:

a first CPU; and

a first memory module comprising:

at least one memory address range for program code, wherein the program code comprises computer-executable code, and wherein the at least one memory address range for program code is configured by hardware circuitry; and

at least one memory address range for other data, wherein the other data comprises data read from the second partition;

wherein the first CPU is hardware-configured to execute only the computer-executable code in the memory address range for program code; and

the second partition comprising:

a second CPU;

a second memory module; and

at least one communication module configured to couple to a network;

wherein the first CPU is configured to access the second memory module and read data from the second partition into only the at least one memory address range for other data; and

wherein the second CPU is restricted from accessing the first memory module; wherein

the computer system ~~of claim 37,~~ comprising at least one external physical switch configured to be turned on or off, wherein the first CPU is configured to modify data stored in the at least one memory address range for program code only when the external physical switch is on.

34. A computer system comprising:

at least one CPU,

at least one I/O module connecting to at least one other computer, and

at least one memory module, comprising:

at least one memory address range for program code, configured by hardware circuitry, wherein the program code comprises computer-executable code;

at least one memory address range for other data, wherein the other data comprises data read from the at least one other computer;

wherein the at least one CPU is hardware-configured to execute only the computer-executable code in the memory address range for program code;

wherein data read from the at least one other computer can be written only into the at least one memory address range for other data;

wherein the at least one other computer is hardware-limited from directly communicating with the at least one CPU.

35. The computer system of claim 34, wherein the at least one memory module comprises:

a first memory unit for the at least one memory address range for program code; and

a second memory unit for the at least one memory address range for other data.

36. The computer system of claim 34, comprising at least one external physical switch which can be turned on or off, wherein the first CPU can modify data stored in the at least one memory address range for program code only when the external physical switch is on.

37. The computer system of claim 34, further comprising:

a bus,

wherein the computer system is communicatively coupled to the at least one other computer through the bus;

wherein the computer system is configured to execute a pull command through the bus to read the data from the at least one other computer and write the data only to the at least one memory address range for other data;

wherein the computer system is configured to execute a push command through the bus to write data to the at least one other computer;

wherein the computer system is configured not to accept a push command from the at least one other computer or a pull command from the at least one other computer; and

wherein the at least one other computer is hardware-limited from directly communicating with the at least one CPU.