

Description

BACKGROUND OF THE INVENTION

The present invention relates to a paging receiver having a battery saving circuit and, more particularly, to the sync monitoring of such a receiver and the control of the battery saving circuit.

Paging signals elaborated to call paging receivers include POCSAG (Post Office Code Standardisation Advisory Group) code as proposed by British Post Office. POCSAG code consists of a preamble signal and a required number of batches which follow the preamble signal. One batch is made up of a single synchronization codeword (SC) and eight frames each consisting of two codewords and adapted for the transmission of an address codeword or a message codeword. Paging receivers are divided into eight groups so that a receiver belonging to any of the eight groups receives and processes only an address codeword of a predetermined frame in each of the batches. For example, a paging receiver which belongs to the second group does not receive and process address codewords except for a one which is contained in the second frames.

Usually, a paging receiver includes a sync monitoring circuit and a battery saving circuit. The sync monitoring circuit in turn includes SC detecting means and means for controlling a battery saving circuit. The sync monitoring circuit monitors SCs in consecutive batches and, when it does not receive an SC in N (e.g. N=2) consecutive batches, determines that a paging signal has ceased and restores the battery saving circuit to a battery saving mode. In a battery saving mode, the receiver enables a receiving circuit and others intermittently so that a preamble signal may be received.

A problem with the prior art sync monitoring circuit as described above is that it has to monitor not only an address codeword in each batch which is assigned to the own group but also an SC. Specifically, while a paging signal is received, the operation time of the receiving circuit and others is prolonged by a fraction which is equal to an SC receiving time, resulting in a low battery saving efficiency. Another problem is that because the sync monitoring circuit decides that a paging signal has ceased when the SC has failed to be detected a plurality of times, SCs in a following one of a plurality of paging signals which may be transmitted continuously cannot be detected.

GB-A-2 136 179 describes a pager decoding system which is suitable for use with signal formats in which code words are sent in batches, each batch containing a synchronization code word and (n-1) address/message code words, n being the

number of code words in a batch, each code word comprising m bits. The pager is able to detect or regain a synchronization code word when the carrier signal is lost due to fading. After bit and batch synchronization are established, the receiver section of the paging receiver is energized at the synchronization code word interval and the allocated frame interval in each batch. Thus, this known receiver consumes power during two time intervals in each batch.

US-A-3 851 251 relates to a paging receiver comprising a receiving section, a timing recovery circuit and a synchronization and decode logic circuit. Said synchronization and decode logic circuit comprises, among other things, an address evaluator which evaluates differences between locally generated address signals ADS 1 and ADS 2 and the incoming data signal DDATA. If the number of the detected differences is less than a predetermined number, the evaluator provides an address-accept signal. This evaluator detects only the differences but not errors in the incoming data signal DDATA.

It is therefore an object of the present invention to provide a paging receiver which is operable with an improved battery saving efficiency during reception of a paging signal and a method of saving a battery of a paging receiver.

It is another object of the present invention to provide a paging receiver and a method which, when paging signals are transmitted continuously, is capable of receiving a following address codeword accurately.

The above objects are achieved by a paging receiver having the features of claim 1 and a method having the features of claim 4, resp.

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description taken with the accompanying drawings in which:

Fig. 1 is a block diagram showing a paging receiver in accordance with the present invention;

Fig. 2 is a format representative of POCSAG code;

Figs. 3A. to 3D and 4A to 4D are timing charts demonstrating a prior art sync monitoring and a battery saving operations;

Fig. 5 is a block diagram showing an essential part of the receiver as shown in Fig. 1;

Figs. 6A to 6J are timing charts demonstrating the operation of the circuit of Fig. 5;

Fig. 7 is a block diagram showing a specific construction of a BCH code detector in accordance with the present invention;

Fig. 8 is a block diagram of an error detector as shown in Fig. 7;

Fig. 9 is a chart showing an input-output characteristic of a logic circuit which is included in the error detector of Fig. 8;

Figs. 10A to 10J are timing charts representative of the operation of the Fig. 8 circuit;

Fig. 11 is a block diagram of a sync monitor as shown in Fig. 7;

Figs. 12A to 12D are timing charts demonstrating the operation of the Fig. 11 circuit;

Fig. 13 is a block diagram showing another specific construction of the BCH code detector in accordance with the present invention; and

Figs. 14A to 14H are timing charts showing the operation of the Fig. 13 circuit.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Referring to Fig. 1, a paging signal picked up by an antenna 11 is fed to a radio section 12 which forms a part of a receiving section. The radio section 12 amplifies the received signal, converts its frequency, and demodulates it to produce a baseband signal. The demodulated signal is converted by a wave-form shaper 13 into a rectangular wave which is then applied to a decoder and controller 14. The decoder and controller 14 is adapted to decide whether the received signal contains an address codeword which is directed to the receiver. If the received signal contains the desired address codeword, the decoder and controller 14 energizes a speaker or like annunciator 17 to alert the bearer of the receiver to the paging. A crystal oscillator 15 functions to supply the decoder and controller 14 with a reference clock.

The decoder and controller 14 and the annunciator 17 are powered by a battery 18 continuously, while the radio section 12 and wave-form shaper 13 are powered via a power supply (PS) control switch 16 which is controlled by the decoder and controller 14. In a waiting mode, the PS control switch 16 is closed intermittently so as to power the radio section 12 and wave-form shaper 13. While the switch 16 is closed, the decoder and controller 14 searches for a preamble signal.

When the detector and controller 14 has detected a preamble signal, the PS control switch 16 is closed continuously to in turn maintain the radio section 12 and wave-form shaper 13 in an operative condition. Then, upon detection of a synchronization codeword (SC), the switch 16 is closed only for the duration of a particular frame of one batch to which the receiver belongs. During this period of time, the decoder and controller 14 detects a BCH (Bose-Chaudhuri-Hocquenghem) code, which constitutes a codeword, and a preamble signal as well as an address codeword. In this manner, the receiver in accordance with the present

invention allows only the radio section 12 and wave-form shaper 13 to be turned on only for the duration of two codewords of the own frame while an address codeword is searched for. The receiver, therefore, achieves a higher battery saving efficiency than a prior art receiver which should be turned on not only for the duration of two codewords of the own frame but also for the duration of an SC. In addition, the receiver of the present invention is so constructed as to detect a preamble signal in parallel with an address codeword, so that it does not fail to receive paging signals which may be transmitted continuously.

To better understand the present invention, POCSAG code and prior art sync monitoring and battery saving functions will now be described. As shown in Fig. 2, POCSAG code begins with a preamble signal and includes a required number of batches which follow the preamble signal. Usually, a preamble signal is implemented with a repetitive pattern of "1" and "0". One batch consists of an SC which comprises a single codeword, and eight frames each comprising two codewords.

Referring to Figs. 3A to 3D, a prior art paging receiver which is waiting for a paging signal, or in a waiting mode, searches for a preamble signal by turning on the radio section 12 and wave-form shaper 13 intermittently. Upon detection of a preamble signal, the receiver turns on the radio section 12 and wave-form shaper 13 continuously in order to search for an SC. This is the sync build mode as shown in Fig. 3D. When an SC is detected, the radio section 12 and waveform shaper 13 are enabled for the duration of the SC of each batch of the paging signal and the duration of each frame to which the receiver belongs (second frames F2 in this example), whereby an SC monitoring operation (Fig. 3C) and an address codeword detecting operation are performed. The address codeword detecting operation is represented by an address receiving mode in Fig. 3. If an SC is not received two consecutive times, the receiver returns to the waiting mode.

The on-off control of the radio section 12 and wave-form shaper 13 as shown in Fig. 3B is representative of the so-called battery saving control. While the prior art receiver is turned on for the duration of three codewords in total, i.e., one codeword which constitutes an SC and two codewords which constitute one frame, the receiver of the present invention is turned only for the duration of two codewords, or one frame, enhancing the battery saving efficiency.

Referring to Figs. 4A to 4D, when paging signals I and II are transmitted one after another, the prior art receiver fails to receive the following paging signal II since it does not return to the waiting mode except when an SC has not been detected

two consecutive times. In contrast, the receiver of the present invention safely receives the paging signal II since a preamble signal is detected in parallel even in the address receiving mode.

Referring to Fig. 5, a specific construction of an essential part of the decoder and controller 14 in accordance with the present invention is shown. The operation of the circuit shown in Fig. 5 will be described with reference to the timing charts of Figs. 6A to 6J. In Fig. 5, the decoder and controller 14 includes a bit sync circuit 31 to which the reference clock (e.g. 32 kHz) from the crystal oscillator 13 (Fig. 1) is coupled. The bit sync circuit 31 feeds a recovered clock CLK to various sections of the receiver by timing the reference clock to the output signal DATA of the wave-form shaper 13 (Fig. 1). A battery saving (BS) controller 36, in a waiting mode, delivers a power supply control signal PSC and a control signal b to the receiving section (the radio section 12 and wave-form shaper 13) and a preamble detector 32, respectively, for enabling them intermittently to search for a preamble, as shown in Figs. 6B and 6C.

In response to the detection of a preamble signal during the waiting mode, the preamble detector 32 delivers a preamble detect signal PD to the BS controller 36. As shown in Figs. 6D, 6A and 6E, the BS controller 36 applies to the receiving section and an SC detector 33, respectively, the PSC signal and a control signal c for a predetermined period of time (e.g. a length of seventeen words at maximum) for detecting an SC. In this SC search mode, when the SC detector 33 has detected an SC, it sends an SC detect pulse SCD to the BS controller 36. In response, the BS controller 36 delivers to the receiving section, the preamble detector 32, an address detector 34 and a BCH code detector 35, respectively, the PSC signal, the control signal b, a control signal d and a monitor enable signal ENA, as shown in Figs. 6B, 6C, 6G and 6I. The BS controller 36 then enters into an address receiving mode. As shown in Figs. 6B, 6C, 6G and 6I, during this mode, the PCS signal and control signals b, d and ENA are each being fed only for the duration of the second frame F2 to which the receiver belongs.

As shown in Fig. 6H, when the address detector 34 has detected an address signal addressed to the receiver in the address receiving mode, it generates a detect pulse IDD. An alert generator 37 responds to the pulse IDD by applying an alert signal ALT to the annunciator 17 (Fig. 1), whereby the annunciator 17 produces an alert tone.

In the address receiving mode, when the BCH code detector 35 has not detected a BCH code in two consecutive batches, it produces a mode cancel pulse NBD, as shown in Fig. 6J. In response to the pulse NBD, the BS controller 36 generates a

PSC signal and a control signal b in order to restore the receiver to the waiting mode.

Meanwhile, assume that the BCH code detector 35 has not detected a BCH code in, for example, two consecutive batches. Even in this situation, when the preamble detector 32 has detected a preamble signal, the BS controller 36 delivers a PSC signal and a control signal c so as to restore the receiver to the SC search mode. This allows the receiver to receive the signal II which follows the signal I as shown in Fig. 4A, without fail.

Referring to Fig. 7, a specific construction of the BCH code detector 35 is shown in a block diagram. As shown, the detector 35 is made up of an error detector 101 and a sync monitor 102. The error detector 101 receives a codeword of a predetermined frame and a recovered clock signal CLK while receiving switch control signals x1 to x6 from the sync monitor 102. When the error detector 101 has detected any error in the received codeword, it produces an error detect signal ERR. The sync monitor 102, on the other hand, receives the error detect signal ERR, sync monitor enable signal ENA and clock signal CLK. When the number of signals ERR applied to the sync monitor 102 has exceeded a predetermined one, e.g., when a predetermined number of errors have been detected in two consecutive batches, the sync monitor 102 delivers a control signal NBD indicating that synchronization has failed or a paging signal has ceased. As previously stated, the control signal NBD causes the BS controller 36 (Fig. 5) to enter into a waiting mode.

Referring to Fig. 8, a specific construction of the error detector 101 of Fig. 7 is shown in a block diagram. As shown, the detector 101 is made up of 1-clock delay circuits 201 to 211, an AND gate 212, a NOR gate 213, switches 214 to 219, Exclusive-OR (EXOR) gates 220 to 226, and a logic circuit 227. The logic circuit 227 is so constructed as to have an input-output characteristic as shown in Fig. 9. An output signal E₀ of the logic circuit 227 is representative of the number of errors.

The operation of the error detector 101 will be described with reference also to the timing chart of Fig. 10. In Fig. 10, an address codeword included in a paging signal DATA has been converted into an error correcting and detecting code by extended BCH code $(n, k; d) = (32, 21; 6)$ where n denotes a code length, k the number of data bits, and d a minimum Hamming distance.

Extended BCH (32, 21; 6) code consists of BCH (31, 21; 5) and a parity bit. Because the minimum Hamming distance d is 6, the extended BCH code has a capability of correcting one error and detecting four errors, and this capability is utilized by the error detector 101 (Fig. 8) of this particular embodiment. The 1-clock delays 201 to

205 and EXOR gates 220 and 221 shown in Fig. 8 constitute a circuit for computing a syndrome of BCH (31, 21; 5), and so do the 1-clock delays 206 to 210 and EXOR gates 222 to 225. The output signals E_0 and E_1 of the logic circuit 227 are respectively representative of the error bit number ($e = 0, 1$) of BCH(31, 21; 5) and that the error has been detected.

As shown in Fig. 10J, when two or more bits of error have been detected, a detect code ERR is produced at the end of one address codeword.

Referring to Fig. 11, a specific construction of the sync monitor 102 of Fig. 7 is shown. The monitor 102 is comprised of a timing generator 301 and an error counter 302. In response to the clock CLK and enable signal ENA, the timing generator 301 produces signals x_1 to x_6 which are adapted to control switches 214 to 217 (see Fig. 8) installed in the error detector 101 at those timings which are shown in Figs. 10D to 10I. In this construction, the error detector 101 (Fig. 7) is caused to perform an error detection only on predetermined frames of the paging signal DATA. As shown in Fig. 12, when the error signal ERR has been detected four times in two consecutive batches, i.e., when it has been detected twice in one batch and continued over two batches on the same frame, the error counter 302 determines that the paging signal has ceased and applies a control signal NBD to the BS controller 36 to thereby bring it into a waiting mode.

In the construction and operation as described above, if the SC of the leading batch is detected, sync monitoring can be accomplished without receiving the SCs of the subsequent batches.

Referring to Fig. 13, another specific construction of the error detector 101 is shown. The detector 101 is made up of a sample and hold circuit 601, threshold circuits 602 and 605, a full-wave rectifier 603, and an integrating circuit 604. It is to be noted that a paging signal DATA' as shown in Fig. 13 comprises an analog signal which contains receiver noise, i.e., a signal which has not been propagated through the wave-form shaper 13 as shown in Fig. 1.

The operation of the error detector of Fig. 13 will be described with reference to the timing chart of Fig. 14. The paging signal DATA' is sampled by the sample and hold circuit 601 timed to every clock pulse, an output of the circuit 601 being represented by r_1 in Fig. 14D. The signal r_1 is subjected to data decision at the threshold circuit 602 to become a signal r_2 , as shown in Fig. 14E. Here, the threshold circuit 602 is set such that if the signal DATA' is free from noise, the signal r_1 and r_2 are of the same level. Hence, a signal r_3 (Fig. 14F) representative of a differential between the signals r_1 and r_2 is an error signal which shows the magnitude of receiver noise so long as no

decision error occurs. The error signal r_3 is rectified and integrated by the full-wave rectifier 603 and the integrating circuit 604 to become a signal r_4 , as shown in Fig. 14G.

Because the integrating circuit 604 is discharged frame by frame, the signal r_4 indicates an integrated value of the magnitude of the error signal r_3 which occurred in one frame. As the integrated value increases beyond a predetermined one, the threshold circuit 605 produces an error detect signal ERR (Fig. 14H).

In summary, it will be seen that the present invention provides a paging receiver which detects errors in a paging signal to accomplish sync monitoring without resorting to receiving every SC in consecutive batches.

Further, in the receiver of the present invention, errors in a paging signal and a preamble are detected so that not only sync monitoring is accomplished but also the subsequent paging signal can be monitored. It follows that, in the exemplary paging signal format of Fig. 2, the operation time of the receiving circuit is reduced, except for the leading batch, to 2/3 of the operation time heretofore available, increasing the battery saving efficiency.

In addition, in some applications wherein a signal can be received always a preamble first, it is possible to enhance the data transmission efficiency by causing an SC to be transmitted by the leading one batch only.

Claims

1. A paging receiver comprising:

a receiving section (12, 13) for receiving a paging signal including a preamble signal and batches which follow said preamble signal and each of which begins with a synchronization codeword and contains a plurality of frames, said receiver belonging to one of said frames, address codewords being included in said frames;

switch means (16) for controlling power supply to said receiving section in response to a control signal;

means (32) for detecting a preamble signal to produce a preamble detect pulse;

means (33) for detecting a first synchronization codeword which is present immediately after said preamble signal to produce a synchronization codeword detect pulse; and

means (34) for detecting an address codeword assigned to said receiver to produce an address codeword detect pulse,

CHARACTERIZED BY

error detector means (35) for detecting an error in said frames and producing an error



205 and EXOR gates 220 and 221 shown in Fig. 8 constitute a circuit for computing a syndrome of BCH (31, 21; 5), and so do the 1-clock delays 206 to 210 and EXOR gates 222 to 225. The output signals E_0 and E_1 of the logic circuit 227 are respectively representative of the error bit number ($e = 0, 1$) of BCH(31, 21; 5) and that the error has been detected.

As shown in Fig. 10J, when two or more bits of error have been detected, a detect code ERR is produced at the end of one address codeword.

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In the construction and operation as described above, if the SC of the leading batch is detected, sync monitoring can be accomplished without receiving the SCs of the subsequent batches.

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decision error occurs. The error signal r_3 is rectified and integrated by the full-wave rectifier 603 and the integrating circuit 604 to become a signal r_4 , as shown in Fig. 14G.

Because the integrating circuit 604 is discharged frame by frame, the signal r_4 indicates an integrated value of the magnitude of the error signal r_3 which occurred in one frame. As the integrated value increases beyond a predetermined one, the threshold circuit 605 produces an error detect signal ERR (Fig. 14H).

In summary, it will be seen that the present invention provides a paging receiver which detects errors in a paging signal to accomplish sync monitoring without resorting to receiving every SC in consecutive batches.

Further, in the receiver of the present invention, errors in a paging signal and a preamble are detected so that not only sync monitoring is accomplished but also the subsequent paging signal can be monitored. It follows that, in the exemplary paging signal format of Fig. 2, the operation time of the receiving circuit is reduced, except for the leading batch, to 2/3 of the operation time heretofore available, increasing the battery saving efficiency.

In addition, in some applications wherein a signal can be received always a preamble first, it is possible to enhance the data transmission efficiency by causing an SC to be transmitted by the leading one batch only.

Claims

1. A paging receiver comprising:

a receiving section (12, 13) for receiving a paging signal including a preamble signal and batches which follow said preamble signal and each of which begins with a synchronization codeword and contains a plurality of frames, said receiver belonging to one of said frames, address codewords being included in said frames;

switch means (16) for controlling power supply to said receiving section in response to a control signal;

means (32) for detecting a preamble signal to produce a preamble detect pulse;

means (33) for detecting a first synchronization codeword which is present immediately after said preamble signal to produce a synchronization codeword detect pulse; and

means (34) for detecting an address codeword assigned to said receiver to produce an address codeword detect pulse,

CHARACTERIZED BY

error detector means (35) for detecting an error in said frames and producing an error



detect pulse when the number of errors detected is greater than a predetermined value; and

controller means (36) for, in a waiting mode, generating said control signal intermittently at a predetermined interval, generating said control signal continuously for a predetermined period of time when receiving said preamble detect pulse during the intermittent generation of said control signal, generating said control signal only at a particular frame in each batch to which frame said receiver belongs after receiving said synchronization codeword detect pulse during the continuous generation of said control signal, generating said control signal at said predetermined interval when receiving said error detect pulse during the generation of said control signal at said particular frame, and applying the generated control signal to said switch means (16).

2. A paging receiver as claimed in claim 1, wherein said controller (36) generates said control signal continuously for the predetermined period of time when receiving said preamble detect signal during the generation of said control signal at said predetermined timing, and applies the generated control signal to said switch means (16).

3. A paging receiver as claimed in claims 1 or 2, further comprising means (37) for generating an alert signal in response to said address codeword detect pulse.

4. A method of saving a battery of a paging receiver, comprising the steps of:

supplying power to a predetermined section (12, 13) of said receiver in response to a control signal;

generating said control signal intermittently while said receiver is waiting for a paging signal including a preamble signal and batches which follow said preamble signal and each of which begins with a synchronization codeword and contains a plurality of frames, said receiver belonging to one of said frames, address codewords being to be included in said frames; and

detecting a first synchronization codeword which is present immediately after said preamble signal to produce a sync detect signal, CHARACTERIZED BY the steps of:

responsive to said sync detect signal, generating said control signal only at a particular frame in each batch to which frame said receiver belongs; and

detecting an error in codewords which are

contained in said paging signal while said control signal is generated at said particular frame, and, when the number of the detected errors is greater than a predetermined value, replacing the generation of said control signal at said particular frame with the intermittent generation.

5. A method as claimed in claim 4, further comprising the steps of:

generating said control signal continuously for a predetermined duration when a preamble signal in said paging signal is detected;

detecting said first synchronization codeword while said control signal is generated continuously for said predetermined duration; and

generating said control signal continuously during said predetermined duration when said preamble signal is detected while said control signal is generated at said particular frame.

Patentansprüche

1. Personenrufempfänger, der aufweist:
ein Empfangsteil (12, 13) für den Empfang eines Personenrufssignals mit einem Einleitungssignal und Datenblöcke, die dem Einleitungssignal folgen und von denen jeder mit einem Synchronisationskodewort beginnt und mehrere Rahmen enthält, wobei der Empfänger zu einem der Rahmen gehört und Adreßkodewörter in diesen Rahmen enthalten sind;

eine Schaltereinrichtung (16) zur Steuerung der Stromversorgung für das Empfangsteil in Reaktion auf ein Steuersignal;

eine Einrichtung (32) zur Feststellung eines Einleitungssignals, um ein Einleitungsfeststellungsimpuls zu erzeugen;

eine Einrichtung (33) zur Feststellung eines ersten Synchronisationskodewortes, welches unmittelbar nach dem Einleitungssignal vorliegt, um ein Synchronisationskodewort-Feststellungsimpuls zu erzeugen; und

eine Einrichtung (34) zur Feststellung eines Adreßkodewortes, welches dem Empfänger zugeordnet ist, um ein Adreßkodewort-Feststellungsimpuls zu erzeugen,

gekennzeichnet durch

eine Fehlerfeststelleinrichtung (35), um Fehler in den Rahmen festzustellen und einen Fehlerfeststellungsimpuls zu erzeugen, wenn die Zahl der festgestellten Fehler größer als ein vorbestimmter Wert ist; und

eine Einstellereinrichtung (36), um in einem Wartemode das Steuersignal intermittierend in einem vorbestimmten Intervall zu erzeugen, um das Steuersignal kontinuierlich für



eine vorbestimmte Zeitdauer zu erzeugen, wenn der Einleitungsfeststellimpuls während der intermittierenden Erzeugung des Steuersignals empfangen wird, um das Steuersignal lediglich in einem speziellen Rahmen in jedem Datenblock zu erzeugen, zu welchem Rahmen der Empfänger gehört, nachdem der Synchronisationskodewort-Feststellimpuls während der kontinuierlichen Erzeugung des Steuersignals empfangen wurde, um das Steuersignal in dem vorbestimmten Intervall zu erzeugen, wenn der Fehlerfeststellimpuls während der Erzeugung des Steuersignals in dem speziellen Rahmen empfangen wird, und um das erzeugte Steuersignal an die Schaltereinrichtung (16) zu legen.

2. Personenrufempfänger nach Anspruch 1, bei welchem der Einsteller (36) das Steuersignal kontinuierlich für die vorbestimmte Zeitdauer erzeugt, wenn das Einleitungsfeststellsignal während der Erzeugung des Steuersignals zu dem vorbestimmten Zeitpunkt empfangen wird, und das erzeugte Steuersignal an die Schaltereinrichtung (16) legt.

3. Personenrufempfänger nach Anspruch 1 oder 2, der ferner Einrichtungen (37) zur Erzeugung eines Meldesignals in Reaktion auf den Adreßkodewort-Feststellimpuls aufweist.

4. Verfahren zur Batterieschonung eines Personenrufempfängers, welches die Schritte aufweist:

Zuführen von Strom zu einem vorbestimmten Teil (12, 13) des Empfängers in Reaktion auf ein Steuersignal;

intermittierendes Erzeugen des Steuersignals, während der Empfänger auf ein Personenrufsignal wartet, das ein Einleitungssignal hat und jedes von ihnen mit einem Synchronisationskodewort beginnt und mehrere Rahmen enthält, wobei der Empfänger zu einem der Rahmen gehört und Adreßkodewörter in diese Rahmen einzubeziehen sind, und

Feststellen eines ersten Synchronisationskodewortes, welches unmittelbar nach dem Einleitungssignal vorliegt, um ein Synchronisationsfeststellsignal zu erzeugen, gekennzeichnet durch die Schritte:

Erzeugen des Steuersignals in Reaktion auf das Synchronisationsfeststellsignal lediglich in einem speziellen Rahmen in jedem Datenblock, zu welchem Rahmen der Empfänger gehört; und

Feststellen eines Fehlers in Kodewörtern, die in dem Personenrufsignal enthalten sind, während das Steuersignal in dem speziellen

Rahmen erzeugt wird, und Ersetzen der Erzeugung des Steuersignals in dem vorbestimmten Rahmen durch die intermittierende Erzeugung, wenn die Zahl der festgestellten Fehler größer als ein vorbestimmter Wert ist.

5. Verfahren nach Anspruch 4, welches ferner die Schritte aufweist:

kontinuierliches Erzeugen des Steuersignals für eine vorbestimmte Zeitdauer, wenn ein Einleitungssignal in dem Personenrufsignal festgestellt wird;

Feststellen des ersten Synchronisationskodewortes, während das Steuersignal kontinuierlich für die vorbestimmte Zeitdauer erzeugt wird; und

kontinuierliches Erzeugen des Steuersignals während der vorbestimmten Zeitdauer, wenn das Einleitungssignal festgestellt wird, während das Steuersignal in dem speziellen Rahmen erzeugt wird.

Revendications

1. Récepteur de recherche de personnes comprenant :
- une section de réception (12, 13) afin de recevoir un signal de recherche de personnes comprenant un signal de préambule et des groupes qui suivent ledit signal de préambule et dont chacun commence avec un mot de code de synchronisation et contient une multitude de trames, ledit récepteur appartenant à l'une desdites trames, des mots de code d'adresse étant inclus dans lesdites trames;
 - un moyen de commutateur (16) pour commander l'alimentation de ladite section de réception en réponse à un signal de commande;
 - un moyen (32) pour détecter un signal de préambule afin de produire une impulsion de détection de préambule;
 - un moyen (33) pour détecter un premier mot de code de synchronisation qui est présent immédiatement après ledit signal de préambule afin de produire une impulsion de détection de mot de code de synchronisation; et
 - un moyen (34) pour détecter un mot de code d'adresse affecté audit récepteur afin de produire une impulsion de détection de mot de code d'adresse, caractérisé par :
 - un moyen de détecteur d'erreur (35) afin de détecter une erreur dans lesdites trames et produire une impulsion de détec-



tion d'erreur lorsque le nombre des erreurs détectées est supérieur à une valeur prédéterminée; et

- un moyen de contrôleur (36) pour, dans un mode d'attente, produire ledit signal de commande par intermittence à un intervalle prédéterminé, pour produire ledit signal de commande en continu pendant une période temporelle prédéterminée lors de la réception de ladite impulsion de détection de préambule pendant la production par intermittence dudit signal de commande, pour produire ledit signal de commande seulement à une trame particulière dans chaque groupe, trame à laquelle appartient ledit récepteur après la réception de ladite impulsion de détection du mode de code de synchronisation lors de la production en continu dudit signal de commande, pour produire ledit signal de commande audit intervalle prédéterminé lors de la réception de ladite impulsion de détection d'erreur pendant la production dudit signal de commande à ladite trame particulière, et pour appliquer le signal de commande produit audit moyen de commutateur (16).

2. Récepteur de recherche de personnes selon la revendication 1, dans lequel ledit contrôleur (36) produit ledit signal de commande en continu pendant la période temporelle prédéterminée lors de la réception dudit signal de détection de préambule pendant la production dudit signal de commande audit temps prédéterminé, et applique le signal de commande produit audit moyen de commutateur (16).

Récepteur de recherche de personnes selon la revendication 1 ou 2, comprenant en outre un moyen (37) pour produire un signal d'alerte en réponse à ladite impulsion de détection de mot de code d'adresse.

4. Procédé pour économiser l'énergie de la batterie d'un récepteur de recherche de personnes, comprenant les étapes consistant à :
- fournir de l'énergie à une section prédéterminée (12, 13) dudit récepteur en réponse à un signal de commande;
 - produire ledit signal de commande par intermittence alors que ledit récepteur est en attente d'un signal de recherche de personnes comprenant un signal de préambule et des groupes qui suivent ledit signal de préambule et dont chacun commence avec un mot de code de synchronisation et contient une multitude

de trames, ledit récepteur appartenant à l'une desdites trames, des mots de code d'adresse devant être inclus dans lesdites trames; et

- détecter un premier mot de code de synchronisation qui est présent immédiatement après ledit signal de préambule afin de produire un signal de détection de synchronisation, caractérisé par les étapes consistant à :
 - en réponse audit signal de détection de synchronisation, produire ledit signal de commande seulement à une trame particulière dans chaque groupe, trame à laquelle ledit récepteur appartient; et
 - détecter une erreur dans des mots de code qui sont contenus dans ledit signal de recherche de personnes alors que ledit signal de commande est produit à ladite trame particulière, et, lorsque le nombre des erreurs détectées est supérieur à une valeur prédéterminée, remplacer la production dudit signal de commande de ladite trame particulière par la production intermittente.
5. Procédé selon la revendication 4, comprenant en outre les étapes consistant à :
- produire ledit signal de commande en continu pendant une durée prédéterminée lorsqu'un signal de préambule dans ledit signal de recherche de personnes est détecté;
 - détecter ledit premier mot de code de synchronisation alors que ledit signal de commande est produit en continu pendant ladite durée prédéterminée; et
 - produire ledit signal de commande en continu pendant ladite durée prédéterminée lorsque ledit signal de préambule est détecté alors que ledit signal de commande est produit à ladite trame particulière.