"A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF MANUFACTURING THE SAME".

The present invention relates to a semiconductor integrated circuit device (hereinafter referred to as "IC") having a high density of integration and also to a method of manufacturing it.

New isolation techniques suited to render ICs high in the density of integration are being developed in large numbers. Many of them utilize what is known as the "isotropic" reactive ion etching in which side etching is scarcely involved, as disclosed in 'NIKKEI ELECTRONICS', March 29, 1982, pp 90 - 101.

Such isolation technique itself is applicable to, not only bipolar ICs, but also MOSICs. It can have its merits exploited especially in the bipolar ICs which require deep isolation regions. In the following, therefore, description will be centered on the bipolar ICs.

As one of the isolation techniques of the specified type, there is a method in which the part of a semiconductor body to become an isolation region is cut to form a groove, whereupon the groove is filled up by employing an insulating material, such as SiO_2, or polycrystalline silicon as a burying material.

A known expedient for filling up the groove part with the burying material is given below. On the whole surface of the semiconductor body formed with the groove, the burying material is deposited to be thick. Subsequently, the whole surface is etched and flattened in order to remove the excessive burying material.

In an IC, in laying out various elements such as transistors, a large isolation region for forming wiring is inevitably set in a selected part of a chip, particularly the peripheral part thereof. This poses the problem of the flattening of the surface of that part. The isolation region part which is narrow compared to its depth is not very serious because the groove is almost filled up. In contrast, regarding the isolation part which is wide comparatively to its depth, unavoidably a large hollow develops on the surface even after the deposition of the burying material. A process which is necessary for further flattening such surface is considerably complicated. Therefore, a process for the whole device becomes complicated and forms a serious difficulty in the aspect of production.

As a measure for solving such a difficulty, we have studied a method in which the width of the above referred to groove is set at a substantially constant small value within a range of e.g. about 1.0 - 2.5 μm in relation to the resolving power of photo lithography.

The reason is that, with the CVD (Chemical Vapour Deposition) process for depositing the burying material, the narrow groove is readily filled up because the burying material is piled up also from the side surfaces of the groove.

On the other hand, however, in the case where the width of the groove for electric isolation is rendered constant, wiring must be formed on the inactive area of a semiconductor body (the area where no semiconductor element is formed). The inactive area is not covered thereon with a thick insulating film as obtained by the use of the isoplanar technique. With such wiring structure, accordingly, the wiring capacitance between the wiring and the semiconductor body becomes large, resulting in the problem that the electrical characteristics of the device worsen, in particular that the signal propagation is delayed.

It is an object of the present invention to solve, in producing an IC by applying the isolation technique described above, the difficulty with respect to manufacture and also the delay in signal propagation.

According to one aspect of the present invention there is provided a semiconductor device including:

(a) a semiconductor body;

(b) an isolation region which electrically isolates a major surface of said semiconductor body into a plurality of semiconductor regions, and which comprises a groove extending in the major surface of said semiconductor body and a burying material filling up said groove;

(c) a semiconductor element which is formed within each of selected first semiconductor regions of said plurality of semiconductor regions, each selected first semiconductor region having at least a thin oxide film formed by oxidizing its major surface;

(d) a thick oxide film which is formed within at least one second semiconductor region of said plurality of semiconductor regions so as to cover substantially the whole surface thereof, which oxide film is thicker than said thin oxide film but less than the depth of the groove, and which is formed prior to the formation of the groove by oxidizing the major surface of said second semiconductor region; and

(e) wiring layers which extend over said thick oxide film within said at least one second semiconductor region, and which are used for interconnecting the semiconductor elements.

According to a second aspect of the invention there is provided a method of manufacturing a semiconductor device including the steps of:

(a) preparing a semiconductor body;

(b) selectively forming an oxidation impermeable mask

on a major surface of said semiconductor body; said mask covering a first surface portion of each of a plurality of first semiconductor regions in which semiconductor elements are to be respectively formed and a second surface portion of a second semiconductor region which lies among said plurality of first semiconductor regions and in which an isolation region is to be formed, leaving a third surface portion of a third semiconductor region which separates said first and second semiconductor regions;

(c) forming a thick oxide film in said third surface portion by thermal oxidation of the major surface of said semiconductor substrate by employing said oxidation impermeable mask;

(d) removing said oxidation impermeable mask of said second surface portion;

(e) forming a groove in said second surface portion of said major surface of said semiconductor body by employing as an etching mask the thick oxide film formed in said third surface portion prior to the formation of the groove and said oxidation impermeable mask covering said first surface portion, said groove having a depth greater than the thickness of the thick oxide film and electrically isolating said major surface of said semiconductor body into said plurality of first semiconductor regions;

(f) filling up said groove with a burying material;

(g) forming the semiconductor elements in said first semiconductor regions, the major surface of said each first semiconductor region having a thin oxide film which

is formed by thermal oxidation and which is thinner than said thick oxide film of said third surface portion; and

(h) forming wiring layers over said thick oxide being used for interconnecting said semiconductor elements.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Fig. 1 is a sectional view of a preferred form of bipolar IC;

Figs. 2A and 2F are processing step diagrams showing a preferred method of manufacturing the bipolar IC shown in Fig. 1.

Fig. 3 is a diagram showing an example of a mask pattern for use in the manufacturing technique.

referring to Fig. 1, a semiconductor body 100 has an N^+-type buried layer 5 and further an N^--type epitaxial layer 9 on a P-type silicon semiconductor substrate 2. A bipolar transistor is formed in an active area 1 where the element is to be formed, that is, a selected one of semiconductor areas which are electrically isolated by a groove 3 forming an isolation area. The active area includes a P-type base region 19, an N^+-type emitter region 21 and an N^+-type collector contact region 18. An electrode 30 of aluminium is held in

ohmic contact with the base region 19. Likewise, an aluminium electrode 31 is held in ohmic contact with the emitter region 21, and an aluminium electrode 32 with the collector contact region 18. These electrodes are brought into contact through contact holes which are provided in a thin oxide film 20 (several tens nm) formed by the thermal oxidation of the surface of the semiconductor body 100 and a passivation film 22.

As will be stated later, wiring layers 33 and 34 of aluminium are formed on a thick silicon oxide film 72 in an inactive area 6, namely, the area where no semiconductor element is formed among the semiconductor areas electrically isolated by the isolation area or groove 3.

In accordance with this invention, the deep groove 3 whose width is set substantially constant (for example, 1.0 - 1.5 μm) is formed in one surface of the semiconductor body 100 and over the whole area thereof, and the groove 3 is filled up with a burying material 4 which is an insulating material such as SiO_2. Thus, the electrical isolation among the elements is effected. The burying material may well be a material other than the insulator, for example, polycrystalline silicon. In this case, the surface of the polycrystalline

silicon filling up the groove needs to be oxidized. The isolation area defines a plurality of element forming areas. In the case of the bipolar IC, the deep groove 3 needs, at least, to be deep enough to reach the semiconductor substrate 2 through the buried layer 5, and its depth dimension is greater than its width dimension. In the case of a MOSIC, however, the groove can be shallowed within a range which the electrical isolation among the elements is possible. Accordingly, the expression "deep" in the deep groove 3 signifies that the groove has a depth sufficient for electrically isolating the elements.

In addition, thick oxide films 71 and 72 are formed due to the local oxidation of the surface

of the semiconductor body 100 over the whole surface parts of the areas (inactive areas) 6 where the semiconductor elements such as transistors are not formed. The thick oxide films 71 and 72 serve to reduce the stray capacitances of the aluminium wiring leads 33 and 34 to be formed thereon. They accordingly need, at least, be thick enough to lower the stray capacitances of the wiring leads. The thicknesses of the oxide films 71 and 72 are selected within a range from several hundred nm to a few μm. This value is considerably greater than the thickness of the thermal oxidation film 20 of the surface of the semiconductor body in the area where the semiconductor element is formed.

In the above embodiment, thin silicon oxide film 17 is formed in the groove portion. The silicon oxide film 17 is provided in order to protect the surface of the semiconductor body exposed in the groove 3, against contamination in later steps. In the case of employing any other material than the insulator as the burying material, the silicon oxide film 17 is indispensable, and it is rendered as thick as several hundred nm.

A thick silicon oxide film 70 serves to isolate the collector contact region 18 and the base region 19, and is formed simultaneously with the other thick

silicon oxide films 71 and 72.

The thick oxide films 71 and 72 adjoin the isolation area 8 among the elements to form the deep groove 3. Therefore, the thick oxide films 71 and 72 can be utilized as a mask at the step of forming the deep groove 3. From this viewpoint, it is favorable to form the thick oxide films 70, 71 and 72 by the local oxidation and thereafter form the deep groove 3.

In order to isolate the collector contact region 18 from the base region 19 by employing an insulator instead of the thick oxide film 70, a groove shallower than the groove 3 can also be used. However, in the present embodiment, the thick oxide film 70 is used for preventing the deterioration of the electrical characteristics of the transistor. This technique has been developed following our experiment on the isolation technique. Our study has revealed that, when the oxide film 70 is replaced with the groove shallower than the groove 3, defects concerning the characteristics of the element are liable to arise in the vicinity of the shallower groove. They are attributed to crystal defects caused by dislocations, and are difficult to avoid in devices of the structure isolating the collector contact region and the base region by the use of the shallower groove. With regard to the function of the

isolation, the isolation area 8 and the shallower groove for isolating the collector contact region join each other at both the ends of the shallower groove, so that the steps of the grooves develop in those parts.

Since, the collector contact region 18 is isolated by the oxide 70 produced by the local oxidation of the surface of the semiconductor body 100, the steps of the grooves are not involved, and the crystal defects due to the dislocations do not appear, either. Moreover, defects having originally existed can be caused to disappear by performing the local oxidation at a higher temperature of, e. g., about 1100 ^{o}C.

In the next place, there will be explained a manufacturing method which is well-suited for producing the bipolar IC shown in Figure 1.

First, an N^{+}-type buried layer 5 which is 1 - 2 μm thick is formed on the major surface of a P-type Si substrate 2 having the crystal face (100), and an N^{-}-type Si epitaxial layer (1 - 2 μm thick, more desirably 1.4 - 1.6 μm thick) 9 to become the active parts of a transistor is formed thereon. Thus, a semiconductor body 100 is obtained. Subsequently, the surface of the Si epitaxial layer 9 is thermally oxidized to form an SiO_2 film (silicon oxide film) 10 which is about

(22)

500 - 900 Å thick. On the SiO_2 film 10, an oxidation impermeable film, e.g. Si_3N_4 film 11 is deposited by the conventional CVD technique, and further an SiO_2 (or phosphosilicate glass) film 12 by the low pressure CVD technique, in succession. Thereafter, as shown in Fig. 2A, the SiO_2 film 12 and the Si_3N_4 film 11 are patterned by the conventional photolithography technique, to open parts which are to become an isolation area among elements and an inactive area 6 together with a collector contact isolation portion 13.

Next, selected parts of the opened isolation area 8 among the elements are covered with an Si_3N_4 film (silicon nitride film) 14. As shown in Figure 2B, using the Si_3N_4 film 14 and the opened Si_3N_4 film 11 as a mask, the surface of the Si body 100 is locally oxidized, whereby thick oxide films 70, 71 and 72 each having a thickness of about 1 μm are formed in the respective parts of the collector contact isolation portion 13 and the inactive areas 6. An example of the essential portions of mask patterns for use in these steps is shown in Figure 3. Regarding the positioning between a mask pattern 15 for forming the pattern of the SiO_2 film 12 as well as the Si_3N_4 film 11 and a mask pattern 16 for etching the Si_3N_4 film 14, the inner peripheral edge 16a of the mask pattern 16 may be arranged so as to overlie the mask pattern 15, and the positioning is easy. Thus,

the width of a groove 3 to be formed later becomes slightly greater at both ends of the oxide film 70. However, the change of the groove width to such extent does not affect the filling operation.

After the local oxidation has been ended in this way, the Si_3N_4 film 14 used as the mask for the local oxidation is removed, and the underlying SiO_2 film 10 is partly removed. As to the Si_3N_4 film 14, either the dry etching technique or the wet etching technique with hot phosphoric acid may be employed. As to the underlying SiO_2 film 10, the use of the dry etching is recommended. The reason is that, since the thick oxide films 70, 71 and 72 are utilized as a mask in the etching of the SiO_2 film 10, the overetching of them should be avoided. Basically, neither of the etching steps of the Si_3N_4 film 14 and the SiO_2 film 10 requires any new mask. Owing to the series of etching processing, Si in the part of the Si body 100 corresponding to the isolation area 8 among the elements is exposed as shown in Fig. 2C. If thereafter, the thick oxide films to serve as a mask for forming the groove are etched over the whole surfaces, then, the width of the groove can be made as great as desired. That is, the thin parts (known as bird's beak parts) at the ends of the thick oxide films are etched to increase the exposure of the Si body.

Next, the deep groove 3 is formed as shown in Fig.2D.

The deep groove 3 needs to have a depth at which it reaches the semiconductor substrate 2 by penetrating the buried layer 5. In order to form the deep groove 3, a reactive ion etching technique is used in which side etching is scarcely involved. As a gas, it is preferable to use CCl_4-gas to which O_2-gas is added. The capability of masking the etching action of the reactive ion etching becomes higher in the order of Si, Si_3N_4 and SiO_2. Si_3N_4 can be rendered about 10 times higher than Si in the capability, and SiO_2 about 20 times higher than Si. Accordingly, the deep groove 3 can be formed by utilizing such differences of the etching resistance. In forming such a deep groove 3, an obliquely etched surface may be formed in an upper part by anisotropic etching with an alkaline etchant such as hydrazine or potassium hydroxide KOH before the reactive ion etching. Alternatively, after the reactive ion etching, etching with fluoric or nitric acid may be added in order to shape the exposed surface. At the time of the completion of the etching for the deep groove 3, the Si_3N_4 film 11 as the mask can be removed almost entirely. Of course, the Si_3N_4 film 11 can be left behind depending upon the selection ratio of the ion etching, the thickness of the Si_3N_4 film and the depth of the etching groove.

Subsequently, a silicon oxide film (SiO_2 film) 17

having a thickness of 250 - 4000 Å is formed on the exposed inner surface of the deep groove 3 by thermal oxidation. At the same time, or after the formation of the oxide film 17, the major surface of the semiconductor body 100 is again covered with a silicon oxide film 20 being 500 - 900 Å thick by the thermal oxidation thereof. In forming the oxide film 20, the oxide film 10 needs to be removed in advance. Although the oxide film 10 can also be replaced with the oxide film 20, it is better to form the oxide film 20 anew. Thereafter, a burying material 4 which is an insulating material such as SiO_2 is deposited on the whole surface of the Si substrate 2 by the CVD process as shown in Fig. 2E. The amount of the deposition has to exceed at least the depth of the groove 3.

At the next step, the deposited burying material 4 is removed by an isotropic etching technique such as plasma etching, in order to flatten the major surface of the Si body 100 as shown in Fig. 2F. Thus, the isolation steps are completed. Since, in this case, the width of the deep groove 3 is rendered constant over the whole area of the Si body 100, the surface of the burying material 4 as deposited is substantially flat, and the surface flattening mentioned above is substantially simplified. It is sometimes recommended that the deposited burying material 4 is coated with

a photoresist or SOG (Spin On Glass), whereupon the surface is flattened by an isotropic etching technique resorting to physical means. Thus, the flattening of the surface can be executed more effectively. In the case where any material other than the insulator is employed as the burying material, its surface needs to be covered with an insulator. For example, in case of employing polycrystalline silicon, the surface is flattened, and it is covered with an SiO_2 film by thermal oxidation thereof.

After the isolation steps, the N^+-type collector contact portion 18 and the P-type base region 19 are formed in the epitaxial layer 9 as shown in Figure 2F. The collector contact portion 18 is formed by employing the oxide film 70 and the isolation area 8 as a mask, and in self-alignment thereto. The base region 19 is similarly formed. In forming the two regions, the registration margin of photoresist masks is unnecessary. A passivation film 22 such as silicon oxide film is formed on the surface and is patterned, and an N^+-type emitter region 21 is formed. Thereafter, as shown in Figure 1, aluminium electrodes 30, 31 and 32 are arranged through contact holes formed in the thin thermal oxidation film 20 and the passivation film 22, and wiring leads 33 and 34 are also provided in order to complete the bipolar IC.

In this manner, in the above described bipolar IC, the

collector contact isolation portion 13 is arranged at the boundary between the collector contact portion 18 and the base region 19, and hence, the breakdown voltage between the base and collector of the transistor can be enhanced sufficiently. In this case, in the illustrated example, the collector contact isolation portion 13 is formed of the oxide film 70 produced by local oxidation of the major surface of the Si body 100. Therefore, the oxide film 70 can be formed simultaneously with the thick oxide films 71 and 72 in order to reduce the capacitance coupled to the wiring.

The collector contact isolation portion 13, however, can also be constructed so as to fill up a groove with a burying material in similar manner to the isolation area 8 among the elements.

This invention is greatly effective when applied to a bipolar IC, especially a bipolar memory such as a PROM or RAM. It is also applicable to a MOSIC. In the application to the MOSIC, a P-type or N-type semiconductor body can be used for forming MOSFETs or for forming a complementary MOSIC (CMOSIC). In the CMOSIC, it is also possible to isolate the MOSFETs by thick oxide films and the well regions (of the P type and N type) by a deep groove.

As set forth above,

the width dimension of the deep groove 3 in the isolation area 8 among elements is rendered substantially constant over the whole semiconductor body 100, and hence, a process for flattening the surface of the burying material 4 can be substantially simplified. Moreover, since the thick oxide film 7 produced by the local oxidation of the surface itself of the semiconductor body 100 is formed in the surface part of the inactive area 6 where no semiconductor element is formed, the wiring capacitance between the substrate 2 and the wiring lead running on the inactive area 6 can be substantially reduced.

With the manufacturing method in which the thick oxide films 70, 71 and 72 are first formed by the local oxidation technique and the deep groove 3 is thereafter formed using these thick oxide films 70, 71 and 72 as a part of a mask, a great effect can be attained in the aspect of production concerning the mask registration.

CLAIMS:

1. A semiconductor device including:

(a) a semiconductor body;

(b) an isolation region which electrically isolates a major surface of said semiconductor body into a plurality of semiconductor regions, and which comprises a groove extending in the major surface of said semiconductor body and a burying material filling up said groove;

(c) a semiconductor element which is formed within each of selected first semiconductor regions of said plurality of semiconductor regions, each selected first semiconductor region having at least a thin oxide film formed by oxidizing its major surface;

(d) a thick oxide film which is formed within at least one second semiconductor region of said plurality of semiconductor regions so as to cover substantially the whole surface thereof, which oxide film is thicker than said thin oxide film but less than the depth of the groove, and which is formed prior to the formation of the groove by oxidizing the major surface of said second semiconductor region; and

(e) wiring layers which extend over said thick oxide film within said at least one second semiconductor region, and which are used for interconnecting the semiconductor elements.

2. A semiconductor device according to claim 1, wherein an oxide film is formed on a surface of said semiconductor body inside said groove.

3. A semiconductor device according to claim 2, wherein said burying material is silicon dioxide.

4. A semiconductor device according to claim 2, wherein said burying material is polycrystalline silicon.

5. A semiconductor device according to claim 4, wherein a surface of said polycrystalline silicon filling up said groove is covered with a silicon dioxide film produced by thermal oxidation thereof.

6. A semiconductor device according to any one of claims 3 to 5, wherein said semiconductor body comprises a P-type semiconductor substrate, and a plurality of layers which include an N-type buried region and an N-type epitaxial layer, formed one on the other on top of said semiconductor substrate, the N-type buried region having an impurity concentration which is higher than that of said epitaxial layer; and wherein said semiconductor element is a bipolar transistor, said bipolar transistor including an N-type collector region which is composed of said epitaxial layer, said buried region and a collector contact region having an impurity concentration higher than that of said epitaxial layer, a P-type base region which is formed within said epitaxial layer, and an N-type emitter region which is formed within said base region.

7. A semiconductor device according to claim 6, wherein said thick oxide film on said second semiconductor region is a first thick oxide film, and said collector contact region and said base region are isolated by a second thick oxide film which is formed by oxidizing the major surface of said first semiconductor regions, and which has a thickness substantially equal to that of said first thick oxide film.

8. A semiconductor device according to any one of the preceding claims, wherein there are spaces between one side of a respective groove and the respective adjacent second thick oxide films, said spaces being located between "birds beak" parts of the second thick oxide film and the burying material.

9. A semiconductor device according to claim 8, wherein the distance between the respective ends of the first and second thick oxide films and respective sides of the groove are of unequal length, that between the second thick oxide film being longer than that between the first thick oxide film to the respective sides of the groove.

10. A method of manufacturing a semiconductor device including the steps of:

(a) preparing a semiconductor body;

(b) selectively forming an oxidation impermeable mask on a major surface of said semiconductor body, said mask covering a first surface portion of each of a plurality of first semiconductor regions in which semiconductor elements are to be respectively formed and

a second surface portion of a second semiconductor region which lies among said plurality of first semiconductor regions and in which an isolation region is to be formed, leaving a third surface portion of a third semiconductor region which separates said first and second semiconductor regions;

(c) forming a thick oxide film in said third surface portion by thermal oxidation of the major surface of said semiconductor substrate by employing said oxidation impermeable mask;

(d) removing said oxidation impermeable mask of said second surface portion;

(e) forming a groove in said second surface portion of said major surface of said semiconductor body by employing as an etching mask the thick oxide film formed in said third surface portion prior to the formation of the groove and said oxidation impermeable mask covering said first surface portion, said groove having a depth greater than the thickness of the thick oxide film and electrically isolating said major surface of said semiconductor body into said plurality of first semiconductor regions;

(f) filling up said groove with a burying material;

(g) forming the semiconductor elements in said first semiconductor regions, the major surface of said each first semiconductor region having a thin oxide film which is formed by thermal oxidation and which is thinner than said thick oxide film of said third surface portion; and

(h) forming wiring layers over said thick oxide being used for interconnecting said semiconductor elements.

11. A method of manufacturing a semiconductor device according to claim 10, including before the burying step, the step of oxidizing a surface of said semiconductor body inside said groove thereby to form a silicon dioxide film.

12. A method of manufacturing a semiconductor device according to claim 11, wherein said burying material is silicon dioxide.

13. A method of manufacturing a semiconductor device according to claim 12, wherein said step of preparing said semiconductor body consists of the substep of forming an N-type buried region in a surface of a P-type semiconductor substrate, and the substep of forming an N-type epitaxial layer lower in impurity concentration than said buried region in the surface of said semiconductor substrate; wherein said groove is formed so as to reach said semiconductor substrate; and wherein said step of forming said semiconductor elements includes the substep of forming an N-type collector contact region reaching said buried region in a part of said each first semiconductor region, the substep of forming a P-type base region in another part of said first semiconductor region, and the substep of forming an N-type emitter region within said base region.

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14. A method of manufacturing a semiconductor device according to claim 13, wherein said oxidation impermeable mask is formed on the respective first surface portions except surface parts over regions to become regions between the collector contact regions and the base regions; and a thick oxide film is formed on regions between said collector contact regions and said base regions by thermal oxidation of said major surface of said semiconductor body simultaneously

with the formation of the thick oxide film of said third surface portion.

15. A method of manufacturing a semiconductor device according to Claim 11, wherein said burying material is polycrystalline silicon.

16. A method of manufacturing a semiconductor device according to Claim 15, wherein the polycrystalline silicon is covered with an oxide film which is formed by thermal oxidation thereof.

17. A method of manufacturing a semiconductor device according to Claim 16, wherein said step of preparing said semiconductor body consists of the substep of forming an N-type buried region in a surface of a P-type semiconductor substrate, and the substep of forming an N-type epitaxial layer lower in impurity concentration than said buried region in the surface of said semiconductor substrate; wherein said groove is formed so as to reach said semiconductor substrate; and wherein said step of forming said semiconductor elements includes the substep of forming an N-type collector contact region reaching said buried region in a part of said each first semiconductor region, the substep of forming a P-type base region in another part of said first semiconductor region, and the substep of forming an N-type emitter region within said base region.

18. A method of manufacturing a semiconductor device according to Claim 17, wherein said oxidation impermeable mask is formed on the respective first surface portions except surface parts over regions to become regions between the collector contact regions and the base regions; and a thick oxide film is formed on regions between said collector contact regions and said base regions by thermal oxidation of said major surface of said semiconductor body simultaneously with the formation of said thick oxide film of said third surface portion.

19. A method of manufacturing a semiconductor device according to Claim 10, wherein said oxidation impermeable mask is made of a silicon nitride film.

20. A method of manufacturing a semiconductor device according to Claim 19, wherein said silicon nitride film consists of silicon nitride films of a first level and a second level, the former of which is formed on said first surface portion and the latter of which is formed on at least said second surface portion.

21. A method of manufacturing a semiconductor device according to Claim 20, wherein a film different in property from said silicon nitride films is arranged therebetween in order to isolate said silicon nitride films of said first and second levels.

22. A method of manufacturing a semiconductor device according to any of Claims 10 to 21, wherein said groove

is formed by reactive ion etching.

23. A semiconductor device constructed substantially as herein described with reference to and as illustrated in the accompanying drawings.

24. A method of manufacturing a semiconductor device substantially as herein described with reference to Figs. 2A to 2F of the accompanying drawings.