## Description

### Technical Field

This invention relates to integrated circuits including field effect transistors and to methods for making them.

### Background of the Invention

As the complexity of integrated circuits continues to increase, there is a continuing need to reduce dimensions of the individual components of the integrated circuits to increase device packing density. For field effect transistors, this need includes not only reducing the dimensions of the channel but also the areas of the source and drain regions.

One approach to reducing the channel length is described in U.S. Patent 4,324,038 issued on April 13, 1982 to C. C. Chang et al. The device disclosed can he termed a "grooved gate" which is formed by patterning a metal or silicide, silicon oxide, silicon nitride structure to form an opening between the field oxide regions, depositing and etching an oxide layer to form insulating sidewall spacers, growing a gate oxide and making the appropriate metal contacts. In forming the sidewalls, the silicon nitride acts as an etch stop to prevent overetching of the silicon oxide. The sidewalls act as an insulator to prevent contact between the gate metal and the source and drain contact layers. The described gate structure may be adversely affected by the etching which is necessary for the gate, because the etching may damage the portion of the substrate forming the channel. Additionally, patterning requires a gate head to compensate for misregistration and the horizontal dimension required for the gate layout is not a minimum.

It has also been realized that self-aligned source and drain contacts can reduce device size. One such process is described by NEC in Japanese Journal of Applied Physics, *21*, pp. 34-38, Symposium on VLSI Technology, September 1-3, 1982. After gate formation and source and drain implantation, an oxide is formed which is thicker on the gate than on the bulk silicon. Etching removes the oxide on the bulk silicon while leaving oxide on the gate. A nitride layer is now formed on the bulk silicon and serves as a mask during a second oxidation. The nitride is removed and doped polysilicon deposited for the source and drain contacts. IBM Technical Disclosure Bulletin, *26*, pp. 4303-4307, January, 1984 describes a generally similar process although the nitride layer is formed by ion implantation.

The NEC process suffers several drawbacks. It is difficult to control the oxide etching because there is no etch stop and reliance must be placed on the difference in oxide thicknesses. Additionally, growing the nitride at high temperature is not desirable because the junction may be driven deeper. The IBM process suffers the drawback that the ion implantation is likely to create many defects and lead to high stress levels.

Another approach to producing devices with small area source and drain regions is described in U.S. Patent 4,453,306 issued on June 12, 1984 to William T. Lynch and Frederick Vratny. Device fabrication begins with formation of a multilevel gate electrode having sequential layers of a conductor, an insulator and a silicide forming metal deposited on an insulating layer. Standard depositing and patterning techniques are used. A layer of polycrystalline silicon is blanket deposited over the entire structure, and a heat treatment forms the silicide on the gate structure. A selective etch removes the silicide and leaves the polysilicon aligned with respect to both the source and drain regions. Windows are formed in a blanket deposited dielectric layer for contacts to both the source and drain regions.

Although the structure is self-aligned, the precise control of the process may be difficult as the boundary between the polysilicon and the silicide may not he sharp because diffusion and etching of the sidewalls may occur. Also, the etching of the four layer metal containing sandwich may require a separate etching machine because of possible contamination. The windows are spaced further from the gate electrode than are the source and drain regions thus reducing packing density. The spacing of the windows is stated as desirable because it, e.g., reduces the possibility of aluminum spiking into the substrate and simplifies etching as all three contacts are at approximately the same level. Deeper etching for source and drain contact window than for the gate might cause growth of the gate window.

### Summary of the Invention

A method according to the invention is set out in claim 1. Preferred forms of the invention are set out in the sub-claims.

### Brief Description of the Drawing

FIGs. 1-4 illustrate stages in the fabrication of field effect transistors according to this invention, and in particular:

FIG. 1 shows the structure before gate patterning;

FIG. 2 shows the structure after the gate has been patterned and the sidewall spacers have been fabricated;

FIG. 3 shows the structure after the window pad layer has been deposited and patterned;

FIG. 4 shows the structure after the metal for source and drain contacts has been deposited and patterned;

FIG. 5 shows a cell using the window pad layer as a sublevel interconnection; and

FIG. 6 is a sectional view of the cell in FIG. 5 along the line A-A'.

For reasons of clarity, the elements of the structures depicted are not drawn to scale.

## Detailed Description

An exemplary method of fabricating a field effect transistor will be described together with several variations. Other variations will be apparent to those skilled in the art.

Depicted in FIG. 1 are silicon substrate 1 and disposed thereon: field oxide regions 3, gate oxide 5, silicide/polysilicon layer 7, deposited oxide 9, silicon nitride ($Si_3N_4$) layer 11 and patterned photoresist 13. The photoresist has been patterned for fabrication of the gate electrode, i.e., transfer of the gate electrode pattern into layers 5, 7, 9 and 11. The structure depicted is fabricated by techniques well known to those skilled in the art and accordingly need not he described in detail. Appropriate layer thicknesses will he readily selected by those skilled in the art. Although a sectional view of only a single device is depicted in FIGs. 1-4, it will be readily appreciated that many devices are present in an integrated circuit.

The metal layer used to form the silicide may be omitted if only a polysilicon layer is desired, i.e., the silicide need not be present. Layer 11 is resistant to the etch, described later, used to form the insulating sidewall spacers. Materials other than silicon nitride may be used for layer 11 provided that they etch at a rate significantly lower than the rate for the sidewall spacer material.

Conventional etching techniques are now used to define the gate structure, that is, to pattern the layers that form the gate structure. An ion implantation is performed to form lightly doped source and drain regions 15. The insulating sidewall spacers 17 are formed by techniques well known to those skilled in the art. For example, an oxide can be blanket deposited and then etched back to leave the sidewall spacers. The $Si_3N_4$ acts as an etch stop and prevents etching of the gate during this step. A second ion implantation is now performed for the source and drain regions 19 followed by, if desired, silicide 21 formation in the source and drain regions. The resulting structure is depicted in FIG. 2.

A layer of conductive material, for example, TiN, is now deposited and patterned so that the source and drain regions, as well as the sidewall spacers, are covered. The patterned layer is called window pad 23. A portion of the field oxide will be typically covered. Techniques for depositing and patterning TiN are well known in the art and need not be described in detail. The layer may be as much as 600 nm thick although typically only 200 nm will be needed. Slight misregistrations of the mask may be tolerated as the materials surrounding the source and drain regions are electrically insulating and electrical shorts will not occur if the window pad covers a small portion of the gate electrode surface. It is only necessary that the portions of the source and drain regions required to form electrical contacts be covered, i.e., not all of the source and drain regions need be covered.

A passivating dielectric layer 25 is now deposited and patterned to expose selected portions of the window pads for electrical contacts as well as open windows for the gate contacts. The windows lie substantially directly above the source and drain regions but need not he the same size as the source and drain regions. Misregistrations will result in the windows exposing portions of adjacent insulating layers. A metal, for example, aluminum or tungsten, is now blanket deposited to cover the dielectric and fill the windows. The metal is now patterned to form contacts 27 and the resulting structure is depicted in FIG. 4. Alternatively, selective deposition may be used to fill the windows.

The spacings between the window and the gate, as well as the source and drain regions, may be greatly reduced as compared to typical prior art structures. This is true because the window can overlap the sidewall spacer and the field oxide provided that the window exposes a portion of the window pad layer as shown in FIG. 4. It is also noted that TiN is advantageously used as a window pad layer material because it also serves as a barrier preventing spiking of either aluminum or tungsten from the window into the substrate. It is also a desirable material because the etching selectivity of TiN with respect to the dielectric during the window etch is extremely good and may be, typically 1:15. It will he readily appreciated that any conductive material with similar etching properties may be used for the window pad.

The window pad layer is formed from a conductive material and, in another embodiment of this invention, is used for sublevel interconnection runners. This use can further reduce the chip layout area. An exemplary layout is depicted in FIG. 5 in a top view of a cell showing TiN used as sublevel interconnection. Depicted are the thin oxide layer 51, sublevel interconnects 53, polysilicon gate run-

ners 55, and contact windows 59. A sectional view of the structure along the line A-A' is shown in FIG. 6. The numerals used correspond to those used in FIGs. 1-4. For this embodiment, the window pad layer is patterned not only for the source and drain contacts but also to interconnect the source and drain regions of different transistors. If desired, a merged contact scheme may also connect to the gate runner. It will be appreciated that the window pad layer is insulated from the gate electrodes and can therefore cross the gate structures. It will also be readily appreciated that the sublevel interconnection described needs only one deposition and one patterning step.

In addition to the significant amount of area saved by the transistor structure, the sublevel interconnection scheme can save additional area due to the routing structure depicted. For example, the output of a logic cell is usually obtained by connecting the source/drain regions to a polysilicon runner by an aluminum metallization. This means that the source and drain regions need to contact the aluminum runner and that the aluminum runner needs to contact the polysilicon by an additional window opening contact. The polysilicon is used as an output runner across the field oxide and connects to the input of another cell. However, the structure depicted can greatly improve the routing. The window pad layer can be patterned to run directly across the field oxide to any desired input node without the need for any indirect connection. Therefore, some output polysilicon runners can be eliminated and their corresponding areas saved. Additionally, window contact area can be saved and the number of window contacts can also be reduced.

Thus, the interconnection scheme described can cross the field oxide to obtain additional flexibility. Additionally, it can cross polysilicon runners and can connect to a polysilicon runner by a merged contact or a butting contact.

The fabrication sequence when the window pad layer is formed from a polycide differs slightly from the sequence described for TiN. In particular, the window pad material, polysilicon, used for sublevel interconnects, is deposited after the sidewall spacers are formed. The source and drain implants are performed followed by window pad layer patterning. The source and drain regions are doped by a thermal drive out from the polysilicon as the implant energies are desirably chosen so that the implant damage is restricted to the polysilicon. A metal film is now deposited and the salicide (self-aligned silicide) formed by well known techniques. The unreacted metal may be removed by a wet chemical etch. Exemplary etching solutions are mixtures of $H_2SO_4/H_2O_2$ and $H_3PO_4/H_2O_2/H_2O$. The etching selectivities of polysilicon to oxide and oxide to polycide are 20-30:1 and 10-15:1, respectively. Both ratios are quite acceptable for window pad patterning and opening windows and ratios as low as 7:1 are likely to be useful.

Those skilled in the art will readily appreciate that other embodiments of this invention are possible.

## Claims

1. A method of fabricating an integrated circuit having a plurality of transistors, comprising:

   forming gate structures, each comprising a gate oxide (5), a gate electrode (7) and an insulating top layer (9,11),

   fabricating insulating sidewall spacers (17) on the sides of said gate structures by etching a deposited insulating material, said insulating top layer acting as an etch stop;

   forming source and drain regions (15,19,21)

   depositing and lithographically patterning a conductive window pad layer (23) so that said window pad layer contacts at least one of said source and drain regions at least one of said insulating sidewall spacers and at least one of said insulating top layer and the field oxide separating two adjacent transistors, said insulating top layer insulating said gate electrode from said window pad layer;

   depositing and patterning a dielectric layer (25) to form windows in said dielectric layer, said windows being substantially directly above at least some of said source and drain regions and exposing at least portions of said window pad layer; and

   depositing a contact material (27) in said windows.

2. A method as claimed in claim 1 in which said window pad layer is of TiN, a silicide, polysilicon or a polycide.

3. A method as claimed in claim 2 in which said window pad layer comprises polysilicon.

4. A method as claimed in claim 2 in which said window pad layer comprises TiN.

5. A method as claimed in any of the preceding claims in which said source and drain forming step comprises ion implantation.

6. A method of fabricating an integrated circuit having a plurality of transistors, comprising:

   forming gate structures, each comprising a gate oxide (5), a gate electrode (7) and an insulating top layer (9,11),

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ners 55, and contact windows 59. A sectional view of the structure along the line A-A' is shown in FIG. 6. The numerals used correspond to those used in FIGs. 1-4. For this embodiment, the window pad layer is patterned not only for the source and drain contacts but also to interconnect the source and drain regions of different transistors. If desired, a merged contact scheme may also connect to the gate runner. It will be appreciated that the window pad layer is insulated from the gate electrodes and can therefore cross the gate structures. It will also be readily appreciated that the sublevel interconnection described needs only one deposition and one patterning step.

In addition to the significant amount of area saved by the transistor structure, the sublevel interconnection scheme can save additional area due to the routing structure depicted. For example, the output of a logic cell is usually obtained by connecting the source/drain regions to a polysilicon runner by an aluminum metallization. This means that the source and drain regions need to contact the aluminum runner and that the aluminum runner needs to contact the polysilicon by an additional window opening contact. The polysilicon is used as an output runner across the field oxide and connects to the input of another cell. However, the structure depicted can greatly improve the routing. The window pad layer can be patterned to run directly across the field oxide to any desired input node without the need for any indirect connection. Therefore, some output polysilicon runners can be eliminated and their corresponding areas saved. Additionally, window contact area can be saved and the number of window contacts can also be reduced.

Thus, the interconnection scheme described can cross the field oxide to obtain additional flexibility. Additionally, it can cross polysilicon runners and can connect to a polysilicon runner by a merged contact or a butting contact.

The fabrication sequence when the window pad layer is formed from a polycide differs slightly from the sequence described for TiN. In particular, the window pad material, polysilicon, used for sublevel interconnects, is deposited after the sidewall spacers are formed. The source and drain implants are performed followed by window pad layer patterning. The source and drain regions are doped by a thermal drive out from the polysilicon as the implant energies are desirably chosen so that the implant damage is restricted to the polysilicon. A metal film is now deposited and the salicide (self-aligned silicide) formed by well known techniques. The unreacted metal may be removed by a wet chemical etch. Exemplary etching solutions are mixtures of $H_2SO_4/H_2O_2$ and $H_3PO_4/H_2O_2/H_2O$. The etching selectivities of polysilicon to oxide and oxide to polycide are 20-30:1 and 10-15:1, respectively. Both ratios are quite acceptable for window pad patterning and opening windows and ratios as low as 7:1 are likely to be useful.

Those skilled in the art will readily appreciate that other embodiments of this invention are possible.

## Claims

1. A method of fabricating an integrated circuit having a plurality of transistors, comprising:

   forming gate structures, each comprising a gate oxide (5), a gate electrode (7) and an insulating top layer (9,11),

   fabricating insulating sidewall spacers (17) on the sides of said gate structures by etching a deposited insulating material, said insulating top layer acting as an etch stop;

   forming source and drain regions (15,19,21)

   depositing and lithographically patterning a conductive window pad layer (23) so that said window pad layer contacts at least one of said source and drain regions at least one of said insulating sidewall spacers and at least one of said insulating top layer and the field oxide separating two adjacent transistors, said insulating top layer insulating said gate electrode from said window pad layer;

   depositing and patterning a dielectric layer (25) to form windows in said dielectric layer, said windows being substantially directly above at least some of said source and drain regions and exposing at least portions of said window pad layer; and

   depositing a contact material (27) in said windows.

2. A method as claimed in claim 1 in which said window pad layer is of TiN, a silicide, polysilicon or a polycide.

3. A method as claimed in claim 2 in which said window pad layer comprises polysilicon.

4. A method as claimed in claim 2 in which said window pad layer comprises TiN.

5. A method as claimed in any of the preceding claims in which said source and drain forming step comprises ion implantation.

6. A method of fabricating an integrated circuit having a plurality of transistors, comprising:

   forming gate structures, each comprising a gate oxide (5), a gate electrode (7) and an insulating top layer (9,11),

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fabricating insulating sidewall spacers (17) on the sides of said gate structures by etching a deposited insulating material, said insulating top layer acting as an etch stop;

depositing, doping and lithographically patterning a conductive window pad layer (23) of polysilicon so that at least a portion of said window pad layer contacts at least one of said insulating sidewall spacers and contacts at least one of said insulating top layer and the field oxide separating two adjacent transistors, said insulating top layer insulating said gate electrode from said window pad layer; forming source and drain regions by thermal drive-out of dopants from said polysilicon window pad layer;

depositing and patterning a dielectric layer (25) to form windows in said dielectric layer, said windows being substantially directly above at least some of said source and drain regions and exposing at least portions of said window pad layer; and

depositing a contact material (27) in said windows.

7. A method as claimed in any of the preceding claims in which said sidewall spacers comprise an oxide.

8. A method as claimed in any of the preceding claims in which said window pad layer is patterned so as to include portions (53) interconnecting source and drain regions of at least two transistors.

9. A method as claimed in claim 8 in which one or more of the said portions of the window pad layer cross the gate structure of at least one transistor.

10. A method as claimed in claim 8 or claim 9 in which the total number of said windows is less than the total number of said source and drain regions.

**Patentansprüche**

1. Verfahren zur Herstellung einer integrierten Schaltung mit einer vielzahl von Transistoren umfassend: Ausbilden von Gate-Strukturen, die jede ein Gate-Oxid (5), eine Gate-Elektrode (7) und eine isolierende obere Schicht (9, 11) umfassen, Ausbilden isolierender Seitenwand-Abstandshalter (17) an den Seiten der Gate-Strukturen durch Ätzen eines abgeschiedenen, isolierenden Materials, wobei die isolierende obere Schicht als Ätzstopp wirkt, Ausbilden von Source- und Drain-Bereichen (15, 19, 21), Abscheiden und lithographisches Strukturieren einer leitfähigen Fenster-Anschlußschicht 23, so daß die Fenster-Anschlußschicht wenigstens einen von den Source- oder Drain-Bereichen und wenigstens einen der isolierenden Seitenwand-Abstandshalter kontaktiert und wenigstens die isolierende obere Schicht oder das Feldoxid, das zwei benachbarte Transistoren trennt, kontaktiert, wobei die isolierende obere Schicht die Gate-Elektrode gegenüber der Fenster-Anschlußschicht isoliert,
Abscheiden und Strukturieren einer dielektrischen Schicht (25) zum Ausbilden von Fenstern in der dielektrischen Schicht, wobei die Fenster im wesentlichen direkt oberhalb wenigstens eines Teils des Source- und Drain-Bereichs sind und wenigstens Teile der Fenster-Anschlußschicht freilegen, und
Abscheiden eines Kontaktmaterials (27) in den Fenstern.

2. Verfahren nach Anspruch 1,
in welchem die Fenster-Anschlußschicht TiN, ein Silicid, Polysilicium oder ein Polycid enthält.

3. Verfahren nach Anspruch 2,
in welchem die Fenster-Anschlußschicht Polysilicium umfaßt.

4. Verfahren nach Anspruch 2,
in welchem die Fenster-Anschlußschicht TiN umfaßt.

5. Verfahren nach einem der vorstehenden Ansprüche,
in welchem die Source- und Drain-ausbildenden Schritte Ionenimplantation umfassen.

6. Verfahren zur Herstellung einer integrierten Schaltung mit einer Vielzahl von Transistoren umfassend:
Ausbilden von Gate-Strukturen, die jede ein Gate-Oxid (5), eine Gate-Elektrode (7) und eine isolierende obere Schicht (9, 11) umfassen,
Herstellen isolierender Seitenwand-Abstandshalter (17) an den Seiten der Gate-Strukturen durch Ätzen eines abgeschiedenen isolierenden Materials, wobei die isolierende obere Schicht als Ätzstopp wirkt,
Abscheiden, Dotieren und lithographisches Strukturieren einer leitfähigen Fenster-Anschlußschicht (23) aus Polysilicium, so daß wenigstens ein Teil der FensterAnschlußschicht wenigstens einen der isolierenden Seitenwandabstandshalter kontaktiert und wenigstens die isolierende obere Schicht oder das Feldoxid, das zwei benachbarte Transistoren trennt, kon-

taktiert, wobei die isolierende obere Schicht die Gate-Elektrode gegenüber der Fenster-Anschlußschicht isoliert,
Ausbilden von Source- und Drain-Bereichen durch thermisches Austreiben von Dotierstoffen aus der Polysilicium-FensterAnschlußschicht,
Abscheiden und Strukturieren einer dielektrischen Schicht (25) zum Ausbilden von Fenstern in der dielektrischen Schicht, wobei die Fenster im wesentlichen direkt oberhalb wenigstens eines Teils des Source- und Drain-Bereichs ist und
Freilegen wenigstens eines Anteils der Fenster-Anschlußschicht und
Abscheiden eines Kontaktmaterials (27) in den Fenstern.

7. Verfahren nach einem der vorstehenden Ansprüche,
in welchem die Seitenwand-Abstandshalter ein Oxid enthalten.

8. Verfahren nach einem der vorstehenden Ansprüche,
in welchem die Fenster-Anschlußschicht strukturiert ist, um Anteile (53) zu umfassen, die Source- und Drain-Bereiche von wenigstens zwei Transistoren miteinander verbinden.

9. Verfahren nach Anspruch 8,
bei welchem einer oder mehrere der besagten Anteile der Fenster-Anschlußschicht die Gate-Struktur wenigstens eines Transistors kreuzen.

10. Verfahren nach Anspruch 8 oder 9,
in welchem die gesamte Anzahl der Fenster niedriger als die gesamte Anzahl der Source- und Drain-Bereiche ist.

**Revendications**

1. Un procédé de fabrication d'un circuit intégré comportant un ensemble de transistors, comprenant:
la formation de structures de grille, comprenant chacun un oxyde de grille (5), une électrode de grille (7) et une couche supérieure isolante (9, 11),
la fabrication d'éléments d'espacement de parois latérales isolants (17) sur les côtés de ces structures de grille, par attaque d'un matériau isolant déposé, la couche supérieure isolante remplissant la fonction d'un élément d'arrêt d'attaque;
la formation de régions de source et de drain (16, 19, 21)
le dépôt d'une couche de plot de fenêtre conductrice (23), et la formation d'un motif, par lithographie, dans cette couche, de façon que la couche de plot de fenêtre vienne en contact avec l'une au moins des régions de source et de drain, avec l'un au moins des éléments d'espacement de parois latérales isolants, et avec l'un au moins des éléments comprenant la couche supérieure isolante et l'oxyde de champ qui sépare deux transistors adjacents, la couche supérieure isolante isolant l'électrode de grille vis-à-vis de la couche de plot de fenêtre;
le dépôt d'une couche diélectrique (25) et la formation d'un motif dans cette couche pour former des fenêtres dans la couche diélectrique, ces fenêtres étant pratiquement situées directement au-dessus de certaines au moins des régions de source et de drain, et mettant à nu au moins des parties de la couche de plot de fenêtre; et
le dépôt d'un matériau de contact (27) dans les fenêtres.

2. Un procédé selon la revendication 1, dans lequel la couche de plot de fenêtre consiste en TiN, en un siliciure, en silicium polycristallin ou en un siliciure polycristallin.

3. Un procédé selon la revendication 2, dans lequel la couche de plot de fenêtre consiste en silicium polycristallin.

4. Un procédé selon la revendication 2, dans lequel la couche de plot de fenêtre consiste en TiN.

5. Un procédé selon l'une quelconque des revendications précédentes, dans lequel l'étape de formation de régions de source et de drain comprend une implantation ionique.

6. Un procédé de fabrication d'un circuit intégré comportant un ensemble de transistors, comprenant:
la formation de structures de grille, comprenant chacun un oxyde de grille (5), une électrode de grille (7) et une couche supérieure isolante (9, 11)
la fabrication d'éléments d'espacement de parois latérales isolants (17) sur les côtés de ces structures de grille, par attaque d'un matériau isolant déposé, la couche supérieure isolante remplissant la fonction d'un élément d'arrêt d'attaque;
le dépôt et le dopage d'une couche de plot de fenêtre conductrice (23) en silicium polycristallin, et la formation d'un motif par lithographie dans cette couche, de façon qu'au

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moins une partie de la couche de plot de fenêtre vienne en contact avec l'un au moins des éléments d'espacement de parois latérales isolants, et l'un au moins des éléments comprenant la couche supérieure isolante et l'oxyde de champ qui sépare deux transistors adjacents, cette couche supérieure isolante isolant l'électrode de grille vis-à-vis de la couche de plot de fenêtre;

la formation de régions de source et de drain par expulsion thermique de dopants à partir de la couche de plot de fenêtre en silicium polycristallin;

le dépôt d'une couche diélectrique (25) et la formation d'un motif dans cette couche, pour former des fenêtres dans la couche diélectrique, ces fenêtres étant pratiquement situées directement au-dessus de certaines des régions de source et de drain, et mettant à nu des parties au moins de la couche de plot de fenêtre; et

le dépôt d'un matériau de contact (27) dans les fenêtres.

7. Un procédé selon l'une quelconque des revendications précédentes, dans lequel les éléments d'espacement de parois latérales consistent en un oxyde.

8. Un procédé selon l'une quelconque des revendications précédentes, dans lequel le motif qui est formé dans la couche de plot de fenêtre est tel que cette couche comprenne des parties (53) qui interconnectent des régions de source et de drain d'au moins deux transistors.

9. Un procédé selon la revendication 8, dans lequel une ou plusieurs des parties précitées de la couche de plot de fenêtre croisent la structure de grille d'au moins un transistor.

10. Un procédé selon la revendication 8 ou la revendication 9, dans lequel le nombre total des fenêtres est inférieur au nombre total des régions de source et de drain.