

What is Claimed is:

1. A semiconductor package, comprising:
 - a first layer comprising a first semiconductor chip and a first through via;
 - a first redistribution layer disposed on a surface of the first layer, and comprising a first-first wiring and a second-first wiring; and
 - a second layer comprising a second semiconductor chip and a second through via, and stacked on the first layer;
 - a second redistribution layer disposed on a surface of the second layer,
 - wherein the first semiconductor chip comprises a first-first buffer, and the first-first buffer is electrically connected between the first-first wiring and the second-first wiring, and
 - wherein the second through via is electrically connected to the first redistribution layer and the second redistribution layer.

2. The semiconductor package of claim 1, wherein the first semiconductor chip comprises a first-first pad, a second-first pad, and a third-first pad,
 - wherein the first-first buffer is electrically connected between the first-first pad and the second-first pad,
 - wherein the first-first wiring is connected to the first-first pad, the second-first wiring is connected to the second-first pad and the third-first pad, and
 - wherein the first-first wiring is connected to an external connection terminal which is an input/output terminal.

3. The semiconductor package of claim 2, wherein the first redistribution layer is disposed between the first layer and the second layer, and

wherein the first through via is electrically connected to the first-first wiring and the external connection terminal.

4. The semiconductor package of claim 3, wherein the second redistribution layer comprises a first-second wiring and a second-second wiring, and

wherein the second through via is electrically connected to the second-first wiring of the first redistribution layer and the second-second wiring of the second redistribution layer.

5. The semiconductor package of claim 4, wherein the first semiconductor chip further comprises a second-first buffer, and

wherein the second-first buffer is electrically connected between the second-first wiring and the first-first wiring.

6. The semiconductor package of claim 5, wherein the first redistribution layer further comprises a third-first wiring,

wherein the first semiconductor chip further comprises a third-first buffer, and

wherein the third-first buffer is electrically connected between the second-first wiring and the third-first wiring.

7. The semiconductor package of any one of claims 2 to 6, wherein the first layer further comprises a first panel formed with a first receiving portion for receiving the first semiconductor chip, and

wherein the first through via is a through panel via (TPV) through the first panel.

8. The semiconductor package of claim 1 or claim 2, further comprising an

external connection terminal which is an input/output terminal, and

wherein the first layer is disposed between the first redistribution layer and the second layer, and the external connection terminal is disposed on the first redistribution layer, and the first redistribution layer is disposed between the external connection terminal and the first layer.

9. The semiconductor package of claim 8, wherein the first-first wiring is electrically connected to the second-first wiring, and

wherein the second-first wiring is electrically connected to the first through via.

10. The semiconductor package of claim 9, wherein the second redistribution layer comprises a first-second wiring and a second-second wiring, and

wherein the second semiconductor chip comprises a first-second buffer, a first-second pad, and a second-second pad, and a third-second pad,

wherein the first-second buffer is electrically connected between the first-second pad and the second-second pad,

wherein the first-second wiring is electrically connected to the first-second pad, and the second-second wiring is electrically connected to second-second pad and the third-second pad, and

wherein the first through via is electrically connected to the second-second wiring, and

wherein the second redistribution layer is disposed between the first layer and the second layer.

11. The semiconductor package of claim 9, wherein the second redistribution

layer comprises a first-second wiring and a second-second wiring, and

wherein the second semiconductor chip comprises a first-second buffer, a first-second pad, a second-second pad, and a third-second pad,

wherein the first-second buffer is electrically connected between the first-second pad and the second-second pad,

wherein the first-second wiring is electrically connected to the first-second pad, and the second-second wiring is electrically connected to the second-second pad and the third-second pad,

wherein the first through via is electrically connected to the second through via, and the second through via is electrically connected to the first-second wiring, and

wherein the second layer is disposed between the second redistribution layer and the first layer.

12. The semiconductor package of claim 11, wherein the first through via is directly connected to the second through via.

13. The semiconductor package of any one of claims 1 to 12, further comprising:
a panel disposed between an external connection terminal and the first layer;
a third semiconductor chip disposed on the panel; and
a molding layer covering the third semiconductor chip, and
wherein the third semiconductor chip comprises a memory controller for controlling the first and second semiconductor chips.

14. The semiconductor package of any one of claims 1 to 11, wherein the first through via and the second through via are located at different positions on a plane not to

overlap each other.

15. The semiconductor package of any one of claims 1 to 14, wherein the first buffer is a bidirectional buffer.

16. The semiconductor package of any one of claims 1 to 15, wherein the first semiconductor chip of the first layer and the second semiconductor chip of the second layer are substantially the same.

17. The semiconductor package of any one of claims 1 to 6 or 8 to 12, wherein the first layer further comprises a first panel having a first receiving portion to receive the first semiconductor chip, and

wherein the first through via is a through panel via (TPV) or a through silicon via (TSV) penetrating the first panel.

18. A semiconductor package comprising a plurality of layers,
wherein two or more of the layers comprise respective semiconductor chips, insulated from one another, and redistribution layers respectively disposed on the semiconductor chips,
wherein each semiconductor chip comprises two or more pads connected to one another by a plurality of wirings included in a corresponding redistribution layer, one of the pads being an input/output pad of a corresponding semiconductor chip,

wherein a first-first wiring included in a first redistribution layer disposed on a first layer, among the two or more layers, is configured to be connected to an external input/output terminal,

wherein the first redistribution layer further comprises a second-first wiring,

connected to the input/output pad of a first semiconductor chip included in the first layer, and at least one buffer connecting the first-first wiring and the second-first wiring by being disposed therebetween, and

wherein a second layer among the two or more layers comprises a second through via penetrating the second layer to connect one of the first-first wiring and the second-first wiring in the first redistribution layer to a second-second wiring included in a second redistribution layer disposed on the second layer.

19. The semiconductor package of claim 18, wherein the first layer comprises a first through via penetrating the first layer to connect the first-first wiring and the external input/output terminal,

wherein the second-second wiring included in the second redistribution layer disposed on the second layer is further connected to the input/output pad of the second semiconductor chip, and

wherein the second redistribution layer further comprises a first-second wiring and at least one buffer connecting the first-second wiring and the second-second wiring by being disposed therebetween.

20. A semiconductor package comprising a plurality of layers which are vertically stacked,

wherein two or more of the layers comprise respective semiconductor chips, insulated from one another, and redistribution layers respectively disposed on the semiconductor chips,

wherein each of the respective layers comprises a plurality of wirings and a same number of buffers connecting the wirings,

wherein the wirings are connected to a pad included in a corresponding

semiconductor chip of a corresponding layer,

wherein a first redistribution layer is disposed on a first layer, among the two or more layers, and comprises a first-first wiring and a second-first wiring, and

wherein a second redistribution layer is disposed on a second layer, among the two or more layers, and comprises a second through via penetrating the second layer to connect one of the first-first wiring and the second-first wiring in the first redistribution layer to a second-second wiring included in the second redistribution layer.