26. A semiconductor package, comprising:

a first package substrate having a first side and a second side, the first side opposite the second side, the first package substrate comprising:

a layer comprising a semiconductor material;

a first ground interconnect structure between the first side and the second side of the first package substrate;

a second ground interconnect structure between the first side and the second side of the first package substrate;

a third ground interconnect structure between the first side and the second side of the first package substrate, wherein the first ground interconnect structure, the second ground interconnect structure and the third ground interconnect structure extend through the layer comprising the semiconductor material; and

a ball pad on the second side of the first package substrate, the ball pad comprising copper, wherein the first ground interconnect structure, the second ground interconnect structure and the third ground interconnect structure are in contact with the ball pad; and

a die coupled to the first side of the first package substrate; and

a second package substrate coupled to the second side of the first package substrate.

27. The semiconductor package of claim 26, further comprising an additional ground interconnect structure between the first side and the second side of the first package substrate, the additional ground interconnect structure through the layer comprising the semiconductor material, and the additional ground interconnect structure in contact with the ball pad.

28. A semiconductor package, comprising:

a first package substrate having a first side and a second side, the first side opposite the second side, the first package substrate comprising:

a first package substrate layer comprising a semiconductor material;

a first ball pad on the second side of the first package substrate, the first ball pad comprising copper;

a first interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the first interconnect structure being at least partially directly over the first ball pad of the first package substrate, the first interconnect structure being in electrical contact with the first ball pad;

a second interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the second interconnect structure being at least partially directly over the first ball pad of the first package substrate, the second interconnect structure being spaced laterally from the first interconnect structure, the second interconnect structure being in electrical contact with the first ball pad of the first package substrate;

a third interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the third interconnect structure being at least partially directly over the first ball pad of the first package substrate, the third interconnect structure being spaced laterally from the first interconnect structure and being spaced laterally from the second interconnect structure, the third interconnect structure being in electrical contact with the first ball pad of the first package substrate;

a second ball pad on the second side of the first package substrate, the second ball pad comprising copper;

a fourth interconnect structure between the first side and the second side of the first package substrate and through the first package substrate layer, the fourth interconnect structure being at least partially directly over the second ball pad of the first package substrate, the fourth interconnect structure being in electrical contact with the second ball pad of the first package substrate;

a die coupled to the first side of the first package substrate; and

a second package substrate coupled to the second side of the first package substrate.

29. The semiconductor package of claim 28, wherein there are fewer interconnect structures between the first side and the second side of the first package substrate and through the first package substrate layer that are at least partially directly over the second ball pad than there are interconnect structures between the first side and the second side of the first package substrate and through the first package substrate layer that are at least partially directly over the first ball pad.

30. The semiconductor package of claim 28, the first package substrate further comprising a second package substrate layer.

31. The semiconductor package of claim 30, the first package substrate further comprising:

a fifth interconnect structure between the first side and the second side of the first package substrate and through the second package substrate layer, the fifth interconnect structure being directly over the first interconnect structure and being in electrical contact with the first interconnect structure;

a sixth interconnect structure between the first side and the second side of the first package substrate and through the second package substrate layer, the sixth interconnect structure being directly over the second interconnect structure and being in electrical contact with the second interconnect structure; and

a seventh interconnect structure between the first side and the second side of the first package substrate and through the second package substrate layer, the seventh interconnect structure being directly over the third interconnect structure and being in electrical contact with the third interconnect structure.

32. The semiconductor package of claim 28, the first interconnect structure, the second interconnect structure, and the third interconnect structure all being in direct contact with the first ball pad.