

1.153.051



# PATENT SPECIFICATION

DRAWINGS ATTACHED

1.153.051

Date of Application and filing Complete Specification: 23 June, 1966.

No. 28061/66.

Application made in United States of America (No. 468,196) on 30 June, 1965.

Complete Specification Published: 21 May, 1969.

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Index at acceptance:—H1 K(211, 217, 221, 22Y, 223, 312, 353, 36Y, 37Y, 373, 41Y, 413, 415, 422, 426, 459, 469, 511, 51Y, 520, 521, 52Y, 530, 54Y, 563, 578, 579, 581, 583, 60Y, 61Y, 611, 618, 619, 615, 62Y, 622, 650)

Int. Cl.:—H 01 I 7/00

## COMPLETE SPECIFICATION

### Electrical Isolation of Semiconductor Circuit Components

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organised according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices, both discrete devices and integrated networks of the type having interconnected circuit components attached to a common support but yet electrically isolated from each other, and to methods of manufacture useful in fabricating said devices.

According to one aspect of the present invention a plurality of electrical circuit components are formed at spaced locations adjacent to one surface of a body of semiconductor material having an opposite surface disposed on and attached to an insulating layer; electrical interconnections are provided between the circuit components, and the semiconductor body is then etched through to the insulating layer to leave regions containing the circuit components as islands attached to the insulating layer and electrically isolated from each other. In a preferred embodiment, the electrical interconnections are positioned on a further insulating layer on the said one surface of the semiconductor body, contact being made with the components through the further insulating layer, and the etching step is effective to remove parts of the further insulating layer as well as parts of the semiconductor body. The insulating layer to which the components are attached is preferably formed on a substrate, e.g. a body of polycrystalline semiconductor material. Formation of the components in a single body of semiconductor material assists in ease of production and the

subsequent electrical isolation by removal of material to separate the components provides electrical isolation between the components such that the capacitance associated with the isolation permits operation of the resultant network at high frequencies and for fast switching operations.

An integrated electrical network structure according to the invention has a plurality of discrete regions of semiconductor material attached to and upstanding from an insulating layer on a surface of a support body of semiconductor material, at least two of the regions being surrounded by an open channel which provides electrical isolation between those two regions. Each of the two regions includes an electrical circuit component formed adjacent the surface of the region opposite that attached to the insulating layer and those opposite surfaces are covered by respective coatings of insulating material. An ohmic interconnection between the two said components bridges the open channel and extends along the said insulating coatings on the regions containing the components.

The invention is also useful in production of a semiconductor device, e.g. a transistor, and comprises forming an electrical circuit component adjacent to a portion of one surface of a body of semiconductor material having an opposite surface disposed on and attached to an insulating layer, which may be formed on a surface of a support member. A region of the semiconductor body is then etched through to the insulating layer to leave the an island containing component attached to the insulating layer and electrically isolated from the remainder of the semiconductor body. In a preferred embodiment, the remainder of the semiconductor body completely surrounds the region containing the circuit component, being spaced and electrically isolated therefrom by the open chan-

nel. The surfaces of the region containing the component and of the remainder of the body opposite those attached to the insulating layer can be covered with a coating of insulating material and one or more electrical leads can be ohmically connected to the component through the coating, the or each lead bridging the channel, extending along or being supported by the insulating coatings on the region containing the component and the remainder of the semiconductor body.

By way of example, the invention will be described in greater detail with reference to the accompanying drawings, in which:—

Figures 1—4 are pictorial views in section of a semiconductor slice in the early stages of the production of an integrated circuit;

Figure 5 represents a pictorial view of a small segment of the slice shown in Figures 1—4;

Figures 6 and 7 are sectional views of a portion of the segment of Figure 5 taken along the line 6—6 showing subsequent steps of the production process;

Figure 8 is a pictorial view of the completed device described with reference to Figures 1—7 before the individual interconnected circuit components have been electrically isolated from each other;

Figure 9 is a pictorial view of the completed device shown in Figure 8 after an electrical isolation step has been completed;

Figure 10 is a sectional view of a portion of the completed circuit shown in Figure 9 taken along the line 10—10;

Figure 11 is a schematic diagram of the integrated circuit contained within the segment shown in Figure 8; and

Figure 12 is a pictorial view in section showing the fabrication of a single high frequency transistor according to this invention.

Referring now to Figure 1 there is described the first step in this invention. A slice 10 of single crystal low-resistivity N+ semiconductor material, such as silicon, having a resistivity of perhaps 0.010 to 0.025 ohms per centimeter is used as the starting material. This slice may be about one inch in diameter and approximately 10 mils thick. The top and bottom surfaces of the slice 10 are covered with insulating coatings 11 and 12, which may be silicon oxide, for example, these coatings being formed by any conventional technique to thicknesses of perhaps 10,000 Å. For instance, the oxide coatings 11 and 12 may be thermally grown by exposing the slice 10 to steam at about 1200°C for a sufficient period of time. An alternative method of forming the oxide layers 11 and 12, however, would be the "oxidative" technique, by which oxygen and tetraethoxysilane are reacted in vapor form at 250—500°C in the presence of the wafer 10. The reaction mixture is obtained by bubbling oxygen through liquid tetraethoxysilane at room temperature, then com-

binning the gaseous mixture with excess oxygen and passing it into a furnace tube containing the slice 10 where the oxidation takes place. The silicon oxide thereby produced is deposited upon the upper and lower surfaces or faces of the slice 10. The advantage of this latter process is the relatively low temperatures at which uniform oxide coatings may be formed.

As the next step in the invention, as depicted in Figure 2, the oxide coated wafer 10 is placed in a reactor to produce the top layer 13 which eventually becomes the substrate. Within the reactor a layer 13 of semiconductor material is vapor deposited over the top surface of the oxide coated slice 10. The most common method of vapor deposition is by the hydrogen reduction of silicon tetrachloride, a technique well known in the art and requiring no elaboration here. The conductivity type of the layer 13 may be N-type, P-type or intrinsic, and the actual crystal orientation of the semiconductor layer 13 is not critical since its primary function is that of a support or base upon which the various integrated circuit components are formed. Due to the fact that the layer 13 is being deposited upon the oxide coating 11, however, the layer would in most probability be either polycrystalline or amorphous, instead of monocrystalline. The thickness of the layer 13 should be perhaps seven or eight mils or more to facilitate handling the unit without breakage. The structure of Figure 2 is then subjected to a lapping and polishing operation, for example in order to remove the oxide layer 12 and substantially all of the low-resistivity N+ semiconductor material 10 except for a thin portion having a thickness of approximately one mil. The lapped and polished structure is then rotated through 180°, the resulting structure depicted in Figure 3, whereby the layer 13 now forms the substrate, the low-resistivity semiconducting material 10 being separated from said substrate by the oxide layer 11.

As the next step in the process, the structure of Figure 3 is subjected to an epitaxial deposition step whereby, as shown in Figure 4, a layer 14 of high-resistivity N-type semiconducting material will be deposited upon the low-resistivity layer 10. The high-resistivity layer 14 now serves as a region into which subsequent diffusions or upon which epitaxial depositions may be made in order to fabricate various components of an integrated circuit.

In accordance with this objective, reference is made to Figure 5 where a small segment of the slice shown in Figure 4 is represented as a chip or wafer 20 which represents the segment occupied by one integrated circuit. Actually the slice would contain in undivided form dozens or even hundreds of the segments such as the wafer 20. An oxide layer 15, for example silicon oxide, is formed over the

top of the wafer segment 20 so as to completely cover the high-resistivity layer 14. Through the use of photographic masking and etching techniques known in the art, selected portions of the oxide layer 15 are removed in the patterns 30—34 shown in Figure 5 so as to expose corresponding portions of the high-resistivity region 14 under the oxide layer 15. A cross-sectional view through a portion of the wafer 20 is pictured in Figure 6. It is to be observed that the exposed portions of the high-resistivity substrate 14 are the regions into which subsequent diffusions are to be made in order to fabricate the various components of an integrated circuit.

Referring now to Figure 7, a sectional view of a portion of a completed integrated circuit is seen, with an NPN transistor  $T_1$  and a resistor  $R_1$  having been formed in the N-type layer by diffusion. A P-type diffused region provides the base of the transistor, while an elongated P-type region formed simultaneously with the base provides the resistor  $R_1$ . An N-type diffused region provides the transistor  $T_1$  emitter. The diffusion operation utilizes silicon oxide masking so that the oxide layer 15 acquires a stepped configuration in the final device. Openings are made in the oxide where electrical contact is necessary, then metal film is deposited over the oxide and selectively removed to provide the desired contacts and interconnections. The lead interconnection 21 connects the base of the transistor  $T_1$  to one end of the resistor  $R_1$ , and the metal regions 25 and 26 form the emitter and collector leads respectively. In order to make a low resistance contact to the collector region of the transistor  $T_1$ , it may be desirable to first form a low resistance  $N^+$  region in layer 14 by diffusion at the location where the lead 26 is to make ohmic contact.

The formation of the leads or interconnections 21, 25 and 26, for example, may be accomplished by any conventional technique known in the art such as vacuum evaporation, and the leads themselves may be formed of any appropriate material. In accordance with a preferred embodiment, however, it is desirable to use materials for the leads or interconnections which do not tend to degrade the semiconductor device by their presence, which lend themselves to manufacturing techniques compatible with other processes used on the devices, and which permit working with very small geometries. In the specific case of silicon devices, the objects are to provide a contact and interconnection arrangement which adheres well to silicon and to silicon oxide surfaces without reacting unfavorably with either, which can be used with available photoresist masking and etching procedures, which forms an ohmic and low resistance electrical connection to the silicon, which can be applied readily by metal evaporation techniques, which have a high conductivity, and which can be bonded with gold wires. A com-

bination of metals almost uniquely commensurate with the above objectives is found to be molybdenum and gold. Accordingly, a thin film of molybdenum is first applied over the entire face of the silicon wafer 20 having the silicon oxide coating 15 with the openings etched in the contact areas. Then the molybdenum is covered with a thin film of gold and thereafter the gold and molybdenum are etched away in the unwanted areas leaving the desired pattern of contacts and interconnections 21, 25 and 26 on the silicon surface and on the oxide.

A top view of the wafer 20 is shown in Figure 8 after the individual circuit components have been formed, and the leads and interconnections have been deposited in their desired locations. At this stage of production the individual circuit components are formed within the wafer 20 but are not electrically isolated from each other.

The electrical isolation of each of the components from each other is accomplished by forming a series of channels or moats completely surrounding each of the components, as depicted in Figure 9. The various leads between the components then cross over the channels in order to make the desired interconnections.

The formation of the moats or channels can be achieved by a photographic masking and etching technique to be described with reference to Figure 10, a sectional view of a portion of the wafer 20 through the channel regions 35 and 36. A layer of photoresist material of the type disclosed in U.S. patents 2,670,285; 2,670,286 and 2,670,287 of L. M. Minsk, or of the type available from the Eastman Kodak Company under the trade name "KMER" or "KTFR", preferably the latter, is coated over the top surface of the slice 20. A photomask is then placed upon the photoresist to mask the regions where the moats or channels are to be formed, and the unmasked portions of the photoresist are then exposed and developed by photographic means. The top surface of the slice 20 is then subjected to etchants which selectively remove the oxide layer 15 and the underlying silicon layers 14 and 10 in the previously masked regions down to the oxide layer 11 leaving the leads and interconnections intact and forming the channel areas 35 and 36, for example, as shown in Figure 10. The interconnections are sufficiently narrow for the etchant to undercut them completely so they are left bridging the channel areas 35 and 36, for example.

The particular etchants used should be of the type that will not attack the leads and interconnections. For example, an integrated circuit structure was fabricated as described with the leads or interconnections formed of molybdenum and gold. After the wafer with the components formed therein was coated with photoresist and masked as described, the top surface of the wafer 20 was subjected to an

ammonium monohydrogen fluoride ( $\text{NH}_4\text{HF}_2$ ) chemical etchant which selectively removed portions of the silicon oxide layer 15 beneath the leads 21 and 26 (the extent of the removal represented by the dotted line 15A) while leaving the underlying silicon material substantially unaffected. The masked surface of the wafer was then subjected to a chemical etchant composed of a mixture of nitric, hydrofluoric, and acetic acids which selectively removed portions of the silicon layers 14 and 10 beneath the dotted lines 15A as shown while leaving the unremoved portion of the silicon oxide layer 15 and the silicon oxide layer 11 substantially unaffected.

The resulting structure is shown in Figure 10 whereby the components  $T_1$  and  $R_1$ , for example, are electrically isolated from each other by the moat or channel 36 and the oxide layer 11, and the lead or interconnection 21 bridges the gap between these components. With ordinary metal deposition techniques being used, the lead 21 was unaffected by the etching operation and was found to be quite strong, even through it bridged the moat 36. The bridged leads withstood further processing steps, such as spraying the structure with alcohol at high pressure in order to remove the photoresist used for the masking operation, without failure, i.e., without breakage of the cantilevered or bridged leads. If desired, it is possible to increase the thickness of the cantilevered leads by electroplating gold, for example, through an appropriate mask. KMFR for example, thereby improving the lead strength. As a result of the above-described process, the completed unit is seen in Figure 9 with the transistors  $T_1$  and  $T_2$  and the resistors  $R_1$ ,  $R_2$ , and  $R_3$  completely isolated from each other through the wafer 20, the metal film interconnections providing a logic circuit as shown in schematic form in Figure 11.

While the invention has been described with reference to a specific method and embodiment, it is to be understood that this description is not to be construed in a limiting sense. The basic concept which has been described so far is the isolation of individual interconnected circuit components through the substrate in which they have been formed by etching away selected portions of the material between the components with chemical etchants that leave the interconnections substantially unaffected. Any techniques or etchants that accomplish this objective besides those specifically described above are also encompassed by this invention.

In addition to the specific integrated circuit structures that have been described, it is obvious that using the process of this invention, a multitude of configuration of circuit components may be formed within a single substrate. For example, in addition to forming transistors, diodes and resistors, other com-

ponents like metal oxide semiconductor devices, field effect transistors, and oxide dielectric capacitors may be fabricated, interconnected to perform desired circuit functions, and then electrically isolated from each other according to this invention. Similarly, although the initial starting slice was described as low resistivity N+ semiconductor material, high resistivity and/or P-type material may also be employed.

The above described process, although particularly useful in the field of integrated circuits, is also useful in the fabrication of single devices mounted upon an insulating substrate. In accordance with the latter objective, reference is made to Figure 12 wherein there is depicted an NPN transistor 40 comprising an N-type collector layer 44, a P-type diffused base region 45, and an N-type diffused emitter region 46. The transistor 40 is formed upon the semiconductor substrate 41 separated therefrom by the oxide layer 42 in substantially the same manner as the process described for the transistor  $T_1$ , for example, with reference to Figures 1—11. This process leaves an oxide coating 57 upon the top surface of the wafer, the coating being in a stepped configuration due to the use of silicon oxide masking during successive diffusion operations. For high frequency applications, the geometry of the active part of the transistor 40 is extremely small, the emitter region 46 being only a few hundredths of a square mil in area in some cases.

The collector, base, and emitter contacts to this transistor are provided by metal strips 51, 56, and 48 respectively, which extend into holes etched in the oxide coating 57 to make ohmic contact to the appropriate regions. The strips terminate respectively in enlarged bonding pads 52, 55 and 49.

This expanded contact arrangement is necessary to high frequency devices because of the previously mentioned extremely small size of the active regions of the transistor 40. If the contacts are no larger than the active regions, it is virtually impossible to bond external lead wires to these contacts, and so the expanded thin strips (for making contact to the active regions) with the enlarged bonding pads (for external connections) are needed. There is necessarily associated with this expanded contact arrangement, however, a capacitance, due to the fact that the expanded contacts extend over the oxide layer 57 (which acts as a dielectric layer), this capacitance causing undesirable coupling at high frequencies.

To reduce these capacitive effects, the channel or moat 47 is etched completely around the active portions of the transistor 40, as shown in Figure 12, thereby isolating the active regions from the bonding pads and substantial portions of the elongated metal strips. The formation of the moat or channel 47 is

accomplished in the same manner as previously described with reference to Figures 9 and 10. As a consequence, a small geometry high frequency transistor 40 is provided having thin film continuous metallic leads from the various active regions to the respective bonding pads, while at the same time reducing the coupling capacitance associated with such an arrangement. To even further reduce any coupling capacitance, channels or moats may also be formed in like manner completely surrounding each of the bonding pads so as to isolate these pads from each other.

Various other modifications of the disclosed embodiments as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

Copending Patent Application No. 53245/68 (Serial No. 1,153,052) claims a method of manufacturing a semiconductor device in which a body of semiconductor material having first and second insulating layers formed on opposite surfaces of the body has a limited area of the first insulating layer opened to expose the semiconductor body and the exposed semiconductor body is then etched to form a cavity in the body which extends to the second insulating layer.

#### WHAT WE CLAIM IS:—

1. A method of manufacture comprising forming an electrical circuit component adjacent to a portion of one surface of a body of monocrystalline semiconductor material having an opposite surface disposed on and attached to an insulating layer, and then etching a region of the semiconductor body through to the insulating layer to leave an island containing the component attached to the insulating layer and electrically isolated from the remainder of the semiconductor body.

2. A method of manufacture comprising forming electrical circuit components at spaced locations of a body of monocrystalline semiconductor material adjacent to one surface thereof and providing electrical interconnections between the components, and etching the semiconductor body around the regions containing the said components through to an insulating layer on and attached to an opposite surface of the body to leave the said regions as mutually spaced islands attached to the insulating layer and electrically isolated from each other.

3. A method according to Claim 2, the said electrical interconnection being positioned on a further insulating layer on the said one surface of the semiconductor body and making contact with the components through the further insulating layer, in which the etching step also removes parts of the further insulating layer.

4. A method according to Claim 3, in which the etching step is a two-step process

comprising a first step using an etchant which attacks the further insulating layer but does not attack the said interconnections, and a second step using an etchant which attacks the semiconductor body and not the first-mentioned insulating layer or the said interconnections.

5. A method according to any one of Claims 2—4, the insulating layer on the said opposite surface of the semiconductor body being attached to a support member.

6. A method according to Claim 1 or Claim 2, the semiconductor body comprising a low resistivity region defining the said opposite surface of the body and a higher resistivity region in which the or each circuit component is formed.

7. A method of fabricating an integrated semiconductor network comprising the steps of:

a) forming a composite structure comprising an insulating layer disposed between and attached to one major surface of a wafer of low resistivity monocrystalline semiconductor material and a surface of a support member,

b) forming a layer of higher resistivity monocrystalline semiconductor material upon the other major face of the said wafer, c) forming individual circuit components in the layer of higher resistivity semiconductor material,

d) applying electrical interconnections to connect selected circuit components together,

e) etching around each interconnected component and under the interconnections to remove selected portions of the higher resistivity material and of the low resistivity wafer between the interconnected components to form a channel surrounding each component and extending to the said insulating layer leaving the said interconnected components electrically isolated from each other by the channel and the insulating layer.

8. A method according to Claim 7, in which the said step c) is effected by covering the layer of higher resistivity material with a coating of insulating material and diffusing impurities into the higher resistivity layer using the said coating as a diffusion mask, and in which the said step (d) comprises depositing the electrical interconnections on the insulating coating to contact the interconnected components through the insulating coating.

9. A method according to any one of Claims 2—8, in which at least one of the components is an active component and at least one other component is a passive component.

10. A method according to Claim 1, in which the circuit component is formed by coating the said one surface of the semiconductor body with an insulating material and diffusing impurity material into that surface using



5 accomplished in the same manner as previously described with reference to Figures 9 and 10. As a consequence, a small geometry high frequency transistor 40 is provided having thin film continuous metallic leads from the various active regions to the respective bonding pads, while at the same time reducing the coupling capacitance associated with such an arrangement. To even further reduce any coupling capacitance, channels or moats may also be formed in like manner completely surrounding each of the bonding pads so as to isolate these pads from each other.

10 Various other modifications of the disclosed embodiments as well as other embodiments of the invention, may become apparent to persons skilled in the art without departing from the scope of the invention as defined by the appended claims.

20 Copending Patent Application No. 53245/68 (Serial No. 1,153,052) claims a method of manufacturing a semiconductor device in which a body of semiconductor material having first and second insulating layers formed on opposite surfaces of the body has a limited area of the first insulating layer opened to expose the semiconductor body and the exposed semiconductor body is then etched to form a cavity in the body which extends to the second insulating layer.

#### WHAT WE CLAIM IS:—

1. A method of manufacture comprising forming an electrical circuit component adjacent to a portion of one surface of a body of monocrystalline semiconductor material having an opposite surface disposed on and attached to an insulating layer, and then etching a region of the semiconductor body through to the insulating layer to leave an island containing the component attached to the insulating layer and electrically isolated from the remainder of the semiconductor body.

2. A method of manufacture comprising forming electrical circuit components at spaced locations of a body of monocrystalline semiconductor material adjacent to one surface thereof and providing electrical interconnections between the components, and etching the semiconductor body around the regions containing the said components through to an insulating layer on and attached to an opposite surface of the body to leave the said regions as mutually spaced islands attached to the insulating layer and electrically isolated from each other.

3. A method according to Claim 2, the said electrical interconnection being positioned on a further insulating layer on the said one surface of the semiconductor body and making contact with the components through the further insulating layer, in which the etching step also removes parts of the further insulating layer.

4. A method according to Claim 3, in which the etching step is a two-step process

comprising a first step using an etchant which attacks the further insulating layer but does not attack the said interconnections, and a second step using an etchant which attacks the semiconductor body and not the first-mentioned insulating layer or the said interconnections.

5. A method according to any one of Claims 2—4, the insulating layer on the said opposite surface of the semiconductor body being attached to a support member.

6. A method according to Claim 1 or Claim 2, the semiconductor body comprising a low resistivity region defining the said opposite surface of the body and a higher resistivity region in which the or each circuit component is formed.

7. A method of fabricating an integrated semiconductor network comprising the steps of:

a) forming a composite structure comprising an insulating layer disposed between and attached to one major surface of a wafer of low resistivity monocrystalline semiconductor material and a surface of a support member,

b) forming a layer of higher resistivity monocrystalline semiconductor material upon the other major face of the said wafer, c) forming individual circuit components in the layer of higher resistivity semiconductor material,

d) applying electrical interconnections to connect selected circuit components together,

e) etching around each interconnected component and under the interconnections to remove selected portions of the higher resistivity material and of the low resistivity wafer between the interconnected components to form a channel surrounding each component and extending to the said insulating layer leaving the said interconnected components electrically isolated from each other by the channel and the insulating layer.

8. A method according to Claim 7, in which the said step c) is effected by covering the layer of higher resistivity material with a coating of insulating material and diffusing impurities into the higher resistivity layer using the said coating as a diffusion mask, and in which the said step (d) comprises depositing the electrical interconnections on the insulating coating to contact the interconnected components through the insulating coating.

9. A method according to any one of Claims 2—8, in which at least one of the components is an active component and at least one other component is a passive component.

10. A method according to Claim 1, in which the circuit component is formed by coating the said one surface of the semiconductor body with an insulating material and diffusing impurity material into that surface using

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- the said coating as a diffusion mask, an electrical lead is formed on the said insulating coating making ohmic contact with the component through the coating and extending along the coating to a location on the body laterally spaced from the component, and in which the etching step removes a region of the said coating and of the underlying body material between the component and the said spaced location to form a channel bridged by the electrical lead and which electrically isolates the component from the remainder of the body.
11. A method according to Claim 10, in which the circuit component is a transistor having electrical leads to its base, emitter and collector regions extending along the insulating coating to locations spaced laterally from the transistor, the electrical leads bridging the said channel.
12. A method according to Claim 10 or Claim 11, the semiconductor body comprising a layer of low resistivity material attached to the said insulating layer and a layer of higher resistivity material in which the said component is formed.
13. A method according to any one of Claims 10—12, the said insulating layer being attached to a support member.
14. A method according to any one of Claims 5, 7, 8 and 13, in which the support member is formed by deposition of polycrystalline semiconductor material on the insulating layer.
15. A method according to any one of the preceding claims, the insulating material being silicon oxide.
16. A method according to any one of the preceding claims, the semiconductor material being silicon.
17. A method of fabricating an integrated electrical network, substantially as described herein with reference to and as illustrated by Figs. 1—11 of the accompanying drawings.
18. A method of fabricating a semiconductor device, substantially as described herein with reference to and as illustrated by Fig. 12 of the accompanying drawings.
19. The product of a method according to any one of the preceding claims.
20. An integrated electrical network structure comprising a plurality of discrete regions of monocrystalline semiconductor material attached to and upstanding from an insulating layer on a surface of a support body of semiconductor material, at least two of the said regions being surrounded by an open channel which provides electrical isolation between those two regions, each of the said two regions having an electrical circuit component formed adjacent to the surface of the region opposite that attached to the insulating layer, the said opposite surfaces being covered by respective coatings of insulating material, and an ohmic interconnection between the two said components, which interconnection bridges the channel and extends along the said insulating coatings on the regions containing those components.
21. A structure according to Claim 20, in which one of the said components is a transistor and the other is a resistor.
22. A semiconductor device comprising a discrete region of semiconductor material attached to and upstanding from an insulating layer on a surface of a support body of semiconductor material, a body of semiconductor material attached to the said insulating layer and surrounding the said region, the region and the body being spaced by an open channel surrounding the region which provides electrical isolation between the region and the body, coatings of insulating material on the surfaces of the body and the region opposite the surfaces attached to the insulating layer, an electrical circuit component formed in the region under the insulating coating, and at least one electrical lead making ohmic contact with the component through the insulating coating thereon, the electrical lead bridging the channel and extending along the insulating coatings on the region and the body.
23. A structure or device according to any one of Claims 20—22, in which the semiconductor material is silicon, the insulating material is silicon oxide, and the support body is polycrystalline.

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