CLAIMS

~~**WHAT IS CLAIMED IS:**~~

1.~~——~~ A bias generation circuit, comprising:

a bias voltage generator, including:

a main NMOS transistor having a drain and a gate of the main NMOS transistor both coupled to a first terminal;

a main resistor having a first main resistor terminal and a second main resistor terminal, wherein the first main resistor terminal couples to a source of the main NMOS transistor; and

a main PMOS transistor having a source of the main PMOS transistor coupled to the second main resistor terminal and a drain and a gate of the main PMOS transistor both coupled to a second terminal, wherein the second terminal couples to a main ground; and

an array of sensors coupled to the first terminal and the second terminal~~.~~

~~2. The bias generation circuit of claim 1, wherein the bias voltage generator is configured to generate a first bias voltage at the first terminal and a second bias voltage at the second terminal.~~

~~3. The bias generation circuit of claim 1 further comprising a main current mirror coupled to the bias voltage generator, wherein the main current mirror comprises a second main PMOS transistor mirroring a current from a current source, wherein the second main PMOS transistor is configured to have a source of the second main PMOS transistor coupled to a main supply voltage, a gate of the second main PMOS transistor coupled to the current source, and a drain of the second main PMOS transistor coupled to the first terminal.~~

~~4. The bias generation circuit of claim 1~~, wherein each sensor of the array of sensors comprises a local bias replica coupled to the first terminal and the second terminal~~.~~

~~5. The bias generation circuit of claim 4,~~ and wherein the local bias replica comprises:

a local NMOS transistor having a gate of the local NMOS transistor coupled to the first terminal;

a local resistor having a first local resistor terminal and a second local resistor terminal, wherein the first local resistor terminal couples to a source of the local NMOS transistor; and

a local PMOS transistor having a source of the local PMOS transistor coupled to the second local resistor terminal, a gate of the local PMOS transistor coupled to the second terminal, and a drain of the local PMOS transistor coupled to a local ground.

~~6.~~ 2. The bias generation circuit of claim ~~5~~1, wherein the bias voltage generator is configured to generate a first bias voltage at the first terminal and a second bias voltage at the second terminal.

3. The bias generation circuit of claim 1 further comprising a main current mirror coupled to the bias voltage generator, wherein the main current mirror comprises a second main PMOS transistor mirroring a current from a current source, wherein the second main PMOS transistor is configured to have a source of the second main PMOS transistor coupled to a main supply voltage, a gate of the second main PMOS transistor coupled to the current source, and a drain of the second main PMOS transistor coupled to the first terminal.

4. The bias generation circuit of claim 1, wherein each sensor of the array of sensors further comprises a local current mirror mirroring a current of the local bias replica.

~~7.~~ 5. The bias generation circuit of claim ~~6~~4, wherein the local current mirror is configured to provide a bias current to a sensing circuit.

~~8.~~ 6. The bias generation circuit of claim ~~6~~4, wherein the local current mirror comprises a second local PMOS transistor having a source of the second local PMOS transistor coupled to a local supply voltage and a gate and a drain of the second local PMOS transistor both coupled to a drain of the local NMOS transistor.

~~9.~~ 7. The bias generation circuit of claim ~~5~~1, wherein the local ground and the main ground are configured to be electrically coupled through a ground interconnect.

~~10.~~ 8. The bias generation circuit of claim ~~5~~1, wherein the local resistor has a resistance value that is about k time a resistance value of the main resistor, wherein k is a positive number.

~~11.~~ 9. The bias generation circuit of claim ~~10~~8, wherein the local NMOS transistor and the local PMOS transistor are sized to mirror a current that is substantially 1/k times a current flowing through the bias voltage generator.

~~12.~~ 10. The bias generation circuit of claim ~~11~~9, wherein the main NMOS transistor has a same channel length as the local NMOS transistor and wherein the main NMOS transistor has a width that is substantially k times a width of the local NMOS transistor.

~~13.~~ 11. The bias generation circuit of claim ~~11~~9, wherein the main PMOS transistor has a same channel length as the local PMOS transistor and wherein the main PMOS transistor has a width that is substantially k times a width of the local PMOS transistor.

~~14.~~ 12. The bias generation circuit of claim ~~4~~1, wherein the local bias replica for each sensor of the array of sensors is substantially the same.

~~15.~~ 13. The bias generation circuit of claim 1, wherein the array of sensors is an array of fingerprint sensors or touch sensors.

~~16.~~ 14. The bias generation circuit of claim 1, wherein the bias voltage generator is at a periphery of the array of sensors.

~~17.~~ 15. A method, comprising:
providing a current source;
generating a first bias voltage at a first terminal and a second bias voltage at a second terminal by a bias voltage generator having a main PMOS transistor, a main NMOS transistor, and a main resistor serially coupled, wherein
a drain and a gate of the main NMOS transistor both coupled to the first terminal;
a first main resistor terminal of the main resistor couples to a source of the main NMOS transistor; and

a source of the main PMOS coupled to a second main resistor terminal of the main resistor and a drain and a gate of the main PMOS transistor both coupled to the second terminal, wherein the second terminal couples to a main ground;

mirroring a current of the current source to the bias voltage generator; and

coupling an array of sensors to the first bias voltage and the second bias voltage~~.~~

~~18. The method of claim 17~~, wherein each sensor of the array of sensors comprises a local bias replica coupled to the first terminal and the second terminal~~.~~, and wherein the local bias replica comprises:

~~19. The method of claim 18, wherein the local bias replica comprises~~

a local NMOS transistor having a gate of the local NMOS transistor coupled to the first terminal;

a local resistor having a first local resistor terminal and a second local resistor terminal, wherein the first local resistor terminal couples to a source of the local NMOS transistor; and

a local PMOS transistor having a source of the local PMOS transistor coupled to the second local resistor terminal, a gate of the local PMOS transistor coupled to the second terminal, and a drain of the local PMOS transistor coupled to a local ground.

~~20.~~ 16. The method of claim ~~19~~15, wherein the local ground and the main ground are configured to be electrically coupled through a ground interconnect.

~~21.~~ 17. The method of claim ~~19~~15, wherein the local resistor has a resistance value that is k time a resistance value of the main resistor, wherein k is a positive number.

~~22.~~ 18. The method of claim ~~21~~17, wherein the main NMOS transistor has a same channel length as the local NMOS transistor and wherein the main NMOS transistor has a width that is substantially k times a width of the local NMOS transistor.

~~23.~~ 19. The method of claim ~~18~~15, wherein each sensor of the array of sensors further comprises a local current mirror mirroring a current of the local bias replica.

~~24.~~ 20. The method of claim ~~23~~19, wherein the local current mirror is configured to provide a bias current to a sensing circuit.

~~25.~~ 21. The method of claim ~~17~~15, wherein the array of sensors is an array of fingerprint sensors or touch sensors.