

Memory Cell Structure

ABSTRACT OF THE DISCLOSURE

A memory structure that reduces soft-errors for us in CMOS devices is provided. The memory cell layout utilizes transistors oriented such that the source-to-drain axis is parallel a shorted side of the memory cell. The dimensions of the memory cell are such that it has a longer side and a shorter side, wherein the longer side is preferably about twice as long as the shorter side. Such an arrangement uses a shorter well path to reduce the resistance between transistors and the well strap. The shorter well strap reduces the voltage during operation and soft errors.

(FIG. 1)