FIG.1

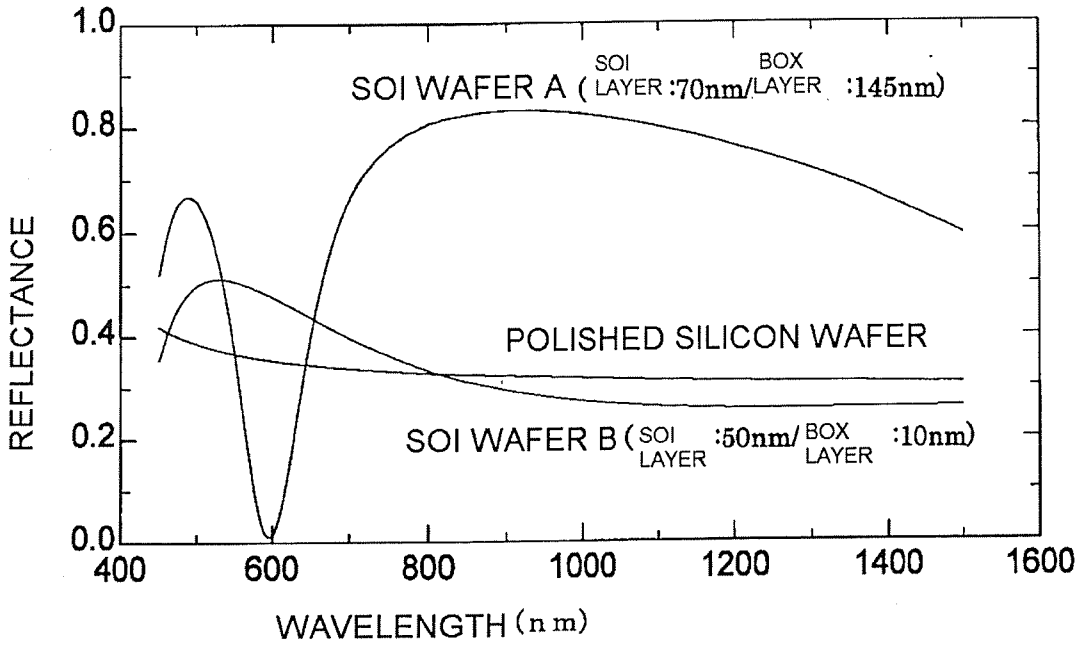

1.0
0.8
0.6
0.4
0.2
0.0
REFLECTANCE
400
600
800
1000
1200
1400
1600
WAVELENGTH (nm)
SOI WAFER A (SOI LAYER :70nm/BOX LAYER :145nm)
POLISHED SILICON WAFER
SOI WAFER B (SOI LAYER :50nm/BOX LAYER :10nm)

FIG.2

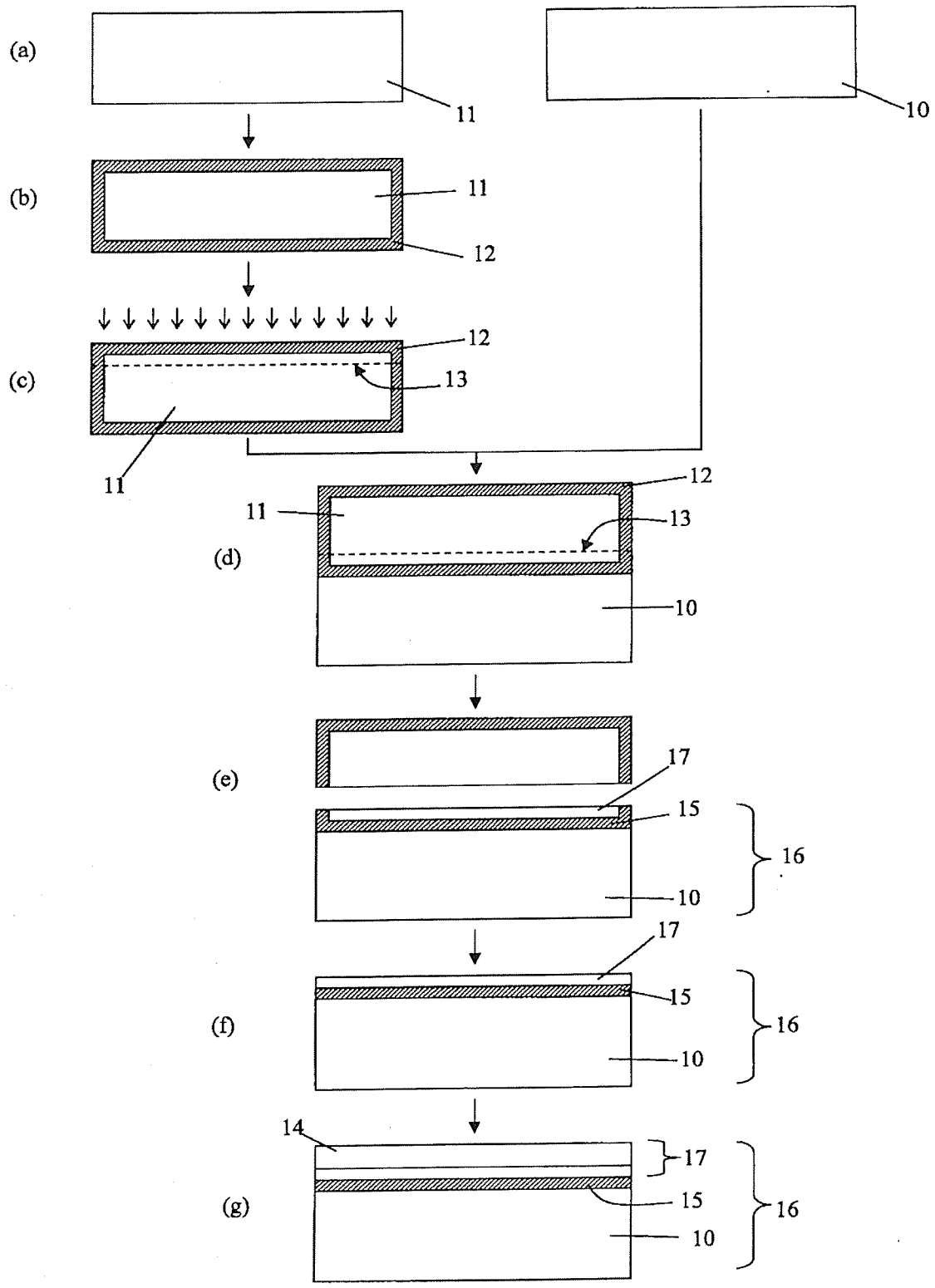

(a)
11
10
(b)
11
12
(c)
12
13
11
(d)
12
11
13
10
(e)
17
15
16
10
(f)
17
15
16
10
(g)
14
17
15
16
10

FIG.3

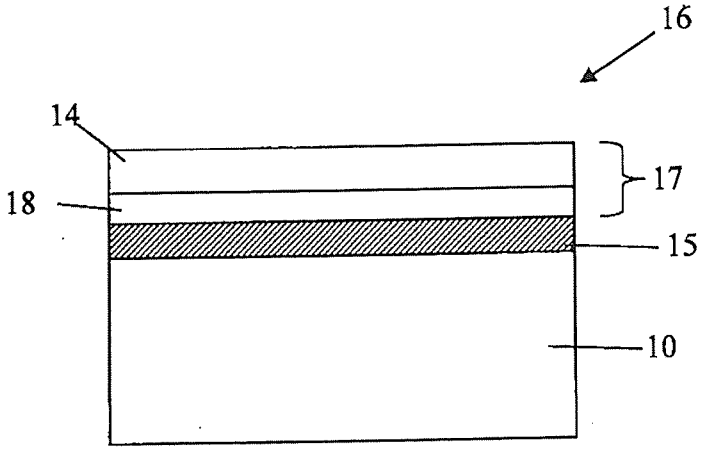


FIG.4

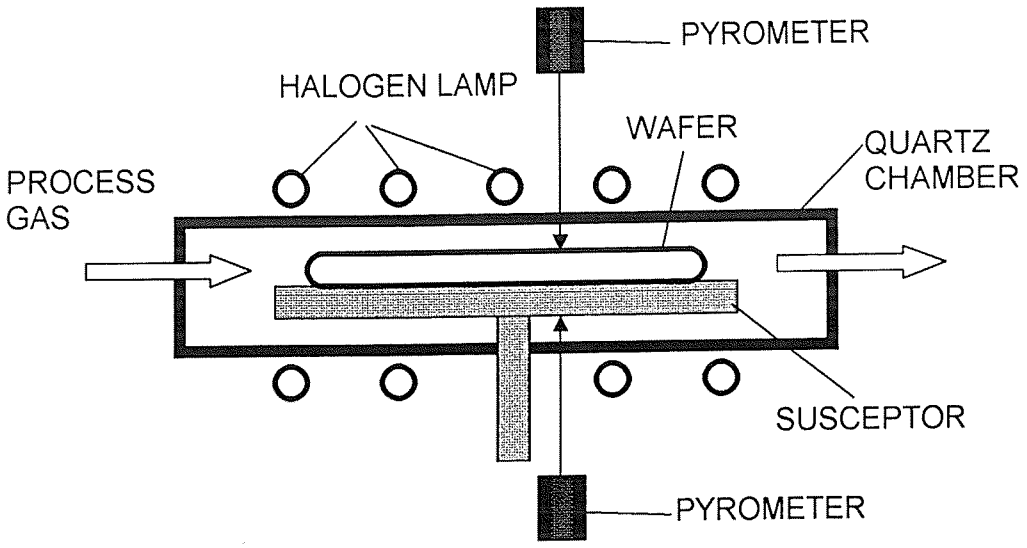

PYROMETER
HALOGEN LAMP
WAFER
QUARTZ CHAMBER
PROCESS GAS
SUSCEPTOR
PYROMETER

FIG.5

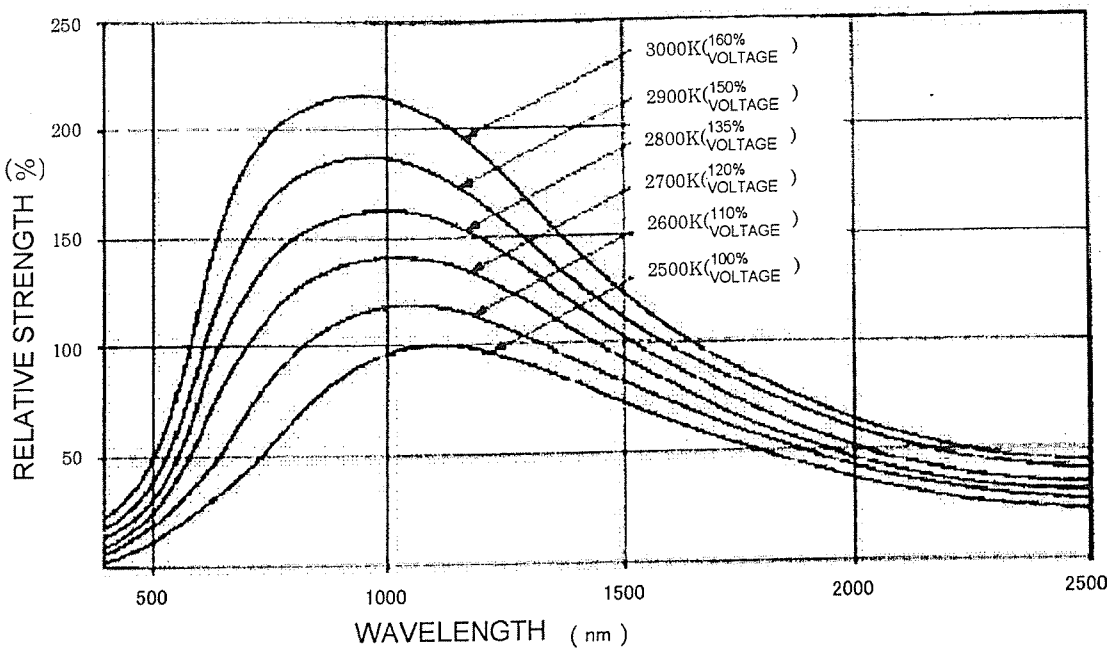

250
200
150
100
50
RELATIVE STRENGTH (%)
500
1000
1500
2000
2500
WAVELENGTH (nm)
3000K(160% VOLTAGE)
2900K(150% VOLTAGE)
2800K(135% VOLTAGE)
2700K(120% VOLTAGE)
2600K(110% VOLTAGE)
2500K(100% VOLTAGE)

FIG.6

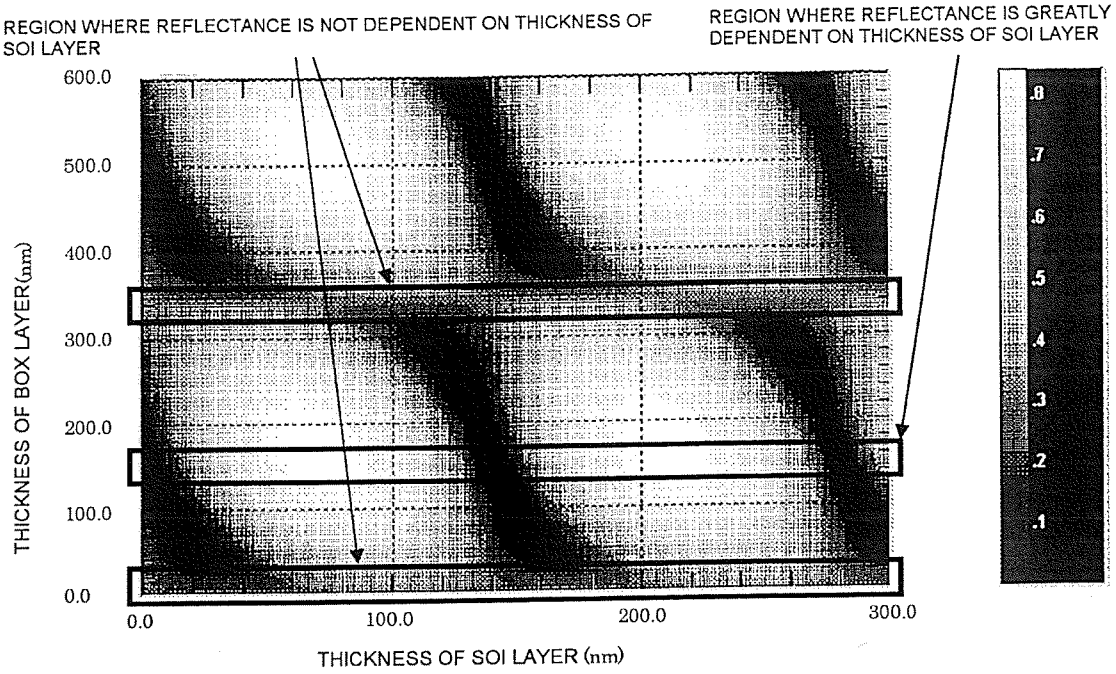

REGION WHERE REFLECTANCE IS NOT DEPENDENT ON THICKNESS OF SOI LAYER
REGION WHERE REFLECTANCE IS GREATLY DEPENDENT ON THICKNESS OF SOI LAYER
600.0
500.0
400.0
300.0
200.0
100.0
0.0
THICKNESS OF BOX LAYER(nm)
0.0
100.0
200.0
300.0
THICKNESS OF SOI LAYER (nm)
.8
.7
.6
.5
.4
.3
.2
.1

FIG.7

AFTER H_2 ANNEALING (1100°C, 900 SECONDS)

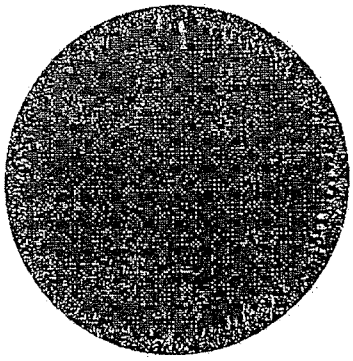
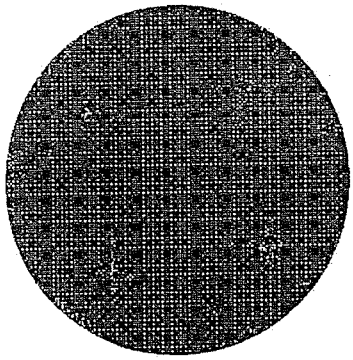
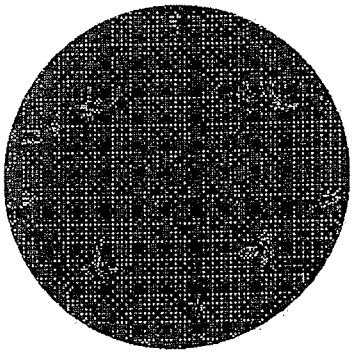
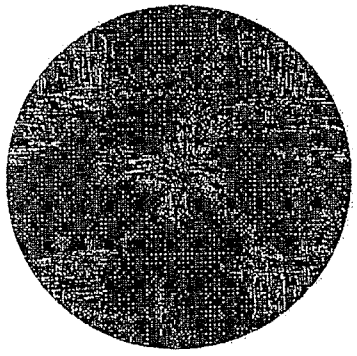
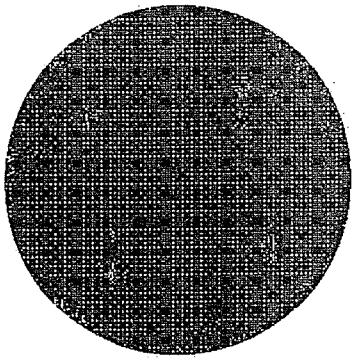
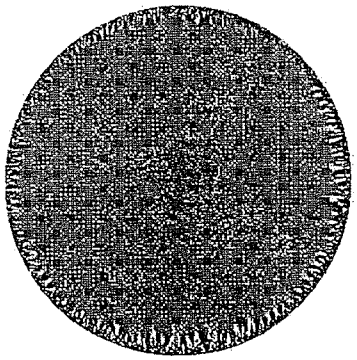
	POLISHED SILICON WAFER SLIP-FREE CONDITIONS	SOI WAFER A SLIP-FREE CONDITIONS
SOI WAFER A SOI LAYER : 70nm BOX LAYER : 145nm		
SOI WAFER B SOI LAYER : 50nm BOX LAYER : 10nm		

FIG.8

	AFTER H_2 ANNEALING	AFTER 5-mm EPITAXIAL GROWTH
SOI WAFER A SOI LAYER : 70nm BOX LAYER : 145nm		
SOI WAFER C SOI LAYER : 70nm BOX LAYER : 340nm	