(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

*G00002*

(43) International Publication Date
12 September 2002 (12.09.2002)

PCT

(10) International Publication Number
WO 02/071611 A3

(51) International Patent Classification[7]: H03K 19/096, H01L 27/118, 21/8238

(21) International Application Number: PCT/US02/03512

(22) International Filing Date: 7 February 2002 (07.02.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/788,109 15 February 2001 (15.02.2001) US

(71) Applicant: MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83716 (US).

(72) Inventor: FORBES, Leonard; 965 N.W. Highland Terrace, P.O. Box 1716, Corvallis, OR 97330 (US).

(74) Agents: MATKIN, Mark, S. et al.; Wells St. John P.S., Suite 1300, W. 601 First Avenue, Spokane, WA 99201-3828 (US).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

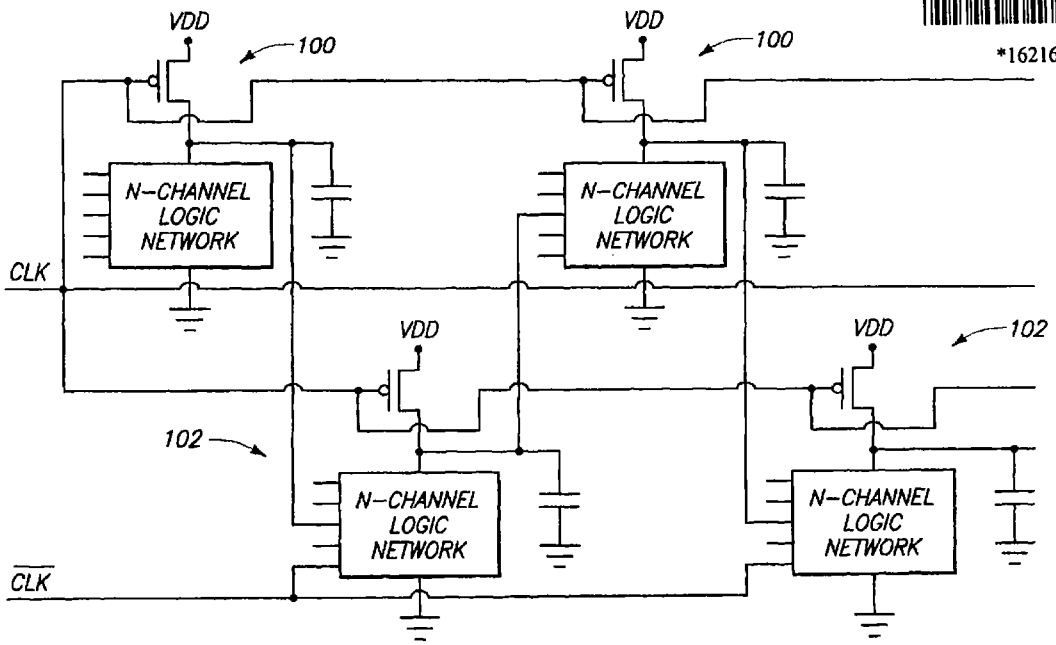
**Published:**
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
30 October 2003

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

(54) Title: MONOTONIC DYNAMIC-STATIC PSEUDO-NMOS LOGIC CIRCUIT AND METHOD OF FORMING A LOGIC GATE ARRAY

*162162*




(57) Abstract: A monotonic dynamic-static pseudo-NMOS logic circuit comprises a dynamic logic circuit having a clock input and having an output configured to be pre-charged high when a low clock signal is provided to the clock input; and a static logic circuit having a clock bar input and having an output configured to be precharged low when a high value of the complement of the clock signal is provided to the clock bar input. A logic gate array comprises a plurality of vertical ultrathin transistors coupled together.

WO 02/071611 A3