FIG. 1

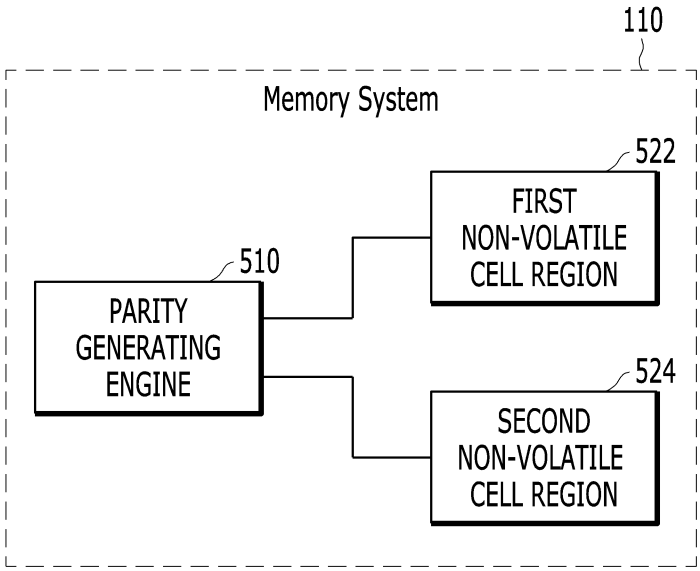

110
Memory System
522
FIRST
NON-VOLATILE
CELL REGION
510
PARITY
GENERATING
ENGINE
524
SECOND
NON-VOLATILE
CELL REGION

FIG. 2

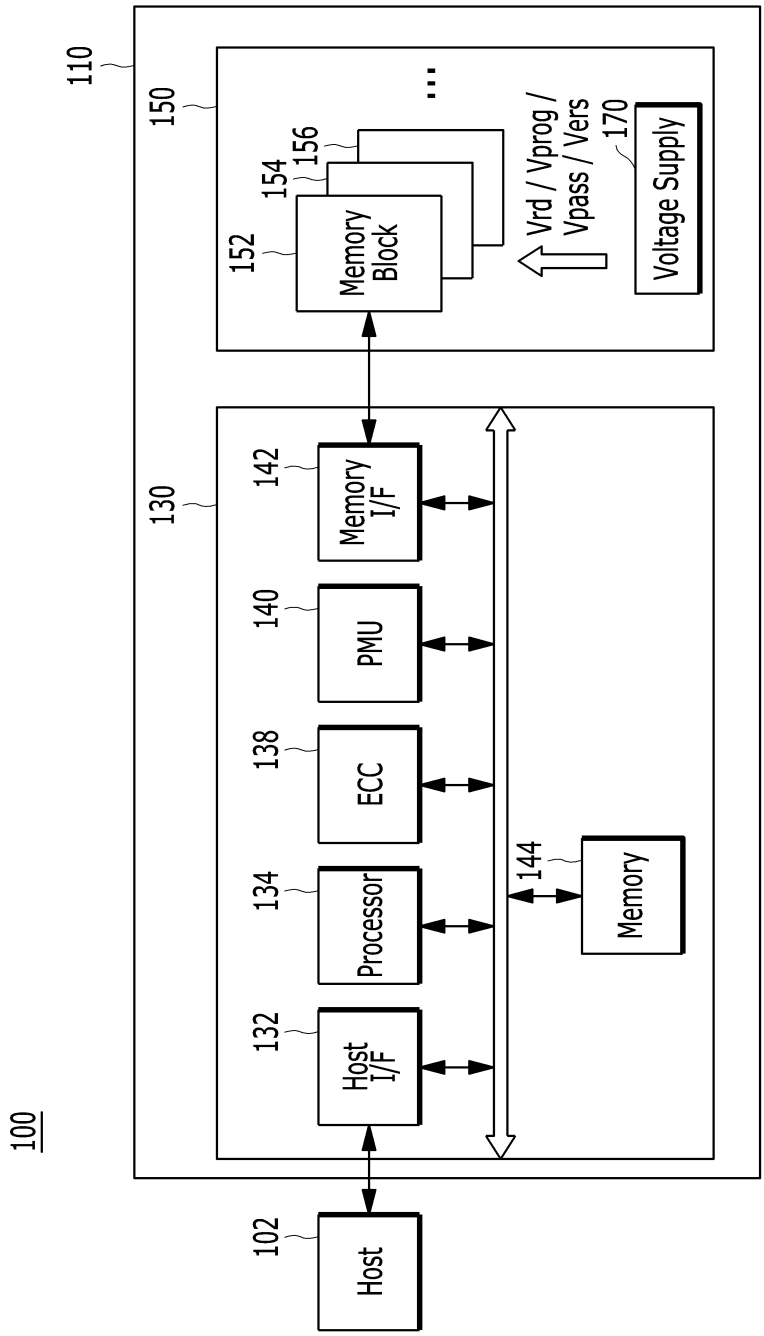

100
110
150
152
Memory Block
154
156
...
Vrd / Vprog / Vpass / Vers
170
Voltage Supply
130
142
Memory I/F
140
PMU
138
ECC
134
Processor
144
Memory
132
Host I/F
102
Host

FIG. 3

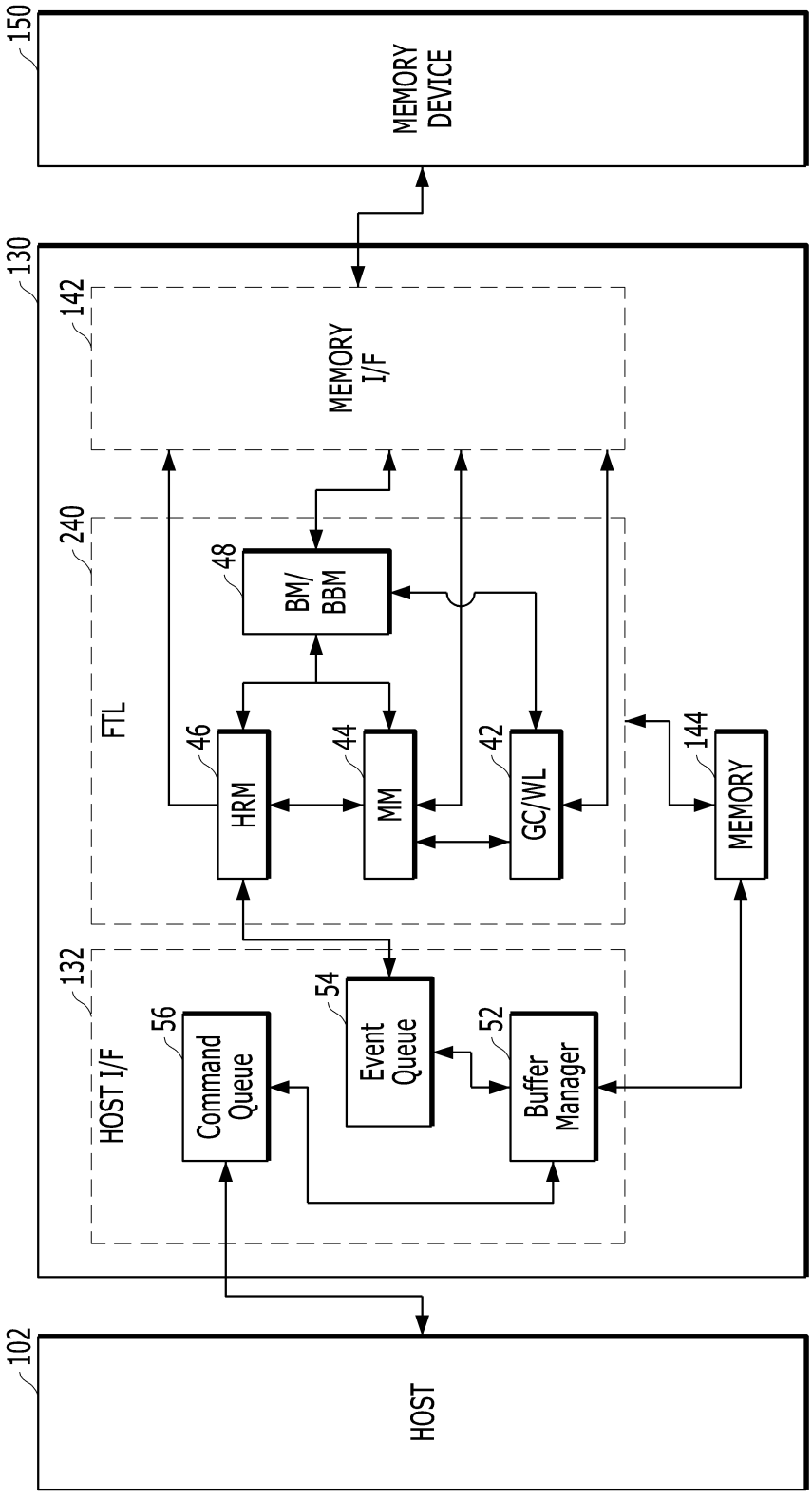

150
MEMORY DEVICE
130
142
MEMORY I/F
240
FTL
48
BM/ BBM
46
HRM
44
MM
42
GC/WL
144
MEMORY
132
HOST I/F
56
Command Queue
54
Event Queue
52
Buffer Manager
102
HOST

FIG. 4

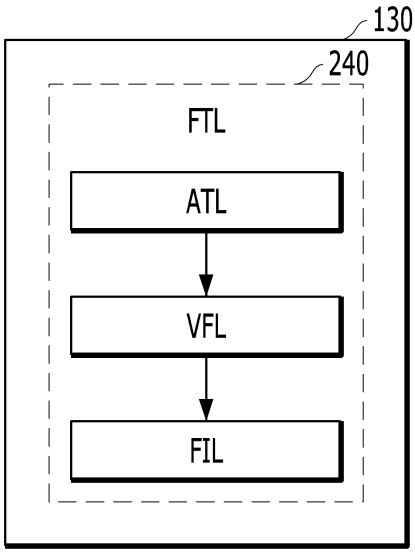


FIG. 5

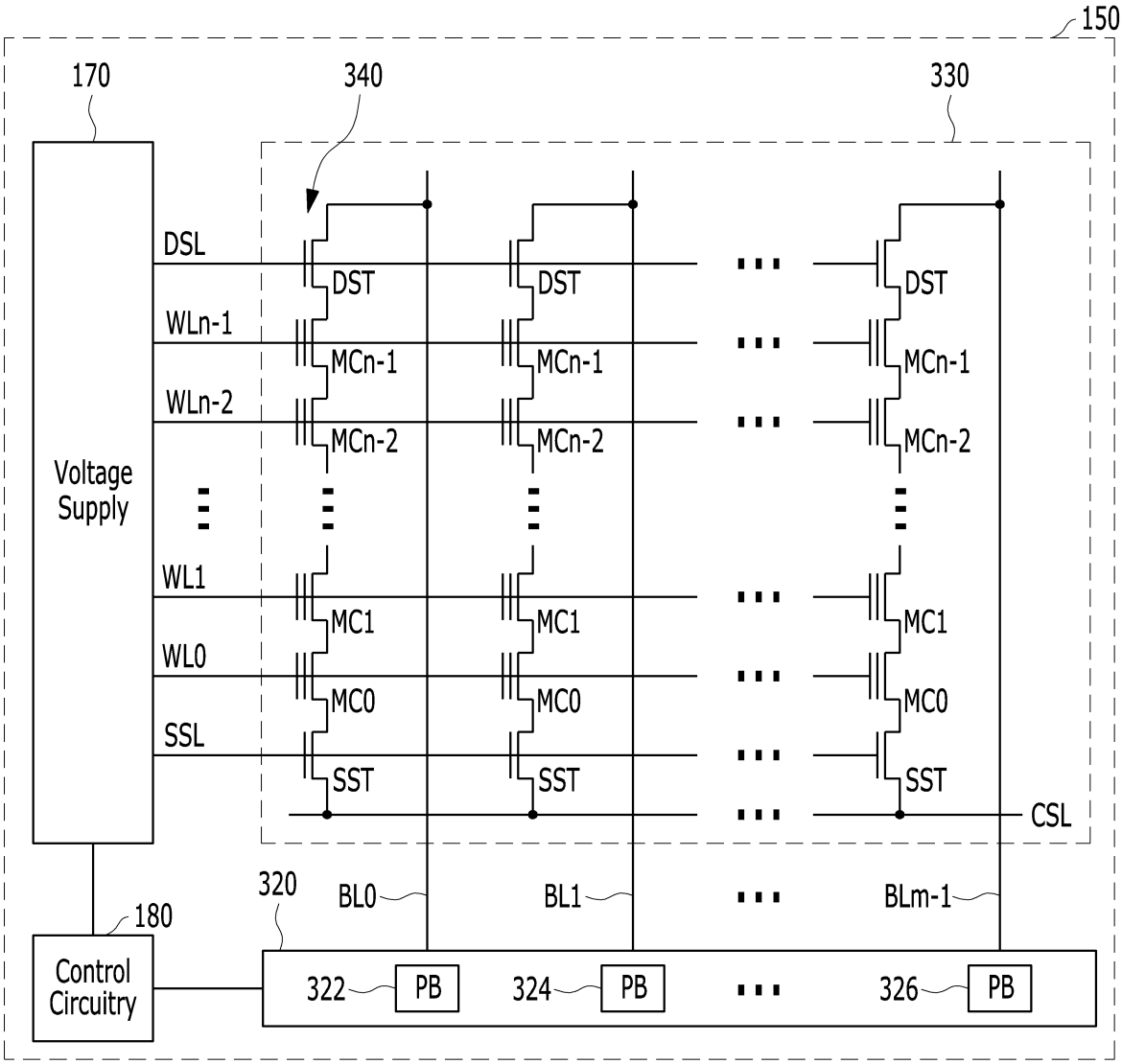

150
170
340
330
DSL
WLn-1
WLn-2
WL1
WL0
SSL
DST
MCn-1
MCn-2
MC1
MC0
SST
CSL
Voltage Supply
320
BL0
BL1
BLm-1
180
Control Circuitry
322
PB
324
PB
326
PB

FIG. 6

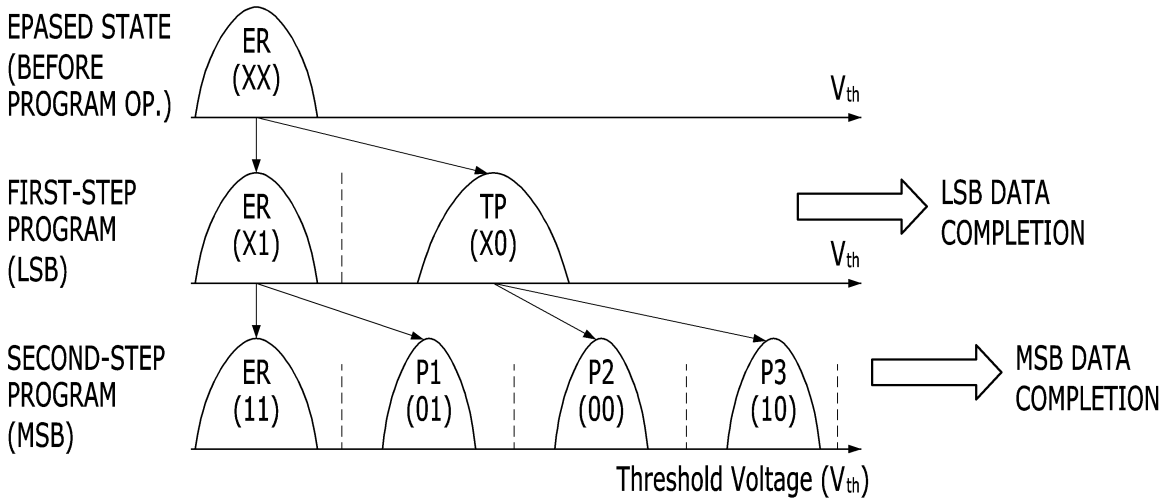

EPASED STATE
(BEFORE
PROGRAM OP.)
ER
(XX)
Vth
FIRST-STEP
PROGRAM
(LSB)
ER
(X1)
TP
(X0)
LSB DATA
COMPLETION
Vth
SECOND-STEP
PROGRAM
(MSB)
ER
(11)
P1
(01)
P2
(00)
P3
(10)
MSB DATA
COMPLETION
Threshold Voltage (Vth)

FIG. 7

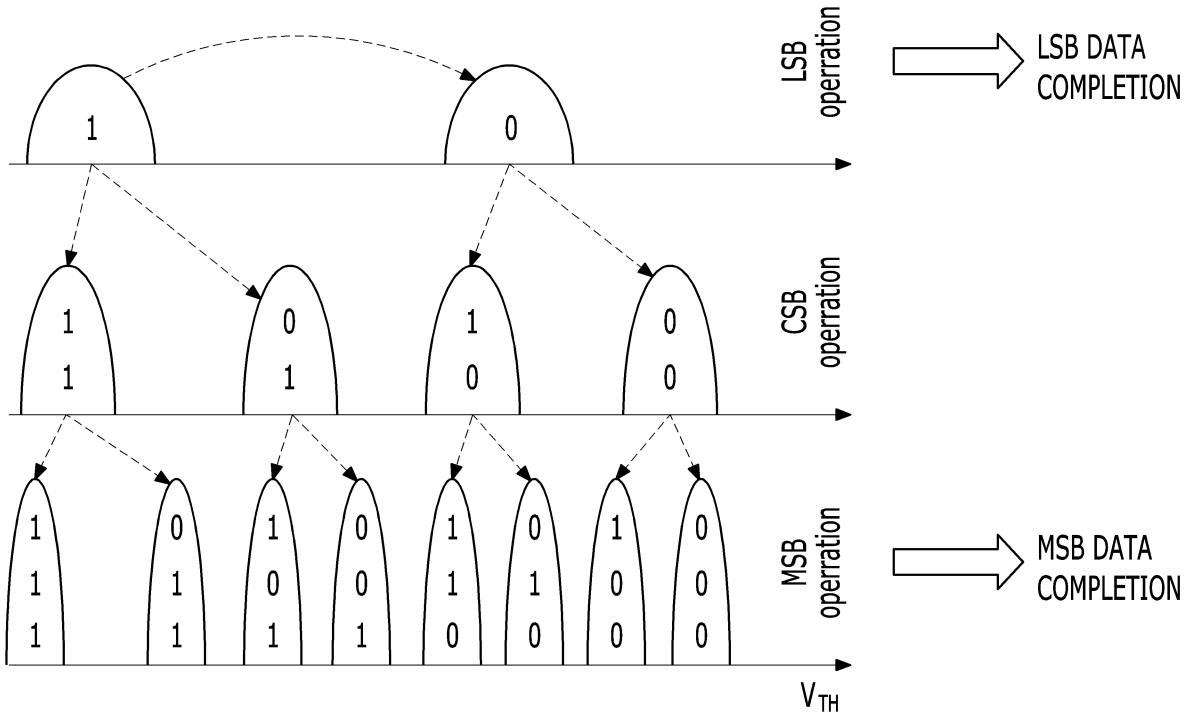

LSB operration
LSB DATA COMPLETION
CSB operration
MSB operration
MSB DATA COMPLETION
V_{TH}

FIG. 8

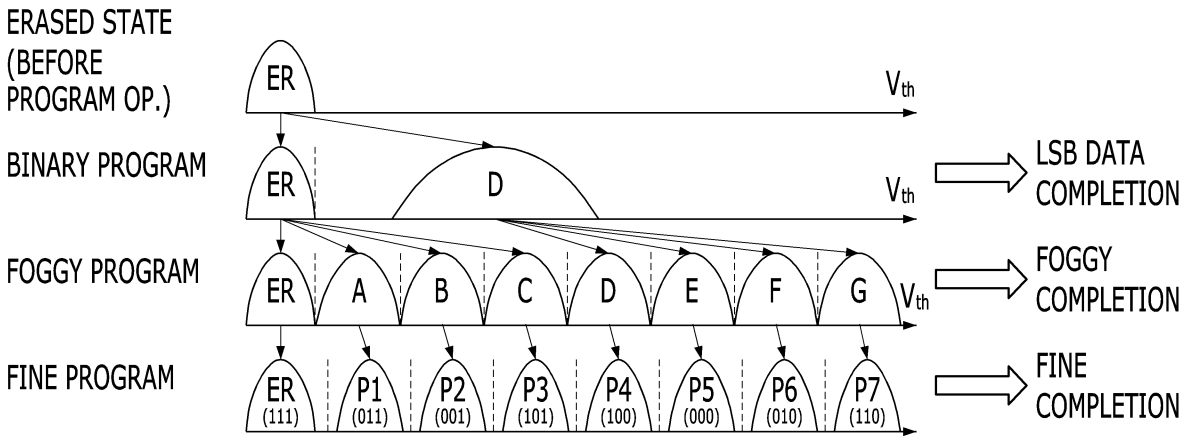

ERASED STATE
(BEFORE
PROGRAM OP.)
BINARY PROGRAM
FOGGY PROGRAM
FINE PROGRAM
ER
D
A
B
C
D
E
F
G
P1
P2
P3
P4
P5
P6
P7
(111)
(011)
(001)
(101)
(100)
(000)
(010)
(110)
Vth
LSB DATA
COMPLETION
FOGGY
COMPLETION
FINE
COMPLETION

FIG. 9

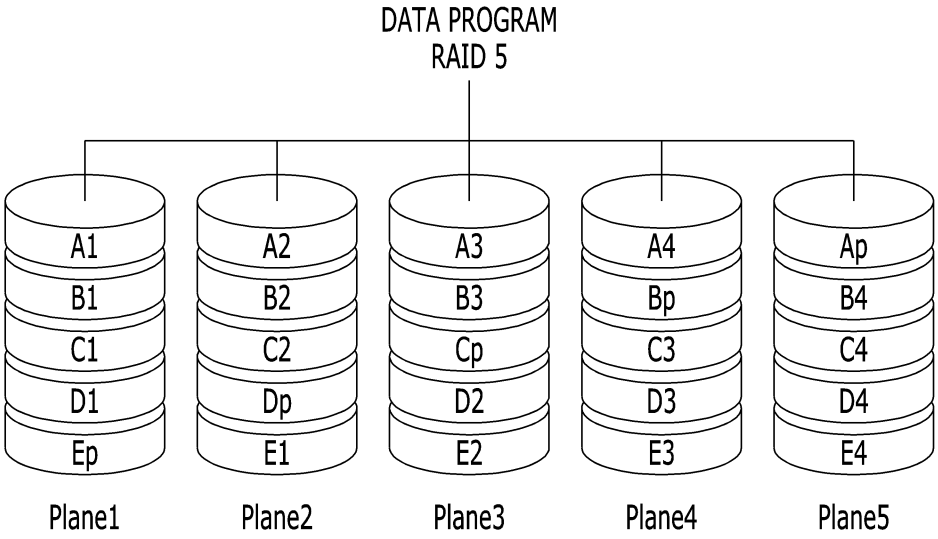

DATA PROGRAM
RAID 5
A1
B1
C1
D1
Ep
A2
B2
C2
Dp
E1
A3
B3
Cp
D2
E2
A4
Bp
C3
D3
E3
Ap
B4
C4
D4
E4
Plane1
Plane2
Plane3
Plane4
Plane5

FIG. 10

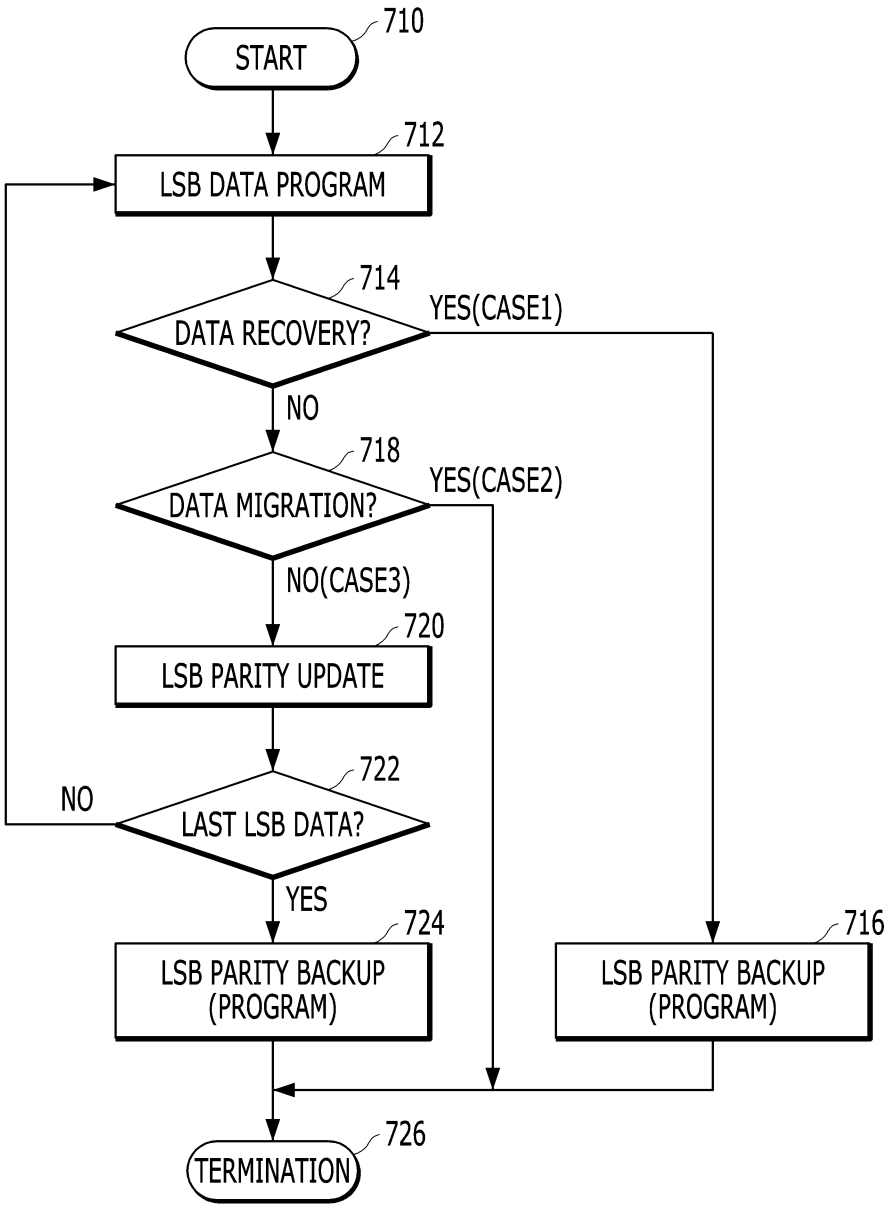

710
START
712
LSB DATA PROGRAM
714
DATA RECOVERY?
YES(CASE1)
NO
718
DATA MIGRATION?
YES(CASE2)
NO(CASE3)
720
LSB PARITY UPDATE
722
NO
LAST LSB DATA?
YES
724
LSB PARITY BACKUP
(PROGRAM)
716
LSB PARITY BACKUP
(PROGRAM)
726
TERMINATION

FIG. 11

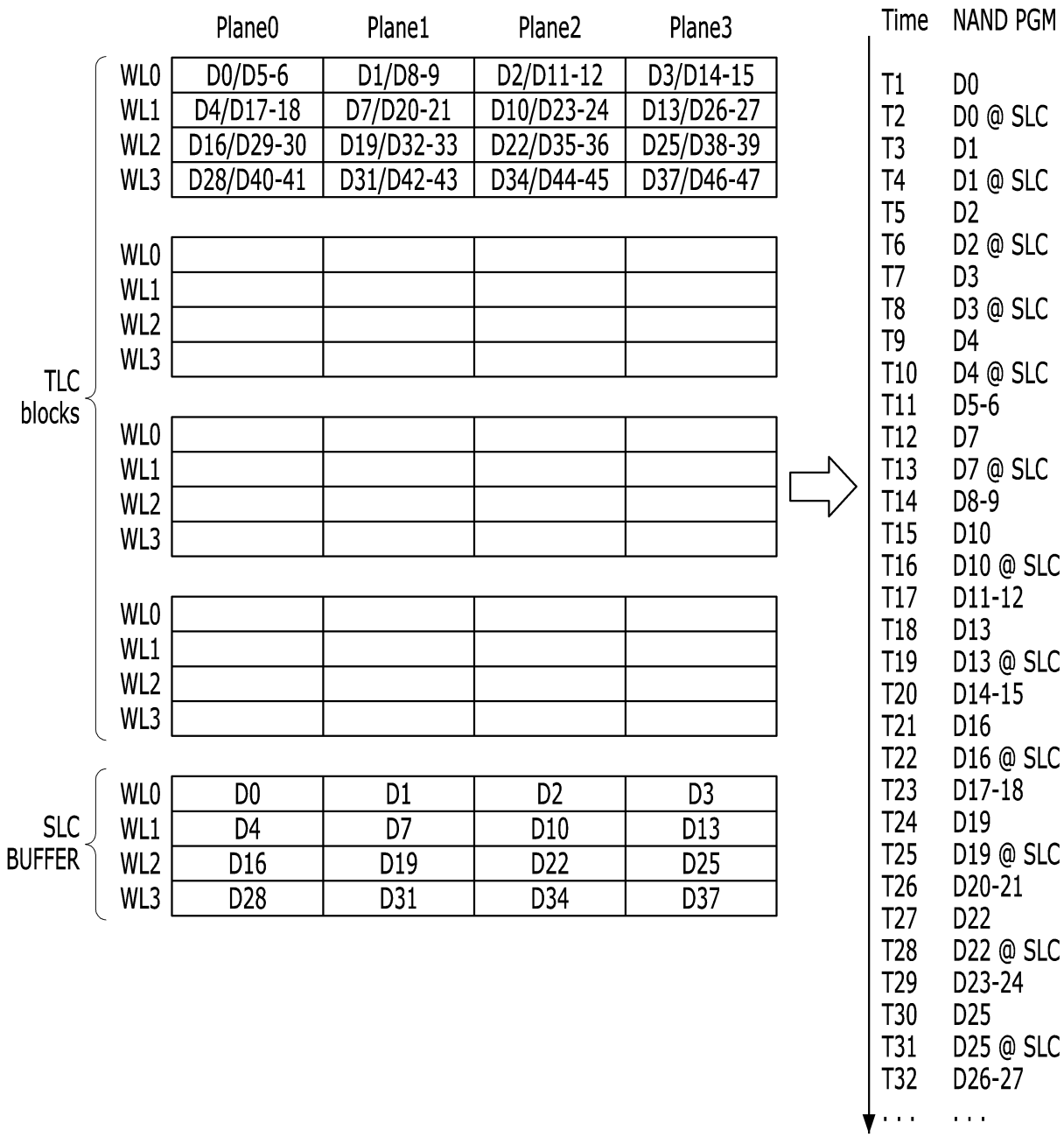

Plane0
Plane1
Plane2
Plane3
TLC blocks
WL0
WL1
WL2
WL3
D0/D5-6
D1/D8-9
D2/D11-12
D3/D14-15
D4/D17-18
D7/D20-21
D10/D23-24
D13/D26-27
D16/D29-30
D19/D32-33
D22/D35-36
D25/D38-39
D28/D40-41
D31/D42-43
D34/D44-45
D37/D46-47
SLC BUFFER
D0
D1
D2
D3
D4
D7
D10
D13
D16
D19
D22
D25
D28
D31
D34
D37
Time
NAND PGM
T1 D0
T2 D0 @ SLC
T3 D1
T4 D1 @ SLC
T5 D2
T6 D2 @ SLC
T7 D3
T8 D3 @ SLC
T9 D4
T10 D4 @ SLC
T11 D5-6
T12 D7
T13 D7 @ SLC
T14 D8-9
T15 D10
T16 D10 @ SLC
T17 D11-12
T18 D13
T19 D13 @ SLC
T20 D14-15
T21 D16
T22 D16 @ SLC
T23 D17-18
T24 D19
T25 D19 @ SLC
T26 D20-21
T27 D22
T28 D22 @ SLC
T29 D23-24
T30 D25
T31 D25 @ SLC
T32 D26-27
. . .
. . .

FIG. 12

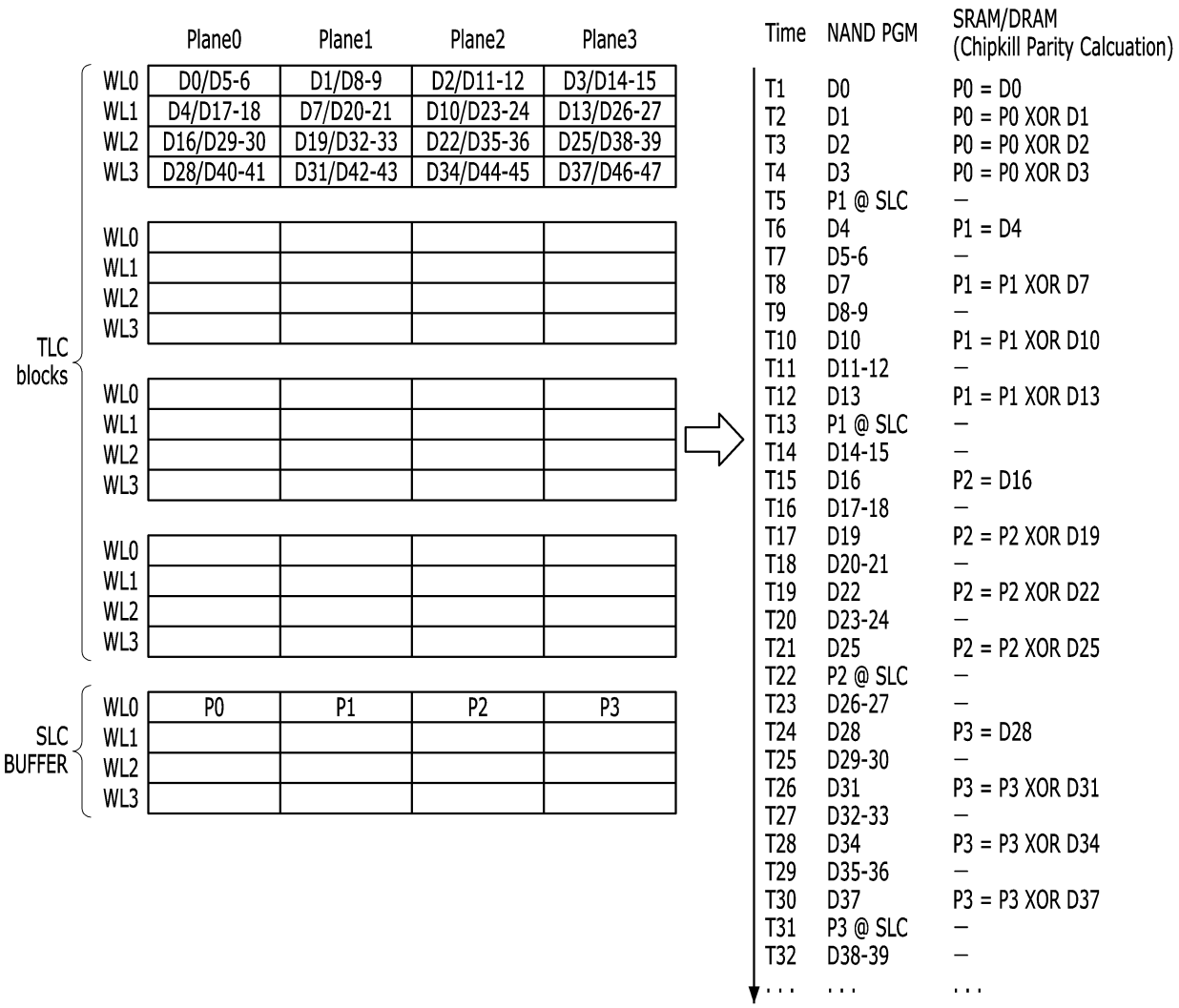

Plane0
Plane1
Plane2
Plane3
TLC blocks
WL0
WL1
WL2
WL3
D0/D5-6
D1/D8-9
D2/D11-12
D3/D14-15
D4/D17-18
D7/D20-21
D10/D23-24
D13/D26-27
D16/D29-30
D19/D32-33
D22/D35-36
D25/D38-39
D28/D40-41
D31/D42-43
D34/D44-45
D37/D46-47
SLC BUFFER
P0
P1
P2
P3
Time
NAND PGM
SRAM/DRAM (Chipkill Parity Calcuation)
T1 D0 P0 = D0
T2 D1 P0 = P0 XOR D1
T3 D2 P0 = P0 XOR D2
T4 D3 P0 = P0 XOR D3
T5 P1 @ SLC –
T6 D4 P1 = D4
T7 D5-6 –
T8 D7 P1 = P1 XOR D7
T9 D8-9 –
T10 D10 P1 = P1 XOR D10
T11 D11-12 –
T12 D13 P1 = P1 XOR D13
T13 P1 @ SLC –
T14 D14-15 –
T15 D16 P2 = D16
T16 D17-18 –
T17 D19 P2 = P2 XOR D19
T18 D20-21 –
T19 D22 P2 = P2 XOR D22
T20 D23-24 –
T21 D25 P2 = P2 XOR D25
T22 P2 @ SLC –
T23 D26-27 –
T24 D28 P3 = D28
T25 D29-30 –
T26 D31 P3 = P3 XOR D31
T27 D32-33 –
T28 D34 P3 = P3 XOR D34
T29 D35-36 –
T30 D37 P3 = P3 XOR D37
T31 P3 @ SLC –
T32 D38-39 –
. . . . . .

FIG. 13

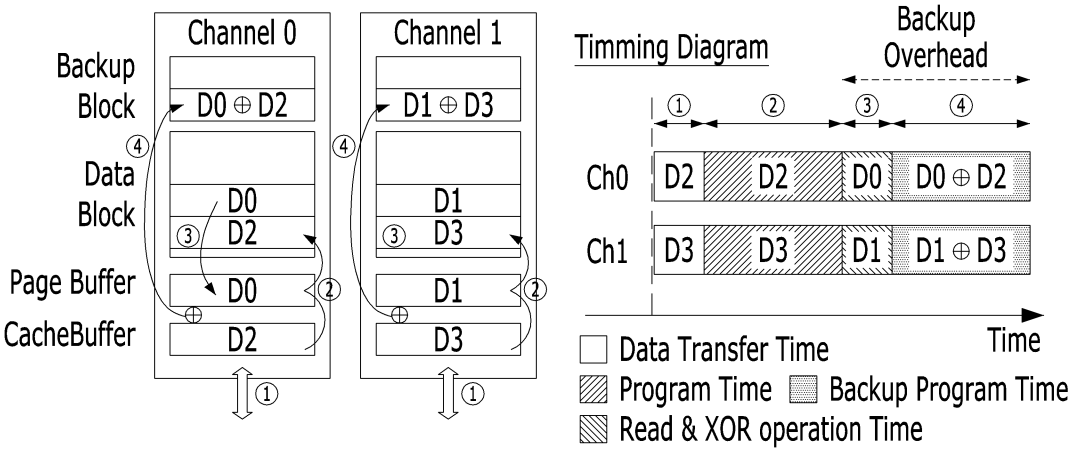

Channel 0
Channel 1
Backup Block
Data Block
Page Buffer
CacheBuffer
D0 ⊕ D2
D1 ⊕ D3
D0
D2
D1
D3
Timming Diagram
Backup Overhead
Ch0
Ch1
Time
Data Transfer Time
Program Time
Backup Program Time
Read & XOR operation Time

FIG. 14

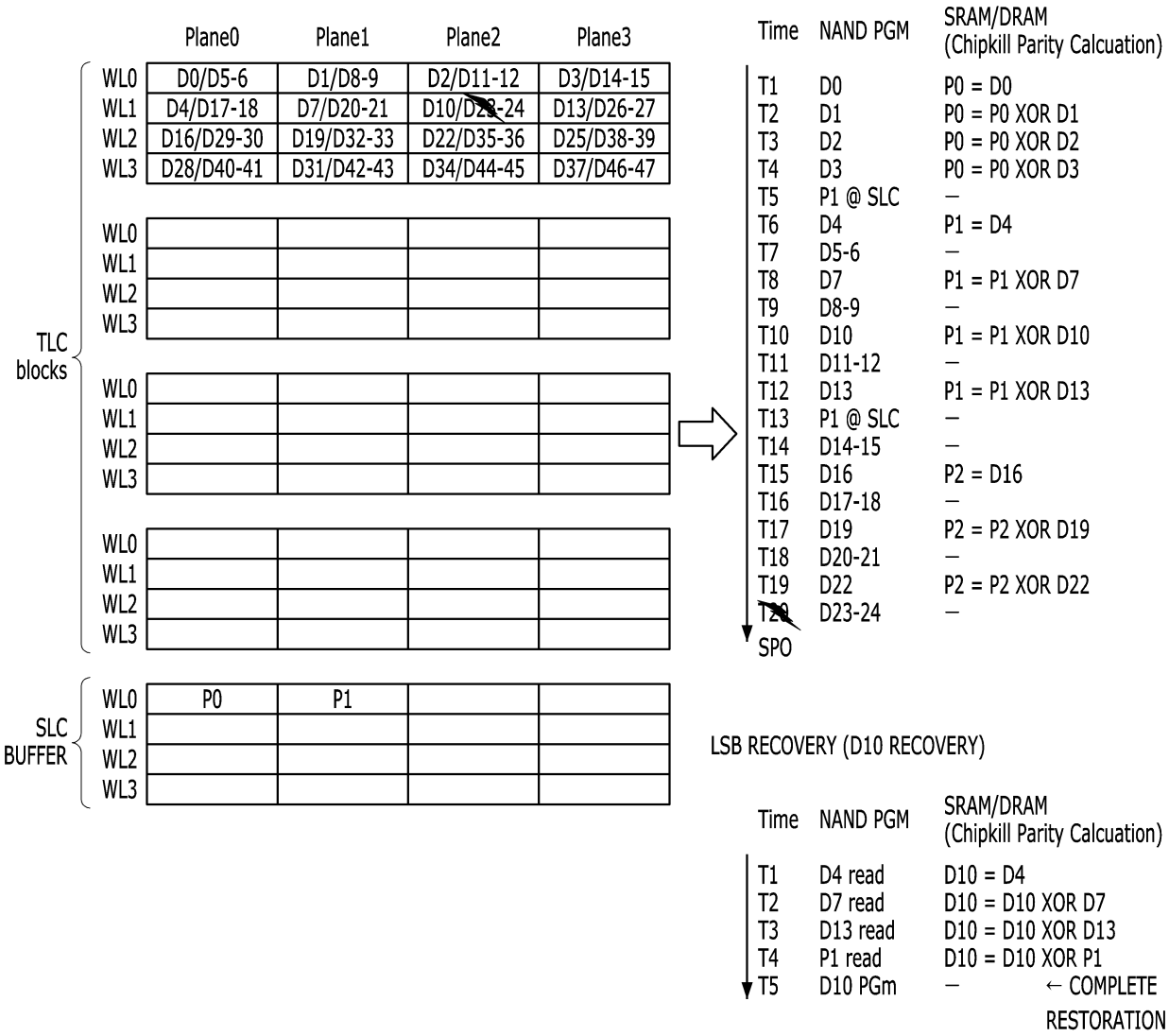

Plane0
Plane1
Plane2
Plane3
TLC blocks
WL0
WL1
WL2
WL3
D0/D5-6
D1/D8-9
D2/D11-12
D3/D14-15
D4/D17-18
D7/D20-21
D10/D23-24
D13/D26-27
D16/D29-30
D19/D32-33
D22/D35-36
D25/D38-39
D28/D40-41
D31/D42-43
D34/D44-45
D37/D46-47
SLC BUFFER
P0
P1
Time
NAND PGM
SRAM/DRAM (Chipkill Parity Calcuation)
T1 D0 P0 = D0
T2 D1 P0 = P0 XOR D1
T3 D2 P0 = P0 XOR D2
T4 D3 P0 = P0 XOR D3
T5 P1 @ SLC –
T6 D4 P1 = D4
T7 D5-6 –
T8 D7 P1 = P1 XOR D7
T9 D8-9 –
T10 D10 P1 = P1 XOR D10
T11 D11-12 –
T12 D13 P1 = P1 XOR D13
T13 P1 @ SLC –
T14 D14-15 –
T15 D16 P2 = D16
T16 D17-18 –
T17 D19 P2 = P2 XOR D19
T18 D20-21 –
T19 D22 P2 = P2 XOR D22
T20 D23-24 –
SPO
LSB RECOVERY (D10 RECOVERY)
Time
NAND PGM
SRAM/DRAM (Chipkill Parity Calcuation)
T1 D4 read D10 = D4
T2 D7 read D10 = D10 XOR D7
T3 D13 read D10 = D10 XOR D13
T4 P1 read D10 = D10 XOR P1
T5 D10 PGm – ← COMPLETE RESTORATION

FIG. 15

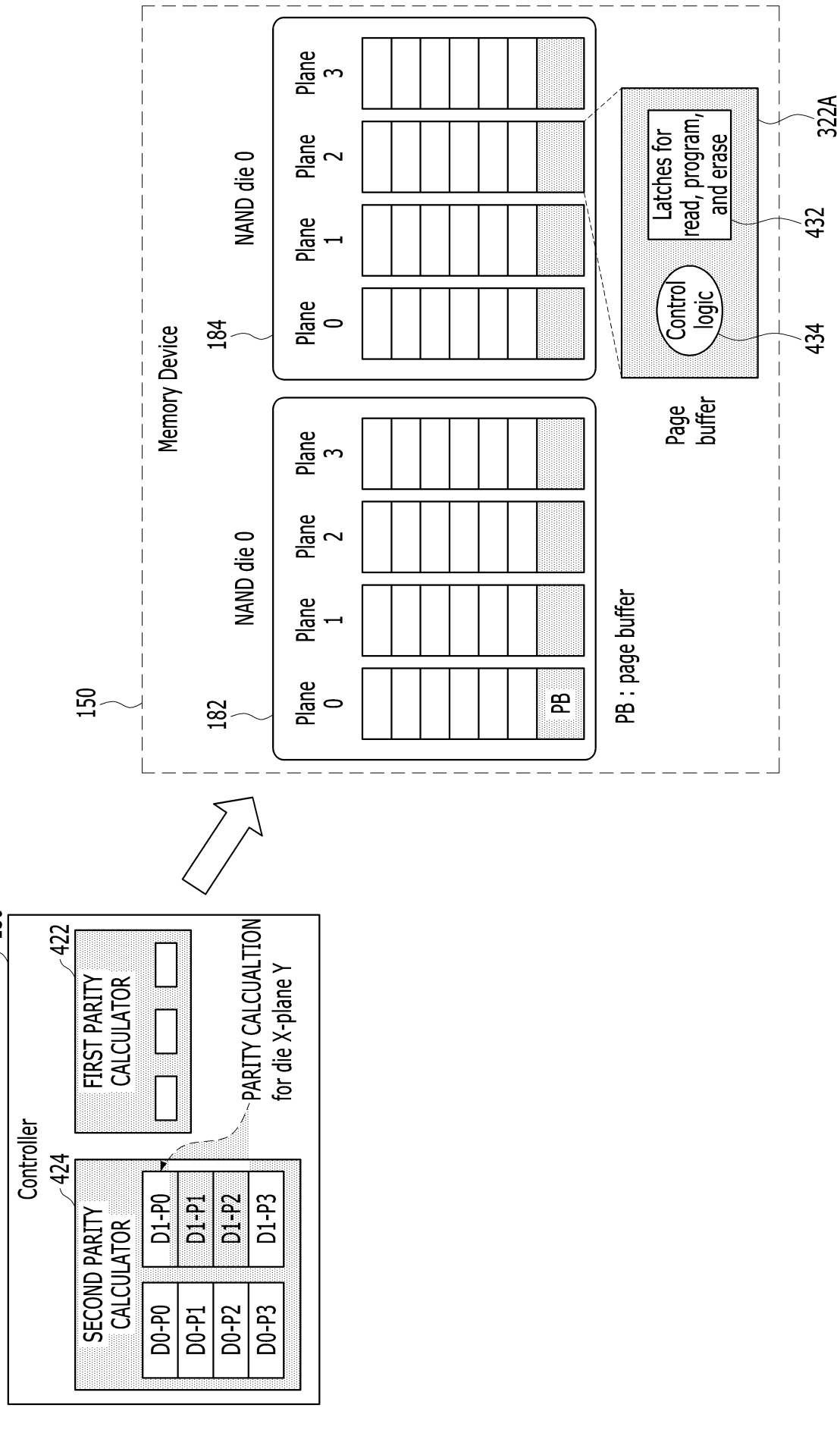

130
Controller
422
FIRST PARITY CALCULATOR
424
SECOND PARITY CALCULATOR
D0-P0
D0-P1
D0-P2
D0-P3
D1-P0
D1-P1
D1-P2
D1-P3
PARITY CALCUALTION for die X-plane Y
150
Memory Device
182
NAND die 0
Plane 0
Plane 1
Plane 2
Plane 3
PB
PB : page buffer
184
NAND die 0
Plane 0
Plane 1
Plane 2
Plane 3
Page buffer
Latches for read, program, and erase
Control logic
322A
432
434

FIG. 16

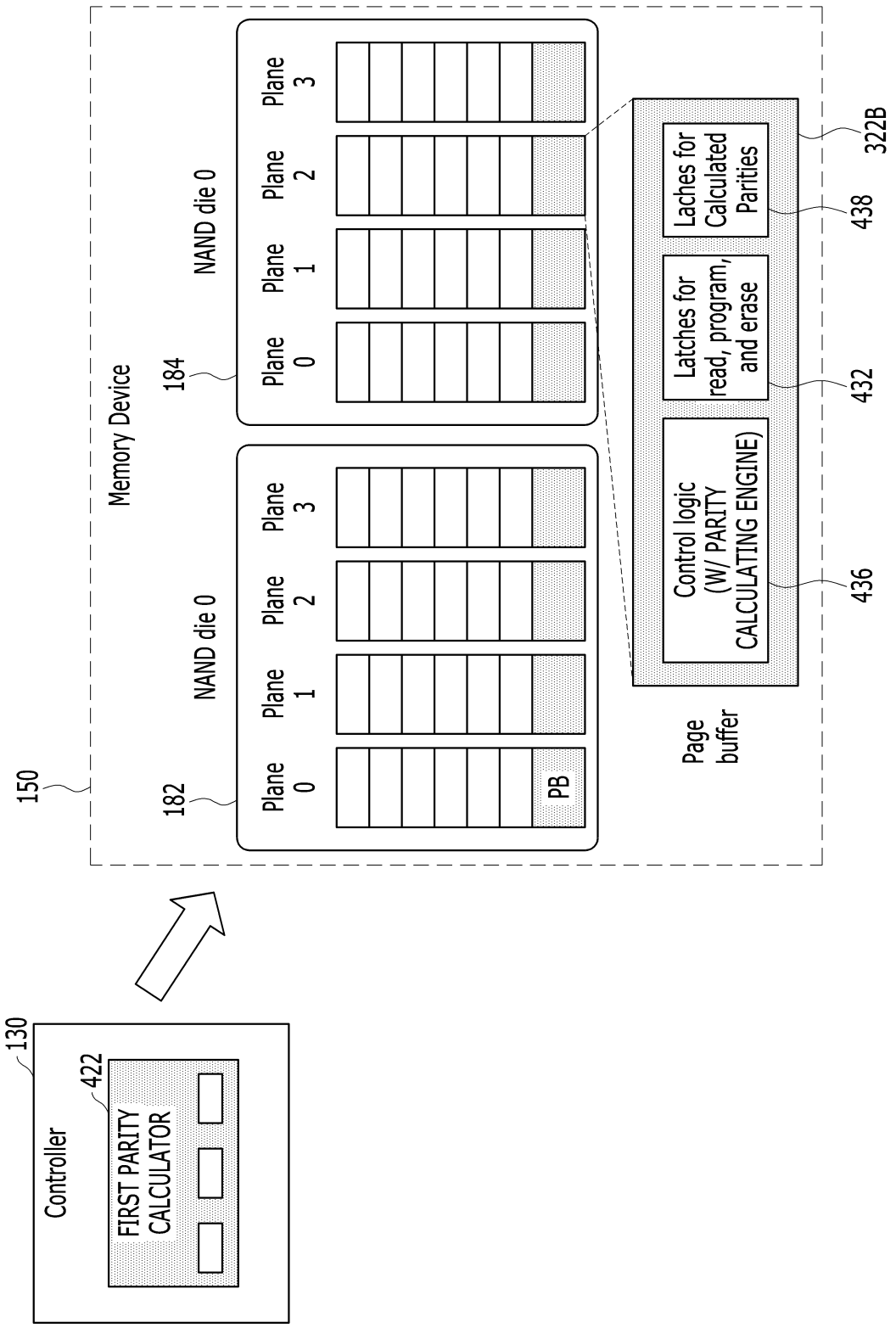

130
Controller
422
FIRST PARITY CALCULATOR
150
Memory Device
182
NAND die 0
Plane 0
Plane 1
Plane 2
Plane 3
PB
184
NAND die 0
Plane 0
Plane 1
Plane 2
Plane 3
Page buffer
Control logic (W/ PARITY CALCULATING ENGINE)
436
Latches for read, program, and erase
432
Laches for Calculated Parities
438
322B

FIG. 17

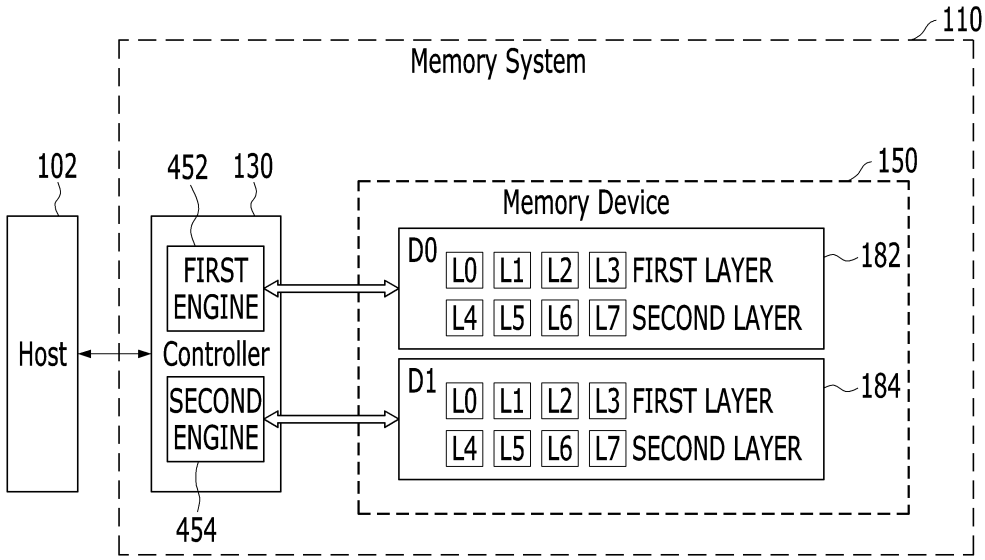

110
Memory System
102
452
130
150
Memory Device
Host
FIRST ENGINE
Controller
SECOND ENGINE
454
D0
L0 L1 L2 L3 FIRST LAYER
L4 L5 L6 L7 SECOND LAYER
182
D1
L0 L1 L2 L3 FIRST LAYER
L4 L5 L6 L7 SECOND LAYER
184

FIG. 18

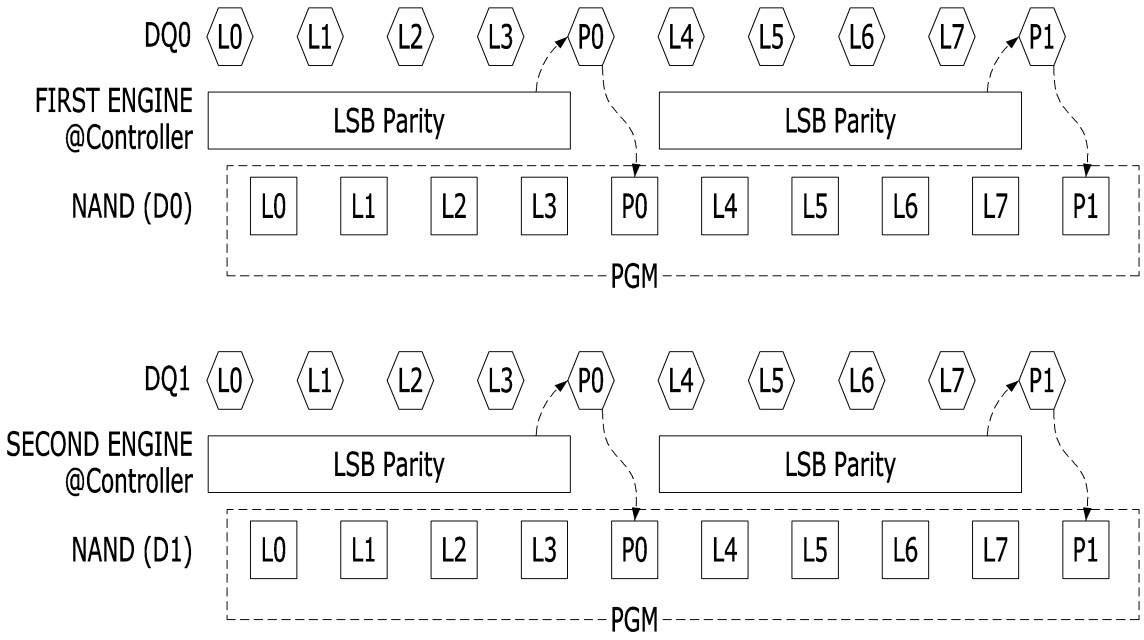

DQ0
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
FIRST ENGINE
@Controller
LSB Parity
LSB Parity
NAND (D0)
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
PGM
DQ1
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
SECOND ENGINE
@Controller
LSB Parity
LSB Parity
NAND (D1)
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
PGM

FIG. 19

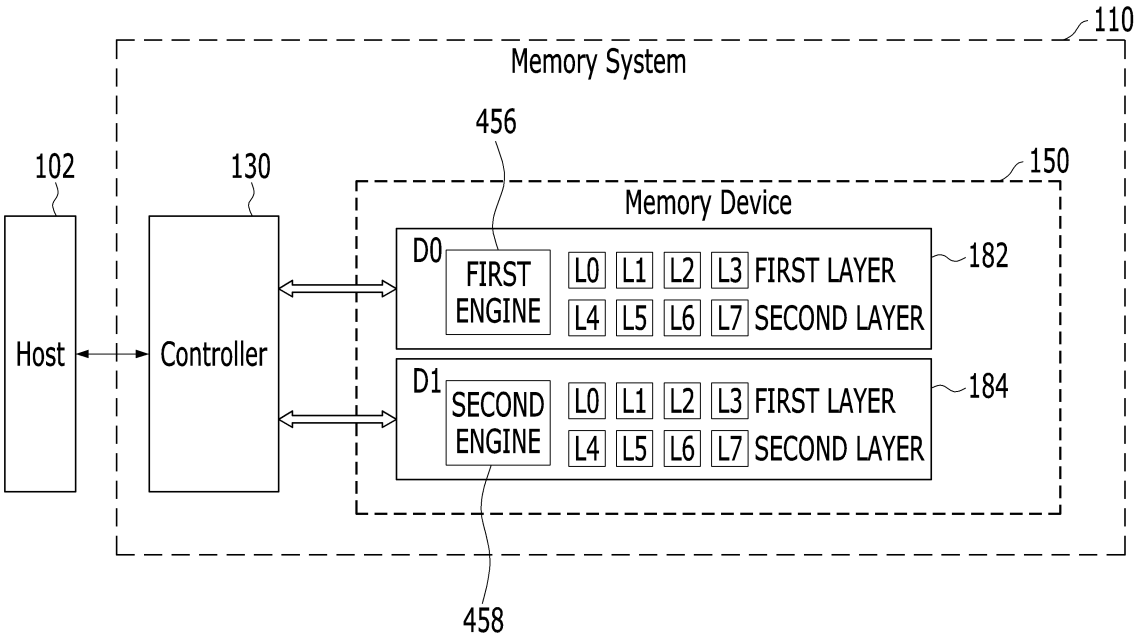

110
Memory System
456
102
130
150
Memory Device
D0
FIRST ENGINE
L0 L1 L2 L3 FIRST LAYER
L4 L5 L6 L7 SECOND LAYER
182
Host
Controller
D1
SECOND ENGINE
L0 L1 L2 L3 FIRST LAYER
L4 L5 L6 L7 SECOND LAYER
184
458

FIG. 20

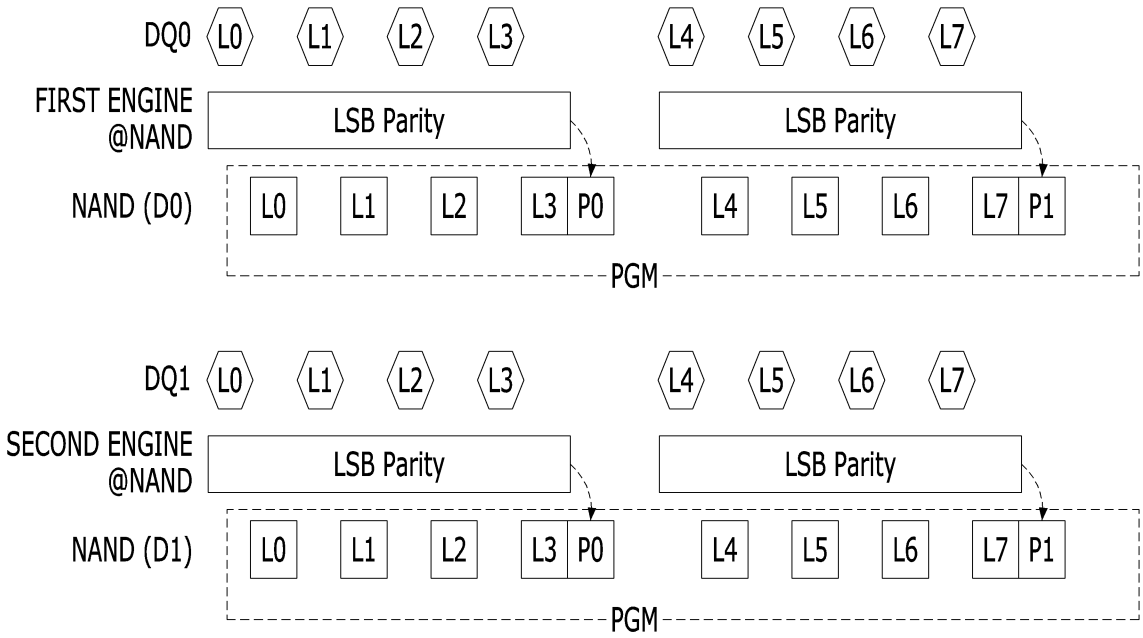

DQ0
L0
L1
L2
L3
L4
L5
L6
L7
FIRST ENGINE @NAND
LSB Parity
LSB Parity
NAND (D0)
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
PGM
DQ1
L0
L1
L2
L3
L4
L5
L6
L7
SECOND ENGINE @NAND
LSB Parity
LSB Parity
NAND (D1)
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
PGM

FIG. 21

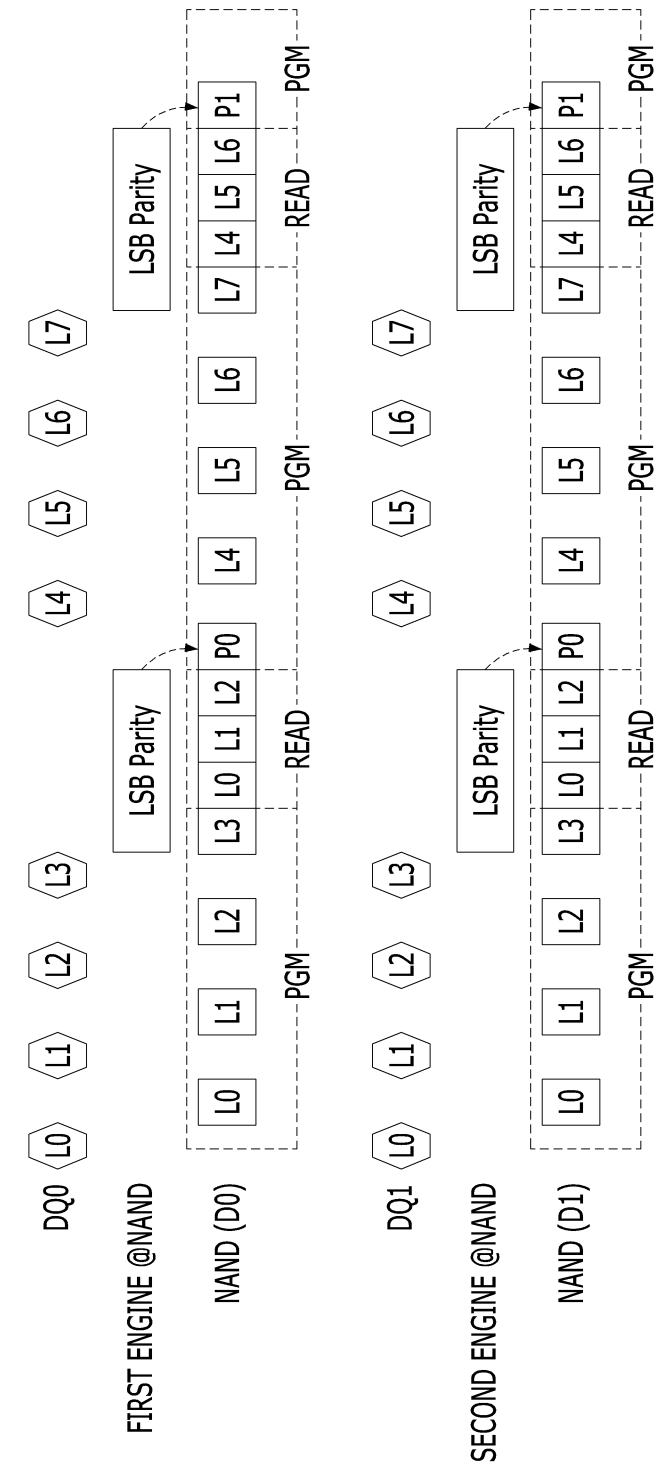
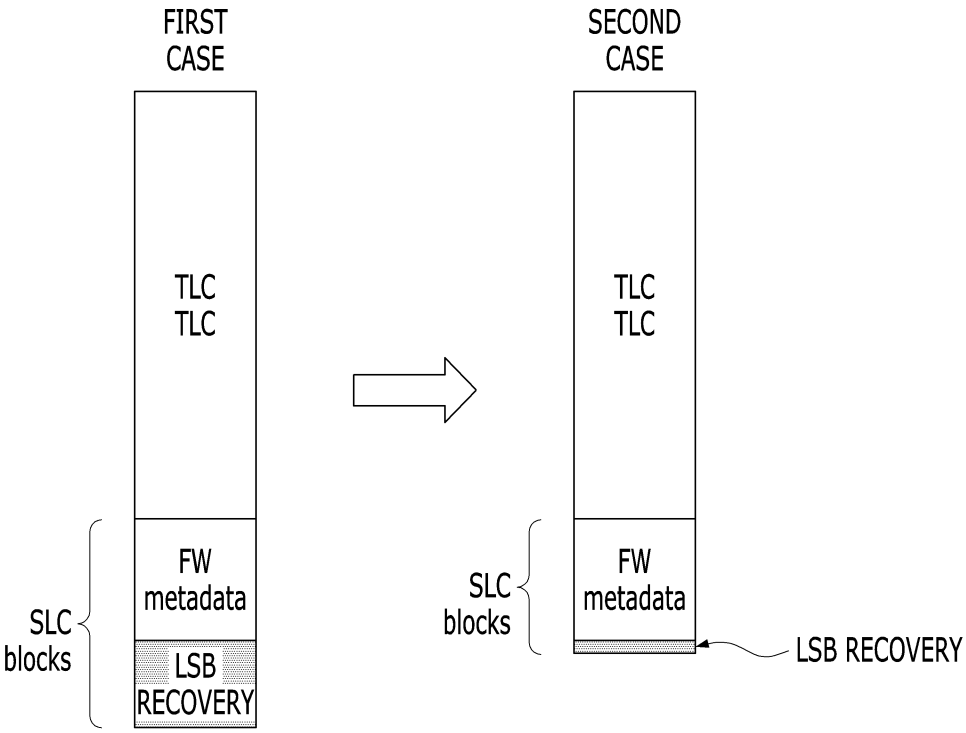

DQ0
L0
L1
L2
L3
L4
L5
L6
L7
FIRST ENGINE @NAND
NAND (D0)
LSB Parity
L0
L1
L2
L3
P0
L4
L5
L6
L7
P1
PGM
READ
PGM
READ
PGM
DQ1
SECOND ENGINE @NAND
NAND (D1)
LSB Parity
PGM
READ
PGM
READ
PGM

FIG. 22


FIRST
CASE
TLC
TLC
FW
metadata
LSB
RECOVERY
SLC
blocks
SECOND
CASE
TLC
TLC
FW
metadata
SLC
blocks
LSB RECOVERY