CLAIMS

WHAT IS CLAIMED:

1. A semiconductor structure, comprising:

a substrate; and

a transistor, the transistor comprising:

a raised source region and a raised drain region provided above said substrate;

one or more elongated semiconductor lines connected between said raised source region and said raised drain region, wherein a longitudinal direction of each of said one or more elongated semiconductor lines extends substantially along a horizontal direction that is perpendicular to a thickness direction of said substrate, each of said elongated semiconductor lines comprising a channel region;

a gate electrode that extends all around each of said channel regions of said one or more elongated semiconductor lines; and

a gate insulation layer provided between each of said one or more elongated semiconductor lines and said gate electrode.

2. The semiconductor structure of claim 1, wherein said substrate comprises a semiconductor material, said semiconductor structure further comprising a layer of an electrically insulating material provided between said substrate and at least portions of said raised source and drain regions.

3. The semiconductor structure of claim 2, wherein each of said one or more elongated semiconductor lines comprises a source region and a drain region, said channel

region being provided between said source region and said drain region, at least a portion of said source region being provided below said raised source region, at least a portion of said drain region being provided below said raised drain region.

4. The semiconductor structure of claim 3, wherein a portion of said gate electrode below said one or more elongated semiconductor lines is closer to said substrate than an interface between said layer of electrically insulating material and said source and drain regions.

5. The semiconductor structure of claim 4, wherein the portion of said gate electrode below said one or more elongated semiconductor lines is provided in an opening of said layer of electrically insulating material.

6. The semiconductor structure of claim 4, wherein parts of the portion of said gate electrode below said one or more elongated semiconductor lines extend below at least one of said source and drain regions and said raised source and drain regions.

7. The semiconductor structure of claim 6, wherein an extension of the portion of said gate electrode below said one or more elongated semiconductor lines along the longitudinal direction of said one or more elongated semiconductor lines is greater than an extension of portions of said gate electrode above said elongated semiconductor lines along the longitudinal direction of said one or more elongated semiconductor lines.

8. The semiconductor structure of claim 1, further comprising a sidewall spacer formed adjacent a portion of said gate electrode located above said channel regions, said

sidewall spacer separating said gate electrode from said raised source region and said raised drain region.

9. The semiconductor structure of claim 1, wherein said gate insulation layer comprises a high-k material having a greater dielectric constant than silicon dioxide and said gate electrode comprises a metal.

10. A method, comprising:

forming one or more elongated semiconductor lines on a layer of electrically insulating material, said layer of electrically insulating material being provided over a substrate comprising a different material than the layer of electrically insulating material, wherein a longitudinal direction of each of said one or more elongated semiconductor lines extends substantially along a horizontal direction that is perpendicular to a thickness direction of said substrate;

removing a portion of said layer of electrically insulating material below a central portion of each of said one or more elongated semiconductor lines;

forming a gate insulation layer on said central portion of each of said one or more elongated semiconductor lines; and

forming a gate electrode extending all around said central portion of each of said one or more elongated semiconductor lines, said gate insulation layer providing electrical insulation between said elongated semiconductor lines and said gate electrode.

11. The method of claim 10, wherein the removal of said portion of said layer of electrically insulating material below said central portion of each of said one or more

elongated semiconductor lines forms an opening in said layer of electrically insulating material and a portion of said gate electrode below said one or more elongated semiconductor lines is formed in said opening.

12. The method of claim 10, wherein removing the portion of said layer of electrically insulating material below said central portion of each of said one or more elongated semiconductor lines comprises:

forming a first feature over a first end portion of each of said one or more elongated semiconductor lines;

forming a second feature over a second end portion of each of said one or more elongated semiconductor lines, wherein the central portion of each of said one or more elongated semiconductor lines and a portion of said layer of electrically insulating material are exposed between said first and the second feature; and

performing an etch process adapted to selectively remove a material of said layer of electrically insulating material relative to a material of said one or more elongated semiconductor lines and one or more materials exposed at surfaces of said first and the second feature.

13. The method of claim 12, wherein said etch process is substantially isotropic.

14. The method of claim 13, wherein said first feature comprises a raised source region, a first portion of a sidewall spacer formed above the first end portion of each of said one or more elongated semiconductor lines, and a first portion of a layer of dielectric material formed above said raised source region; and

wherein the second feature comprises a raised drain region, a second portion of the sidewall spacer formed above the second end portion of each of said one or more elongated semiconductor lines, and a second portion of a layer of dielectric material formed above said raised drain region.

15. The method of claim 14, wherein the formation of said first feature and said second feature comprises:

forming a dummy gate structure over the central portion of each of said elongated semiconductor lines;

forming the sidewall spacer adjacent said dummy gate structure;

performing a selective growth process, said selective growth process forming said raised source region and said raised drain region;

depositing the layer of dielectric material over said dummy gate structure, said raised source region and said raised drain region;

planarizing the layer of dielectric material, wherein the planarization exposes said dummy gate structure; and

performing one or more etch processes to selectively remove said dummy gate structure.

16. The method of claim 15, further comprising forming a silicide in said raised source region and said raised drain region before the deposition of said layer of dielectric material.

17. The method of claim 15, further comprising *in situ* doping said raised source region and said raised drain region during said selective growth process.

18. The method of claim 17, further comprising performing an annealing process, wherein dopants from said raised source region diffuse into the first end portion of each of said elongated semiconductor lines and form a source region, and dopants from said raised drain region diffuse into the second end portion of each of said elongated semiconductor lines and form a drain region.

19. The method of claim 10, wherein the formation of said one or more elongated semiconductor lines comprises:

providing a semiconductor-on-insulator structure, said semiconductor-on-insulator structure comprising a layer of a semiconductor material, said substrate and said layer of electrically insulating material, said layer of electrically insulating material being provided between said substrate and said layer of semiconductor material; and

performing an etch process, said etch process removing portions of said layer of semiconductor material, wherein one or more other portions of said layer of semiconductor material are not removed in said etch process and form said one or more elongated semiconductor lines.

20. The method of claim 10, wherein said gate insulation layer comprises a high-k material having a greater dielectric constant than silicon dioxide and said gate electrode comprises a metal.

What is claimed:

1. A method, comprising: forming one or more elongated semiconductor lines on a layer of electrically insulating material, said layer of electrically insulating material being provided over a substrate comprising a different material than the layer of electrically insulating material, wherein a longitudinal direction of each of said one or more elongated semiconductor lines extends substantially along a horizontal direction that is perpendicular to a thickness direction of said substrate; removing a portion of said layer of electrically insulating material below a central portion of each of said one or more elongated semiconductor lines to expose said substrate; forming a gate insulation layer on said central portion of each of said one or more elongated semiconductor lines and said exposed portion of said substrate; and forming a gate electrode extending all around said central portion of each of said one or more elongated semiconductor lines, said gate insulation layer providing electrical insulation between said elongated semiconductor lines and said gate electrode and between said gate electrode and said exposed portion of said substrate.

2. The method of claim 1, wherein removing the portion of said layer of electrically insulating material below said central portion of each of said one or more elongated semiconductor lines comprises: forming a first feature over a first end portion of each of said one or more elongated semiconductor lines; forming a second feature over a second end portion of each of said one or more elongated semiconductor lines, wherein the central portion of each of said one or more elongated semiconductor lines and a portion of said layer of electrically insulating material are exposed between said first and the second feature; and performing an etch process adapted to selectively remove a material of said layer of electrically insulating material relative to a material of said one or more elongated semiconductor lines and one or more materials exposed at surfaces of said first and the second feature.

3. The method of claim 2, wherein said etch process is substantially isotropic.

4. The method of claim 3, wherein said first feature comprises a raised source region, a first portion of a sidewall spacer formed above the first end portion of each of said one or more elongated semiconductor lines, and a first portion of a layer of dielectric material formed above said raised source region; and wherein the second feature comprises a raised drain region, a second portion of the sidewall spacer formed above the second end portion of each of said one or more elongated semiconductor lines, and a second portion of a layer of dielectric material formed above said raised drain region.

5. The method of claim 4, wherein the formation of said first feature and said second feature comprises: forming a dummy gate structure over the central portion of each of said elongated semiconductor lines; forming the sidewall spacer adjacent said dummy gate structure; performing a selective growth process, said selective growth process forming said raised source region and said raised drain region; depositing the layer of dielectric material over said dummy gate structure, said raised source region and said raised drain region; planarizing the layer of

dielectric material, wherein the planarization exposes said dummy gate structure; and performing one or more etch processes to selectively remove said dummy gate structure.

6. The method of claim 5, further comprising forming a silicide in said raised source region and said raised drain region before the deposition of said layer of dielectric material.

7. The method of claim 5, further comprising in situ doping said raised source region and said raised drain region during said selective growth process.

8. The method of claim 7, further comprising performing an annealing process, wherein dopants from said raised source region diffuse into the first end portion of each of said elongated semiconductor lines and form a source region, and dopants from said raised drain region diffuse into the second end portion of each of said elongated semiconductor lines and form a drain region.

9. The method of claim 1, wherein the formation of said one or more elongated semiconductor lines comprises: providing a semiconductor-on-insulator structure, said semiconductor-on-insulator structure comprising a layer of a semiconductor material, said substrate and said layer of electrically insulating material, said layer of electrically insulating material being provided between said substrate and said layer of semiconductor material; and performing an etch process, said etch process removing portions of said layer of semiconductor material, wherein one or more other portions of said layer of semiconductor material are not removed in said etch process and form said one or more elongated semiconductor lines.

10. The method of claim 1, wherein said gate insulation layer comprises a high-k material having a greater dielectric constant than silicon dioxide and said gate electrode comprises a metal.

11. The method of claim 1, wherein forming said gate insulation layer comprises performing a thermal oxidation process.

12. The method of claim 1, wherein forming said gate insulation layer comprises performing a chemical vapor deposition process.

13. A method, comprising: forming an elongated semiconductor line on a layer of electrically insulating material that is positioned on a substrate comprised of a semiconductor material, wherein a longitudinal direction of said one elongated semiconductor line extends substantially along a horizontal direction that is perpendicular to a thickness direction of said substrate; forming a dummy gate structure over the central portion of said elongated semiconductor line; forming a sidewall spacer adjacent said dummy gate structure; performing a selective growth process to form a raised source region above a first end portion of said elongated semiconductor line and a raised drain region above a second end portion of said elongated semiconductor line; depositing a layer of dielectric material over said dummy gate structure, said raised source region

and said raised drain region; planarizing the layer of dielectric material, wherein the planarization exposes said dummy gate structure; performing one or more etch processes to selectively remove said dummy gate structure to expose a central portion of said elongated semiconductor line and thereby define a gate cavity laterally defined by the sidewall spacers; performing an etching process through the gate cavity to remove at least a portion of said layer of electrically insulating material below said central portion to expose said substrate; forming a gate insulation layer on said central portion of said elongated semiconductor line and said exposed portion of said substrate; and forming a gate electrode extending all around said central portion of said elongated semiconductor line, said gate insulation layer providing electrical insulation between said elongated semiconductor line and said gate electrode and between said gate electrode and said previously exposed portion of said substrate.

14. The method of claim 13, wherein forming said gate insulation layer comprises performing a thermal oxidation process.

15. The method of claim 13, wherein forming said gate insulation layer comprises performing a chemical vapor deposition process.

16. The method of claim 13, wherein said etching process is substantially isotropic.

17. The method of claim 13, further comprising forming a silicide in said raised source region and said raised drain region before the deposition of said layer of dielectric material.

18. The method of claim 13, further comprising in situ doping said raised source region and said raised drain region during said selective growth process.

19. The method of claim 13, further comprising performing an annealing process, wherein dopants from said raised source region diffuse into the first end portion of said elongated semiconductor line and form a source region, and dopants from said raised drain region diffuse into the second end portion of said elongated semiconductor line and form a drain region.

20. The method of claim 13, wherein the formation of said elongated semiconductor line comprises: providing a semiconductor-on-insulator structure, said semiconductor-on-insulator structure comprising a layer of a semiconductor material, said substrate and said layer of electrically insulating material, said layer of electrically insulating material being provided between said substrate and said layer of semiconductor material; forming a patterned masking layer above the layer of semiconductor material; and performing an etch process through the patterned masking layer to remove exposed portions of said layer of semiconductor material, thereby resulting in the formation of the elongated semiconductor line.

21. A semiconductor formed in accordance with the method of any one of the preceding claims.