

ABSTRACT

Embodiments of the disclosure provide a memory, which includes: a clock generation circuit, configured to generate a first oscillation signal and a second oscillation signal. The first oscillation signal and the second oscillation signal have a same frequency but opposite phases, and a duty cycle of the first oscillation signal and a duty cycle of the second oscillation signal are both within a first preset range. And the memory further includes a differential input circuit, which is configured to receive a first external signal and a second external signal, and generate a first internal signal and a second internal signal. Herein, the clock generation circuit is further configured to monitor at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal, and enable the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal to be within a second preset range. According to the embodiments of the disclosure, the memory has a Duty Cycle Monitor (DCM) function and a Duty Cycle Adjust (DCA) function, and also can achieve detection and calibration on the differential input circuit.

Fig. 3