

ABSTRACT

It is possible to let a display, on which pixels are fixed
in number for display, display every video signal with a simple
5 circuit structure.

A one-clock delay circuit (1) delays a reference signal (9)
by one clock for output, a multiplexer (2) switches between the
one-clock-delayed signal and the reference signal (9) for output,
an A/D converter (3) subjects a video signal (24) to two-phase
10 processing with reference to an output signal from the multiplexer
(2), and a comparator (8) outputs a control signal (12) to the
multiplexer (2) to let the multiplexer (2) to select the one-
clock delayed signal when determining, based on a result obtained
by detection in the first and second back porch detection circuits
15 (6) and (7), that a head of video data is not included in first
phase output data.