METHOD OF TRANSFERRING A CIRCUIT ONTO A GROUND PLANE

DESCRIPTION

STATE OF THE PRIOR ART

The invention concerns the formation of novel structures for semi-conductor components or MEMS type devices, and particularly SOI or SOI type devices.

Numerous microsystems or MEMS (Micro Electro Mechanical Systems) are formed by means of SOI (Silicon On Insulator) materials that make it possible in particular to obtain membranes of monocrystalline silicon suspended above a cavity.

SOI type materials are structures composed of a superficial layer 2 in monocrystalline silicon on an insulator layer 4, in general in silicon oxide (figure 1). These structures are obtained for example by assembly by molecular adhesion of a wafer 6 of silicon oxidised on the surface, with another wafer of silicon.

This assembly comprises a step of surface preparation of two wafers, a step of bringing into contact and a step of heat treatment. Conventionally, this heat treatment is carried out at temperatures between, typically, 900° and 1250°C for 2h.

Then, at least one of the two wafers is thinned, leaving behind a thin semi-conductor layer 2 on an insulator layer 4.

The thinning may take place by different mechanical or chemical means, or by separation at the

level of a brittle layer created for example by ion implantation.

For certain applications, it is profitable to obtain circuits on a metallic ground plane.

In the case of SOI circuits, one aims for instance to properly control the density of the carriers on the rear face of the circuit, itself formed in the superficial layer 2.

To achieve this, it is necessary that the SOI circuit, formed in the layer 2 and superficial to the buried layer 4, of low thickness (for example a layer of silicon oxide), is such that the array constituted by said circuit and the buried layer 4 is on an electrically conducting layer, or metallic ground plane. To do this it is profitable to have a buried oxide of very low thickness, for example 10 nm to 50 nm. It is thereby possible to control the density of the carriers in the layer of the semi-conductor in the vicinity of the interface by the intermediary of the potential difference applied to the conducting buried layer and to the semi-conducting layer.

However, it is difficult to obtain SOI wafers with a thin dielectric layer 4 and a metallic ground plane, because the wafers could not then undergo heat treatments at high temperature necessary for the formation of circuits or components.

One may on the other hand transfer, after formation of circuits on SOI material, the circuits onto wafers containing a metallic ground plane. One possibility is to transfer the layer containing the

circuits onto a layer with a metallic deposition by double transfer techniques using molecular adhesion.

But from a technological point of view, this is difficult to implement, because it is difficult to have a direct bonding between a metallic layer and an oxide, especially when this is of low thickness, without having bonding defects.

The problem is therefore posed of being able to form a structure comprising a SOI type circuit or comprising a layer of circuits on a buried layer and a ground plane under this circuit or this buried layer.

DESCRIPTION OF THE INVENTION

The invention firstly concerns a method for forming a semi-conducting structure, comprising:

a) the formation of at least all or part of a component or a circuit, in or on the superficial layer of a substrate, comprising said superficial layer, a buried layer underneath the superficial layer, and an underlying layer serving as first support,

b) a transfer of this substrate onto a handle substrate, and then an elimination of the first support,

c) the formation of a layer forming a ground plane on the buried layer,

d) the formation, on the layer forming a ground plane, of a bonding layer,

e) a transfer of the structure thus obtained onto a second support and an elimination of the handle substrate.

In this first case, the bonding layer may be electrically insulating, for example chosen among SiO2, Si3N4, SiON or other. It may also be electrically conducting, for example in doped Si or in doped polycrystalline Si.

The invention further concerns a method for forming a semi-conducting structure, comprising:

a) the formation of at least all or part of a component or a circuit, in or on the superficial layer of a substrate, comprising said superficial layer, a buried layer underneath the superficial layer, and an underlying layer serving as first support,

b) a transfer of this substrate onto a handle substrate, then an elimination of the first support,

c) the formation of a layer in heavily doped semi-conductor material, forming both bonding layer and electrically conducting layer or ground plane on the buried layer,

d) a transfer of the resulting structure onto a second support and an elimination of the handle substrate.

According to the invention, one forms a circuit on a substrate comprising a superficial layer, a buried layer, for example in silicon oxide, thick or thin, underneath the superficial layer, and a first support.

This strtucture is then assembled on a wafer, for example in semi-conductor, which acts as a handle.

One may then thin the substrate, so as to eliminate the first support up to the level of the buried layer.

This step of thinning may be carried out for example by mechanical thinning and/or chemical attack.

In the first case, the layer forming a ground plane may be in a metallic material or in a heavily doped semi-conductor material. Its lateral extension may be limited, and it may therefore only cover part of the buried layer. In the second case, the layer forming a ground plane also forms a bonding layer.

The transfer step may be carried out by molecular adhesion or by bonding by means of an adhesive substance such as an adhesive, a resin, etc.

After the step b), a step of thinning of the buried layer of the substrate may be carried out, for example by mechanical and/or chemical means (wet or dry). One may therefore adapt the thickness of the buried layer to the desired thickness.

The superficial layer may be in semi-conductor material, for example in silicon or in germanium, or in a III-V, II-VI semi-conductor, or in a mixed semi-conductor, for example in SiGe.

The initial substrate may be a SOI substrate.

The component or circuit may be an electronic or optoelectronic or MEMS type component.

The invention further concerns a semi-conductor device comprising a superficial layer of

circuits or components, a first buried layer in a dielectric material, a second buried layer forming conducting layer or ground plane, if necessary of limited lateral extension, a third buried bonding layer, and a substrate.

The layer forming a ground plane may be in a metallic material or in heavily doped semi-conductor.

The invention further concerns a semi-conductor device comprising a superficial layer of circuits or components, a first buried layer in a dielectric material, a second buried layer in a heavily doped semi-conductor material, forming both bonding layer and electrically conducting layer, or ground plane, and a substrate.

In both cases, the superficial layer, in which are formed the circuits, may be in semi-conductor, for example in silicon or in germanium, or in a III-V, II-VI semi-conductor, or in a mixed semi-conductor, for example in SiGe.

The first buried layer may be an electrical insulator, such as silicon dioxide, or thermal silica or a multilayer for example of SiO2/Si3N4 type.

BRIEF DESCRIPTION OF DRAWINGS

Figure 1 represents a SOI structure.

Figure 2 represents a component according to the invention.

Figures 3A-3E represent the steps of a method according to the invention.

Figure 4 represents another component according to the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Figure 2 represents a device or component according to the invention, comprising, on a substrate 30, a bonding layer 12, a layer 14 forming a ground plane, a dielectric layer 4 and finally a layer 2 of circuits.

The layer 2-layer 4 array forms an "SOI circuit".

The layer 14 may be metallic or in heavily doped semi-conductor material (for example in silicon). This layer may be only local and not uniform or continuous, for example it may be under certain components only.

The bonding layer 12 may be electrically insulating; this may be an oxide, for example SiO2. It may also be chosen among, for example, Si3N4, SiON or other.

It may also be electrically conducting, then being for example in doped amorphous Si or in doped polycrystalline Si, or even in doped Si.

The bonding interface may be localised between the bonding layer 12 and the substrate support 30. This interface may also, in the case where a bonding layer is deposited both on the ground plane and on the support 30, be localised in the middle of the bonding layer itself.

By way of example, the layer 4 has a thickness for example between 10 nm and 500 nm or 1 µm, and the layer 2 a thickness between 10 nm and 1 µm or 10 µm. The metallic layer may have a thickness between 100 nm and 500 nm, and the bonding layer a thickness

between 500 nm and several µm, for example 5 µm. All of these thickness ranges can vary outside of the ranges indicated.

If there is a topology on the rear face (ground plane 14 side) it may be advantageous to carry out a planarisation before the step of bonding or before the deposition of the conducting layer.

A method for forming such a component will now be described, while referring to figures 3A to 3G.

A SOI wafer initially comprises, as illustrated in figure 1, a support 6, a buried layer 4 and a superficial layer 2. This latter layer is for example in silicon, but it can also be in germanium, or in a III-IV, or II-VI semi-conductor, or in a mixed semi-conductor, such as SiGe for example.

On this SOI wafer (figure 3A), one forms circuits 18 or all or part of a component in the layer 2.

The array is then assembled (figure 3B), by the side of the layer 2 of circuits, with a handle substrate 20, by bonding for example by molecular adhesion. Such bonding has the advantage of being compatible with thermal methods, at more or less high temperatures, unlike bonding with adhesive or resins.

The support 6 may then be eliminated for example by mechanical, and/or mechanical-chemical, and/or chemical thinning (figure 3C).

One may then adapt the thickness of the buried layer 4 to the desired thickness. This step

makes it possible to properly control the effect of the conducting layer through the dielectric layer 4.

The thinning of this layer 4 is in a preferential manner carried out by CMP (chemical mechanical polishing) or by chemical attack (wet or dry etching) down to low thickness, for example from 10 nm to 50 nm.

One then forms, on the layer 4, a conducting layer 14 (figure 3D), for example by gas phase chemical deposition. This layer may be for example in copper, or in aluminium or in doped silicon, or in tungsten silicide (WSi2).

This layer may cover the entire surface or be localised according to patterns for the needs of the application; one then uses lithographic and etching techniques to delimit the zones with this conducting layer and the zones without this conducting layer. For instance, the conducting layer may be only local, for example under certain components.

On this conducting layer 14, another layer 12 in a material making it possible to facilitate a bonding on a substrate, particularly of semi-conductor type, may be deposited or formed. This bonding layer 12 is for example a layer of silicon oxide or a layer of amorphous or polycrystalline silicon. Depending on the nature of the bonding layer, there may therefore be electrical conduction between the ground plane and the substrate or an electrical insulation. In the case of an electrical insulation, the contact of the conducting layer may be taken by the front face or by the rear face of the structure. In the case of a conducting

bonding layer, the contact may be taken by the rear face.

This bonding layer 12 may be a thick layer, for example greater than 100 nm, which makes it possible to obtain a good quality of bonding.

The fact of placing a bonding layer on the ground plane makes it possible to free oneself of the characteristics of the conducting layer 14, in particular of the thickness, and/or the roughness of said layer.

It is then possible to transfer the array, for example by bonding by molecular adhesion onto another substrate 30 (figure 3E). If a topology is present on the rear face (on the side to assemble with the substrate 30), a planarisation may be carried out.

For instance, one may easily transfer the structure by assuring a good control of the bonding, the bonding by molecular adhesion making it possible to assure no or few defects and a high bonding energy. Moreover, it is compatible with the carrying out of subsequent microelectronic steps. One may also use a bonding by means of an adhesive substance, such as a glue or a resin.

After this transfer step, the handle wafer 20 that served as manipulator to thin the initial wafer may be eliminated, for example by mechanical and/or chemical thinning or by disbonding at the level of the bonding interface between front face and handle.

One has for instance a structure such as that of figure 2 with SOI circuits containing a thin oxide 4 on a ground plane 14.

The whole lies on a layer 12 that has made it possible to assure the bonding of the structure on a new support 30.

Figure 4 represents another component according to the invention, comprising, on a substrate 30, a layer 34 in heavily doped semi-conductor material, forming a ground plane and bonding layer, a dielectric layer 4 and finally a layer 2 of circuits. The doping of the layer 34 enables the resistivity of said layer to be at the most around several $m\Omega/cm^2$, for example at the most around 10 $m\Omega/cm^2$ or 100 $m\Omega/cm^2$. It is for example a layer of doped polysilicon.

The layer 2 - layer 4 array forms a "SOI type circuit".

The formation of such a device may be described while referring to figures 3A - 3E: the steps are the same, except for the formation of the metallic layer 14 and the bonding layer 12, which are replaced by a unique layer 34.

CLAIMS

1. Method for forming a semi-conducting structure, comprising:

a) the formation of at least one part of a circuit or a component, in or on the superficial layer (2) of a substrate, comprising said superficial layer (2), a dielectric buried layer (4) underneath the superficial layer, and an underlying layer (6) serving as first support,

b) a transfer of this substrate onto a handle substrate (20) then an elimination of the first support (6),

c) the formation of an electrically conducting or ground plane forming layer (14), on at least one part of the buried dielectric layer (4),

d) the formation, on this electrically conducting or ground plane forming layer (14), of a bonding layer (12),

e) a transfer of the structure obtained onto a second support (30) and an elimination of the handle substrate (20),

thereby forming a structure comprising:

- said superficial layer (2) comprising at least part of said component or of said circuit,
- said buried dielectric layer (4),
- said electrically conducting or ground plane forming layer (14),
- said bonding layer (12), and
- said second support (30).

2. Method according to claim 1, the bonding layer (12) being electrically insulating.

3. Method according to claim 2, the bonding layer (12) being an oxide, for example SiO2, or being chosen in Si3N4, or in SiON.

4. Method according to claim 1, the bonding layer (12) being electrically conducting, for example in doped semi-conductor, for example in doped Si or in doped polycrystalline Si.

5. Method according to one of claims 1 to 4, the conducting or ground plane forming layer (14) being in a metallic material or in a heavily doped semi-conductor material.

6. Method according to one of claims 1 to 5, the electrically conducting or ground plane forming layer being formed locally, without covering the entire buried layer.

7. Method for forming a semi-conducting structure, comprising:

a) the formation of at least one part of a circuit or a component, in or on the superficial layer (2) of a substrate, comprising said superficial layer (2), a buried dielectric layer (4) underneath the superficial layer, and an underlying layer (6) serving as first support,

b) a transfer of this substrate onto a handle substrate (20) then an elimination of the first support (6),

c) the formation of a layer (14) in heavily doped semi-conductor material, forming a ground plane and bonding layer, on at least one part of said buried dielectric layer (4),

d) a transfer of the structure obtained onto a second support (30) and an elimination of the handle substrate (20),

whereby forming a structure comprising:

- said superficial layer (2) comprising at least part of said component or of said circuit,
- said buried layer (4),
- said heavily doped semiconductor layer (14) forming a ground plane and bonding layer, and
- said second support (30).

8. Method according to one of claims 1 to 7, the step e) or d) of transfer being carried out by molecular adhesion.

9. Method according to one of claims 1 to 8, further comprising, after the step b), a step of thinning of the buried layer (4) of the substrate.

10. Method according to one of claims 1 to 9, the superficial layer (2) being in semi-conductor, for example in silicon or in germanium, or in a III-V, II-VI semi-conductor, or in a mixed semi-conductor, for example in SiGe.

11. Method according to one of claims 1 to 10, the substrate being a SOI substrate.

12. Semi-conductor device comprising a superficial layer (2) containing all or part of circuits or components, a first buried layer (4) in a dielectric material, a second buried electrically conducting or ground plane forming layer (14), a third buried bonding layer (12), and a substrate (30):

- said first buried layer (4) lying between said superficial layer (2) and said second buried electrically conducting or ground plane forming layer (14), and

- said second buried electrically conducting or ground plane forming layer (14) lying between said first buried layer (4) and said third buried bonding layer (12).

13. Device according to claim 12, the layer (14) forming a ground plane being in a metallic material or in a heavily doped semi-conductor material.

14. Device according to claim 12 or 13, the bonding layer (12) being electrically insulating.

15. Device according to claim 14, the bonding layer being an oxide, for example SiO2, or being chosen in Si3N4 or in SiON.

16. Device according to claim 12 or 13, the bonding layer (12) being electrically conducting, for

example in doped semi-conductor, for example in doped Si or in doped polycrystalline Si.

17. Method according to one of claims 12 to 16, the electrically conducting or ground plane forming layer being formed locally, without covering all of the buried layer.

18. Semi-conductor device comprising a superficial layer (2) of circuits, a first buried layer (4) in a dielectric material, a second buried layer (14) in a heavily doped semi-conductor material forming a ground plane and bonding layer, and a substrate (30):

- said first buried layer (4) lying between said superficial layer (2) and said second buried layer (14), and

- said second buried layer (14) lying between said first buried layer (4) and said substrate (30).

19. Device according to one of claims 12 to 18, the superficial layer (2), in which are formed the circuits, being in semi-conductor, for example in silicon or in germanium, or in a III-V, II-VI semi-conductor, or in a mixed semi-conductor, for example in SiGe.

20. Device according to one of claims 12 to 19, the first buried layer (4) being an electrical insulator, such as silicon dioxide.