WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a first power rail formed in a first rail opening within a first isolation trench on a substrate;

a first power input structure configured to connect with a first terminal of a power source that is external of the semiconductor device to receive electrical power from the power source;

a circuit that is formed, on the substrate, of layers between the first power rail and the first power input structure, the layers extending in a direction parallel to a surface of the substrate; and

a first middle-of-line rail that is formed by one or more of the layers that form the circuit, the first middle-of-line rail being configured to deliver the electrical power from the first power input structure to the first power rail along the direction, the first power rail providing the electrical power to the circuit for operation, topmost and bottommost ones of the layers of the first middle-of-line rail being as high as and leveled with top and bottom surfaces of the circuit, respectively.

2. The semiconductor device of claim 1, further comprising:

a second power rail formed in a second rail opening within a second isolation trench on the substrate, the second power rail being parallel with the first power rail;

a second power input structure configured to connect with a second terminal of the power source, and to receive, in conjunction with the first power input structure, the electrical power from the power source; and

a second middle-of-line rail that is formed by the one or more of the layers that form the circuit, the second middle-of-line rail being parallel with the first middle-of-line rail, and the first and second middle-of-line rails being configured to deliver the electrical power from the first and second input structures to the first and second power rails, the first and second power rails providing the electrical power to the circuit for operation.

3. The semiconductor device of claim 1, wherein:

the circuit includes a cell row of cell circuits that have a same cell height; and

the first middle-of-line rail includes a section in a power tap cell that is disposed in the cell row, the power tap cell having the same cell height as the cell circuits.

4. The semiconductor device of claim 3, wherein:

the first middle-of-line rail is formed by at least a layer that is used to form connections within a cell circuit.

5. The semiconductor device of claim 3, wherein:

the circuit includes multiple cell rows of cell circuits; and

the first middle-of-line rail is formed of sections respectively in power tap cells disposed in the multiple cell rows.

6. The semiconductor device of claim 5, wherein

the power tap cells are aligned in a column, and the sections in the respective power tap cells are conductively connected to form the first middle-of-line rail.

7. The semiconductor device of claim 5, wherein each section of the sections in the respective power tap cells is connected to the first power rail by at least a power via, and is connected to a metal rail by at least a contact.

8. The semiconductor device of claim 2, wherein:

the first and second middle-of-line rails are perpendicular to the first and second power rails.

9. The semiconductor device of claim 1, wherein:

the circuit includes a first transistor that is disposed above a second transistor in a vertical direction that is perpendicular to a surface of the substrate.

10. The semiconductor device of claim 9, wherein:

the first middle-of-line rail includes a first layer for forming a local interconnect in the first transistor, a second layer for forming a local interconnect in the second transistor, and a strap layer to merge the first layer and the second layer.

11. A method for fabricating a semiconductor device, comprising:

forming, in a first rail opening in a first isolation trench on a substrate, a first power rail;

forming, a first power input structure for coupling with a first terminal of a power source that is external of the semiconductor device to receive electrical power from the power source; and

forming, a circuit and a first middle-of line rail in layers between the first power rail and the first power input structure, the first middle-of-line rail delivering the electrical power from the first power input structure to the first power rail, and the first power rail providing the electrical power to the circuit for operation, topmost and bottommost ones of the layers of the first middle-of-line rail being as high as and leveled with top and bottom surfaces of the circuit, respectively.

12. The method of claim 11, further comprising:

forming, in a second rail opening within a second isolation trench on the substrate, the second power rail that is parallel with the first power rail;

forming, a second power input structure for coupling with a second terminal of the power source to receive the electrical power form the power source; and

forming, a second middle-of-line rail in the layers that form the circuit, the second middle-of-line rail being parallel with the first middle-of-line rail, and the first and second middle-of-line rails delivering the electrical power from the first and second input structures to the first and second power rails, the first and second power rails providing the electrical power to the circuit for operation.

13. The method of claim 11, wherein forming, the circuit and the first middle-of-line rail in layers between the first power rail and the first power input structure further comprises:

forming a cell row of cell circuits and at least a power tap cell that has a same height as the cell circuits, the power tap cell including a section of the first middle-of-line rail.

14. The method of claim 13, further comprising:

using at least a layer that is used to form connections within a cell circuit to form, the first middle-of-line rail.

15. The method of claim 13, further comprising:

forming multiple cell rows of cell circuits with power tap cells disposed in the multiple cell rows; and

forming the first middle-of-line rail using respective sections in the power tap cells.

16. The method of claim 15, further comprising:

forming the power tap cells that are aligned in a column.

17. The method of claim 15, wherein each section of the sections in the respective power tap cells is connected to the first power rail by at least a power via, and is connected to a metal rail by at least a contact.

18. The method of claim 12, wherein:

the first and second middle-of-line rails are perpendicular to the first and second power rails.

19. The method of claim 11, further comprising:

forming the circuit having a first transistor that is disposed above a second transistor in a vertical direction that is perpendicular to a surface of the substrate.

20. The method of claim 19, further comprising:

forming the first middle-of-line rail in a first layer that is used for forming local interconnects in the first transistor, a second layer that is used for forming local interconnects in the second transistor, and a strap layer that merges the first layer and the second layer.