

CLAIMS

1. A semiconductor processing chamber, comprising:
 - a showerhead;
 - a pedestal configured to support a semiconductor substrate, wherein the showerhead and pedestal at least partially define a processing region within the semiconductor processing chamber;
 - a spacer characterized by a first surface in contact with the showerhead and a second surface opposite the first surface; and
 - a pumping liner characterized by a first surface in contact with the spacer, and a second surface opposite the first surface, wherein the pumping liner defines a plurality of apertures within the first surface of the pumping liner.
2. The semiconductor processing chamber of claim 1, wherein the spacer comprises an annulus, and wherein an inner annular sidewall of the spacer extending between the first surface of the spacer and the second surface of the spacer at least partially defines the processing region.
3. The semiconductor processing chamber of claim 2, wherein the inner annular sidewall of the spacer is at least partially characterized by an arcuate profile extending away from the processing region in a direction towards the second surface of the spacer.
4. The semiconductor processing chamber of claim 3, wherein the inner annular sidewall of the spacer at the second surface of the spacer is positioned radially outward of the plurality of apertures within the first surface of the pumping liner.
5. The semiconductor processing chamber of claim 1, wherein the second surface of the spacer is seated on the pumping liner.
6. The semiconductor processing chamber of claim 1, wherein the pumping liner comprises an annulus characterized by an inner annular sidewall and

an outer annular sidewall, and wherein the pumping liner defines a plenum between the inner annular sidewall and the outer annular sidewall.

7. The semiconductor processing chamber of claim 6, wherein the plurality of apertures provide fluid access to the plenum from the first surface of the pumping liner.

8. The semiconductor processing chamber of claim 6, wherein the inner annular sidewall of the pumping liner extends vertically to define a rim protruding from the first surface of the pumping liner at the inner annular sidewall.

9. The semiconductor processing chamber of claim 8, wherein the pedestal is vertically translatable within the processing region of the semiconductor processing chamber, and wherein the pedestal comprises a platen and a stem extending from a backside of the platen.

10. The semiconductor processing chamber of claim 9, wherein, when the pedestal is in a raised operational position proximate the showerhead, a plane across the backside of the platen is maintained below an upper surface of the rim protruding from the first surface of the pumping liner.

11. A method of semiconductor processing, the method comprising:
flowing an etchant precursor into a remote plasma region of a semiconductor processing chamber;
generating plasma effluents of the etchant precursor within the remote plasma region of the semiconductor processing chamber;
flowing the plasma effluents of the etchant precursor through a showerhead into a processing region of the semiconductor processing chamber;
contacting a substrate with the plasma effluents, wherein the substrate is seated on a pedestal; and
exhausting etch byproducts from the processing region through a pumping liner characterized by a first surface facing the showerhead and a second surface

opposite the first surface, wherein the pumping liner defines a plurality of apertures within the first surface of the pumping liner.

12. The method of semiconductor processing of claim 11, wherein the semiconductor processing chamber further comprises a spacer characterized by a first surface in contact with the showerhead and a second surface opposite the first surface and in contact with the pumping liner, wherein the spacer comprises an annulus, and wherein an inner annular sidewall of the spacer extending between the first surface of the spacer and the second surface of the spacer at least partially defines the processing region.

13. The method of semiconductor processing of claim 12, wherein the inner annular sidewall of the spacer is at least partially characterized by an arcuate profile extending away from the processing region in a direction towards the second surface of the spacer.

14. The method of semiconductor processing of claim 13, wherein the inner annular sidewall of the spacer at the second surface of the spacer is positioned radially outward of the plurality of apertures within the first surface of the pumping liner.

15. The method of semiconductor processing of claim 11, wherein the pumping liner is further characterized by an inner annular sidewall, and wherein the inner annular sidewall extends vertically to define a rim protruding from the first surface of the pumping liner at the inner annular sidewall.