(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
27 June 2002 (27.06.2002)

PCT

(10) International Publication Number
WO 02/051217 A3

(51) International Patent Classification[7]: H01L 23/02, 23/544, 21/50

(21) International Application Number: PCT/IL01/01183

(22) International Filing Date:
19 December 2001 (19.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
140482 21 December 2000 (21.12.2000) IL
09/758,906 11 January 2001 (11.01.2001) US

(71) Applicant *(for all designated States except US)*: **SHELL-CASE LTD.** [IL/IL]; Manhat Technology Park, P.O. Box 48328, 96251 Jerusalem (IL).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **BADIHI, Avner** [IL/IL]; 6 Nataf Street, 90804 Mobile Post Harei Yehuda (IL).

(74) Agents: **SANFORD T. COLB & CO.** et al.; P.O. Box 2273, 76122 Rehovot (IL).

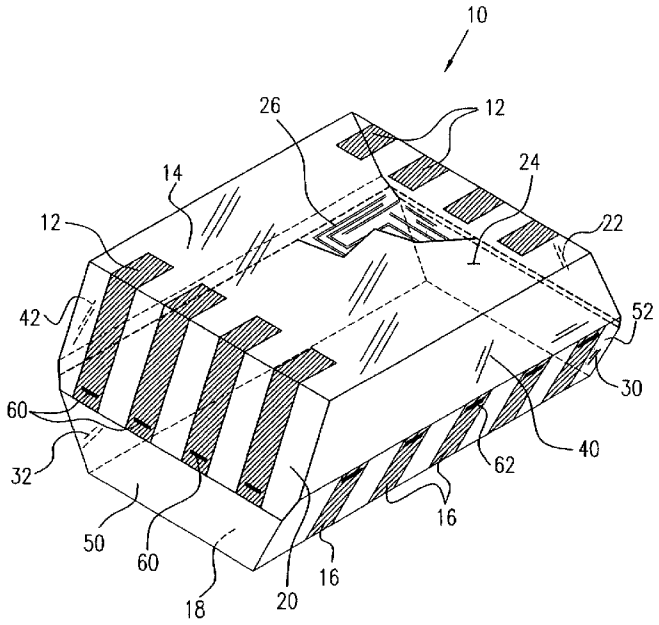
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

[Continued on next page]

(54) Title: PACKAGED INTEGRATED CIRCUITS AND METHODS OF PRODUCING THEREOF



(57) Abstract: A packaged integrated circuit (10) and method for producing thereof including an integrated circuit substrate lying in a substrate plane (24) and having electrical circuitry formed thereon, a package enclosing the integrated circuit substrate and defining first and second planar surfaces generally parallel to the substrate plane and a plurality of electrical contacts, each connected to the electrical circuitry at the substrate plane, at least some of the plurality of electrical contacts extending onto the first planar surface (20) and at least some of the plurality of electrical contacts extending onto the second planar surface (22).

WO 02/051217 A3

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
24 July 2003

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.