[0021] The microelectronic package 100 may further include a memory die 130. Similarly to the description of the package substrate 140, the memory die 130 may be formed one or more layers of an organic or inorganic dielectric material. In some embodiments, the layers may be physically different from one another, e.g. laminated or deposited at different times, while in other embodiments the memory die 130 may be a unitary element such that the layers discussed herein are only logical separations for the sake of discussion.

[0022] Specifically, the memory die may include a complementary metal-oxide semiconductor (CMOS) layer 125 and a number of n-type metal-oxide-semiconductor (NMOS) layers 120a and 120b (collectively, "NMOS layers 120"). Generally, the CMOS layer 125 may have a number of CMOS elements or circuits which may act as control logic for the memory die 130. One such logic is logic 145 which may be or include circuitry which may control memory cells of the NMOS layers 120. For example, the logic 145 may be a decoder, a sensing amplifier, or some other type of logic. It will be understood that although only two NMOS layers are depicted in Figure 1, real-world embodiments may have between one and four layers, while other embodiments may have up to 128 layers or beyond. Additionally, it will be understood that the memory die may have additional layers such as routing layers or other types of layers that are not depicted in Figure 1.

[0023] The NMOS layers 120a/120b may include a number of memory cells 140. Generally, respective ones of the memory cells 140 may be an NMOS dynamic random-access memory (DRAM). Specifically, respective ones of the memory cells 140 may be DRAM memory that includes an NMOS transistor, which may also be referred to as an n-type transistor. The NMOS DRAM may have a memory capacity between approximately 1 Gb and approximately 128 GB. In some embodiments, the memory cells 140 may be implemented using passive and active elements that that within the dielectric material of the memory die 130. In other embodiments, the memory cells 140 may be implemented as distinct dies that are within a larger die package of the memory die 130. It will be understood that although respective ones of the NMOS layers 120 are depicted as having one or two memory cells each, in other embodiments an NMOS layers 120 may have between approximately 128 and approximately 1024 memory cells. It will also be understood that one or more of the NMOS layers may have the same number, or a different number, of memory cells as another of the NMOS layers.