METHOD TO FABRICATE ELEVATED SOURCE/DRAIN TRANSISTOR WITH LARGE AREA FOR SILICIDATION

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ABSTRACT

A method for forming a transistor having an elevated source/drain structure is described. A gate electrode is formed overlying a substrate and isolated from the substrate by a gate dielectric layer. Isolation regions are formed in and on the substrate wherein the isolation regions have a stepped profile wherein an upper portion of the isolation regions partly overlaps and is offset from a lower portion of the isolation regions in the direction away from the gate electrode. Ions are implanted into the substrate between the gate electrode and the isolation regions to form source/drain extensions. Dielectric spacers are formed on sidewalls of the gate electrode and the isolation regions. A conductive layer is deposited overlying the substrate, the gate electrode, and the isolation regions and planarized to leave the conductive layer adjacent to the gate electrode and separated from the gate electrode by the dielectric spacers wherein the conductive layer forms elevated source/drain junctions and wherein the elevated source/drain junctions completely overlie the source/drain extensions and wherein an upper portion of the elevated source/drain junctions extends into the stepped portion of the isolation regions thereby completing formation of a MOSFET having an elevated source/drain structure.

(Figure 20)

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