Transfer Method with a treatment of a surface to be bonded

The invention generally concerns the manufacturing of multilayer wafer including materials selected from semiconductor materials, and used in applications in microelectronics, optics, optoelectronics and/or optronics.

More precisely, the invention concerns the processes for transferring from a "top" wafer (or donor wafer – these terms being herein understood as equivalent) a layer of a semiconductor material onto a "handle" (or receiving wafer, or "base" wafer – these terms being herein understood as equivalent), in order to make a multilayer wafer.

Several main types of such processes are known.

Many of these processes imply a bonding step for bonding the handle and the top wafers, before a removal of the excess material from the bonded top wafer.

We will refer to such processes which imply a bonding step as "bond and transfer processes", or "BTP" processes.

It is specified that the definitions and corresponding acronyms given in this document are provided for the purpose of clearly defining the invention which is the subject matter to be protected by this document.

These definitions/acronyms are therefore intended to be used only for the purpose of understanding this particular subject matter. They are not intended to be used for any other purpose, e.g. for the interpretation of other documents such as other patents or patent applications in the name of the Applicant (unless otherwise specified).

The known types of BTP processes include:

- the BESOI-type process (the removal of material from the top wafer is performed through an etching of said top wafer),
- the ELTRAN™-type process (the removal is performed through a detachment of the excess material said detachment resulting from the attack of a porous region of the top wafer),
- the Smart Cut™-type process (the removal is performed through a detachment of the excess material said detachment resulting from the

splitting of the top wafer at an embrittlement region obtained by implantation of the top wafer with at least one species. It is specified that a general description of the main steps of a non limiting embodiment of this type of method can be found in SILICON-ON-INSULATOR TECHNOLOGY: Materials to VLSI, 2nd Edition (Jean-Pierre COLINGE).

The bonding step of such processes is generally performed without adding between the top and handle wafers any adhesive (such as a resin).

We will refer to such bonding without adhesive as "direct bonding". And a BTP comprising such a direct bonding will be referred to as "Direct bonding and transfer process" (DBTP).

For such direct bonding, the surfaces to be bonded must be very smooth (i-e. present a very low roughness).

And it is possible to provide a smooth surface over a first wafer which is to be bonded with a second wafer through a direct bonding, e.g. by building a "bonding layer" (e.g. with an oxide layer) over said first wafer, and/or by submitting the surface of the first wafer to a specific treatment (e.g. polishing, ...).

A bonding of the surfaces of two wafers generates between the bonded surfaces a bonding interface associated with a given bonding energy (the higher this energy the stronger the bond).

The bonding energy obtained by direct bonding two wafers without any additional treatment is sometimes not high enough.

This is the case in particular when it is desired to obtain with the bonding of two or more wafers a multilayer wafer (each initial wafer bringing a "layer" to the multilayer wafer thus obtained), with a high energy bond (i.e. a bonding energy typically greater than 500mJ/m^2) between the bonded wafers. In such cases, the bonded wafers are thus subjected to a "bonding heat treatment" (BHT) which improves the strength of the bonding.

More precisely, such BHT is generally carried out at high temperatures (i.e. at temperatures of 900°C or higher). We will refer to such a high temperature BHT carried out at temperature higher than 900°C as a "HT BHT".

Such HT BHT reinforces the bonding interface and can bring its bonding energy up to a desired level. As an illustration, the bonding energy between a Si wafer and a Si or SiO2 wafer is maximized after a HT BHT at temperatures in the order of 1100-1200°C.

The bonding energy obtained after a HT BHT can e.g. be 2 to 2.5 J/m^2 for a bonding of Si/Si, SiO_2/SiO_2, or Si/SiO_2.

Such HT BHT can therefore allow the manufacturing of multilayer wafers with adequate bonding energy between the bonded layers of the wafer.

However, it can be undesirable to carry out a HT BHT on a multilayer wafer.

This is the case e.g. when the layers of the multilayer wafer have respective coefficients of thermal expansion (CTE) which are significantly different.

In such case indeed, the layers associated to different CTEs will undergo expansions of different magnitudes when exposed to a HT BHT. This can lead to negative effects such as a warp of the wafers, or even the generation of defects such as dislocations in the crystalline structure of the wafers.

It can also be undesirable to carry out a HT BHT on a bonded multilayer wafer for other reasons, e.g. the wafer already comprises components totally or partially elaborated (such wafer is usually called "structured substrate"), or the material of the wafer is likely to be altered by a high temperature treatment (e.g. case of a wafer comprising sharp doping profile like boron, phosphorous or comprising metastable layers that would be altered by HT BHT, like low k materials, high k materials or comprising layers with metallic elements like Al_2O_3 or TiN), ...

In order to avoid such drawbacks and nevertheless obtain a high bonding energy between bonded layers of a multilayer wafer, techniques of high bonding energy at low temperatures have been developed.

In one of these techniques the surfaces to be bonded are "activated" by their exposure to a plasma, before being contacted together.

Such technique will be referred to as "plasma activation" technique.

Plasma activation is advantageous since it allows obtaining high bonding energy with a BHT which is carried out after contacting the surfaces to be bonded, but which remains limited to a low temperature BHT ("LT BHT").

And plasma activation has been proposed for DBTPs as a solution for obtaining a high energy bonding without requiring carrying out a HT BHT on a bonded multilayer wafer.

A general illustration of such known DBTP is given in "Ultra-thin strained-silicon-on-insulator and SiGe-on-insulator created using low-temperature wafer bonding and metastable layers", Taraschi et al., J. Electrochem. Soc. Vol. 151, N° 1, p. 47 (2004).

This article discloses a Smart Cut™-type process in which prior to the wafer bonding step (between a top and a handle wafers) a plasma activation can be carried out on the surfaces to be bonded.

The general principle of such process is illustrated in figure 1, which comprises figures 1a to 1e to show the successive main steps of such a known principle.

Figure 1a shows a top wafer 10, and a handle wafer 20.

The top wafer 10 has been implanted with one or more species in order to form an embrittlement zone 11.

This top wafer 10 is covered by an insulator layer 12.

The surface 100 of this insulator layer is to be contacted with a surface 200 of the handle wafer, for a direct bonding.

These two surfaces 100, 200 shall be referred to as the respective "front" surfaces of wafers 10 and 20.

And the opposite surfaces of these two wafers (respectively surface 110 and surface 210) are referred to as the respective "back" surfaces of these wafers.

Figure 1b shows the activation of the front surfaces 100 and 200 by a plasma, in a plasma chamber.

As illustrated in figure 1c, this activation creates an activated region 101 on the front surface 100 of the top wafer 10, and an activated region 201 on the front surface 200 of the handle wafer 20.

This activation also generates contaminants due to the exposure of the wafers to a plasma.

Such contaminants are more particularly illustrated by references 111 and 211 on the respective back faces 110, 210 of the wafers, as the front faces receive significantly less contaminants than the back faces (as an example, the plasma activation of a silicon wafer typically generates a contaminant concentration of about 2.10^{10} atoms/cm^2 on the "front" surface which is to be activated and which faces the inner space of the plasma chamber, the contaminant concentration being above 10^{11} atoms/cm^2 on the back surface of the wafer).

This is due in particular to the fact that the physical contacts between each wafer and supporting elements (e.g. chucks) associated to the plasma chamber are made on the back surface of the wafer.

In commercially available equipment for microelectronic application, the wafer is disposed on a chuck in the plasma chamber.

The chuck is adapted to perform the following functions:

- receive and hold the wafer very tightly in place during exposure to the plasma,
- regulate the wafer temperature during plasma exposure, by temperature diffusion,
- act as a an electrode to transfer polarisation (bias voltage) to the wafer.

This set of functions that have to be performed by the chuck leads to selecting for making the chuck materials containing elements that are likely to contaminate the surface of the wafer in contact with said chuck (i.e. the back surface of the wafer, since it is the front surface which is directly exposed to the plasma). This material can typically be Al_2O_3 based sintered ceramics.

Figure 1d illustrates the direct bonding of top wafer 10 and handle wafer 20, these two wafers being bonded by their front surfaces. This

bonding generates a multilayer 30 wafer (referred to as an "intermediate" multilayer wafer) which comprises in particular the embrittlement zone 11.

Figure 1e then illustrates the multilayer wafer 35 obtained after a detachment carried out at the embrittlement zone. This wafer 35 can be of the type SOI (Silicon On Insulator), SGOI (SiliconGermanium On Insulator), sSOI (strained Silicon On Insulator), GeOI (Germanium On Insulator), SiCOI (Silicon Carbide On insulator), SOQ (Silicon On Quartz), or any other type.

Figure 1e also illustrates the remaining part of the top wafer (part 15), which has been detached. This part can be treated and reused for a new process, e.g. for constituting a new top or a new handle wafer.

This type of process illustrates that plasma activation could be advantageous for making multilayer wafers through a DBTP.

However, plasma activation is in itself associated with another drawback, related to the contaminants generated by the activation.

Indeed, as mentioned above plasma activation generates a contamination of the wafer which is exposed to the plasma, in particular on the back surface of the wafer.

This "contamination" corresponds to a deposit of metallic elements (e.g. Al, Fe, Ni, Zn, Cr, Ti, Ca, Mg, Y, ...) that may be incorporated in fine particles, on the surface of the wafer, or absorbed in said surface in the case of isolated atoms, molecules or ions.

Such deposit of metallic elements can be observed with levels of contamination in the order of $5.10^{11} - 5.10^{12}$ atoms/cm^2 on at least some areas of the surface of the exposed wafer.

Such concentrations are too high for a multilayer wafer which is to be subject to further thermal treatments (e.g. a high temperature annealing at temperatures above 1000°C for smoothing the surface of the wafer, or further treatments carried out on the multilayer wafer for integrating components into the wafer).

Indeed, the contaminants of a multilayer wafer which would be exposed to such high temperatures treatments would undergo a diffusion in

the volume of the wafer, and significantly alter the properties (in particular the electrical properties) of the wafer and of its components.

And contaminant concentrations such as mentioned above and resulting from a plasma activation are thus significantly higher than the specifications of maximum contamination level generally in use in the industry of manufacturing the multilayer wafers and their associated components (these specifications being in the order of 5.10^{10} atoms/cm2, or even less).

Thus, carrying out a direct bonding transfer process (such as e.g. a Smart Cut™ process) with an activation of the surfaces to be bonded as in the known state of the art, in order to make multilayer wafers, is associated to some drawbacks.

And it is specified that if these drawbacks have been exposed hereabove in reference to a plasma activation, similar drawbacks can also be associated to the activation of a surface which is different from a plasma activation (e.g. an oxidation and/or a chemical activation...).

It is an object of the invention to overcome the above mentioned drawbacks.

For this purpose the invention proposes a method for transferring from a top donor wafer a layer of material onto a receiving handle wafer, the top and receiving wafers comprising respective surfaces to be bonded, the method comprising :

- a treatment step for treating at least a surface to be bonded, the treatment of a given surface of a wafer generating on the opposed surface of said wafer a contamination,
- a bonding step for direct bonding the surfaces to be bonded of the top and handle wafers, in order to form an intermediate multilayer wafer,
- a removal step for removing excess material from the top wafer,

the method being characterized in that during the treatment step only the surface to be bonded of the top wafer is treated.

Preferred but non-limiting aspects of such a method are the following:

- said treatment step is a surface activation step,
- said contamination of the wafer surface which is opposed to the activated surface corresponds to a metallic contaminants concentration above 10^{11} atoms/cm^2,
- said treatment is carried out through the exposure of the surface(s) to be treated to a plasma,
- said removal step is carried out by detaching said excess material from the top wafer,
- said detachment is carried out at an embrittlement zone which has been made by introduction of at least one species in the top wafer,
- said introduction of species is carried out through an implantation of species,
- said implantation is a co-implantation of at least two species,
- said implantation is carried out with a global implantation dose of a few 10^{16} atoms/cm^2,
- said removal step is carried out through a splitting annealing carried out at temperatures remaining under 350°C,
- said temperature for the splitting annealing is in a range between 200°C and 300°C,
- the method comprises :
    - A treatment step for treating at least a surface to be bonded, the treatment of a given surface of a wafer generating on the opposed surface of said wafer a contamination,
    - a bonding step for direct bonding the surfaces to be bonded of the top and handle wafers, in order to form an intermediate multilayer wafer,
    - a removal step for removing excess material from the top wafer,

  the method being characterized in that it comprises between the bonding step and the removal step a cleaning step for removing from the exposed main surfaces of the intermediate multilayer wafer contaminants brought by the treatment step,

- said treatment step is a surface activation step,
- said contamination of the wafer surface which is opposed to the activated surface corresponds to a contaminants concentration above 10^{11} atoms/cm^2,
- said treatment is carried out through the exposure of the surface(s) to be treated to a plasma,
- during the treatment step only a surface of the top wafer is treated,
- said cleaning step is carried out immediately after said bonding step,
- said cleaning step is carried out before any high temperature thermal treatment,
- said cleaning step is a wet cleaning,
- said cleaning step is carried out with a SC2 solution and/or a HF solution,
- said cleaning step is carried out with a mono face cleaning equipment,
- the top wafer is made of Si, or SiGe, SiC, or Ge,
- the handle wafer is made of Si, fused silica, SiC, or glass,
- the method further comprises a high temperature thermal treatment of the structure which comprises the handle wafer and the part of the top wafer which has not been removed,
- said high temperature thermal treatment is carried out at a temperature greater than 900°C.

Other aspects and advantages of the invention shall appear when reading the following description made in reference to the accompanying drawings, on which (in addition to figure 1 which has already be commented in reference to a principal known in the state of the art) :

- figure 2 is a diagrammatical flowchart of a process according to a first embodiment of the invention,
- figure 3 is a diagrammatical flowchart of a process according to a second embodiment of the invention.

It is specified that the two embodiments which shall be presented hereunder can be combined.

It is also specified that on the figures which shall be commented hereunder, the elements and features which are identical or similar to those commented with reference to figure 1 shall be associated to the same reference numeral.

First embodiment

Figure 2 (which comprises figures 2a-2e) shows the main steps of a first embodiment of the invention.

These steps reproduce some of the steps 1a-1e commented above.

Figure 2a thus shows a top wafer 10 with an implanted embrittlement zone 11, and a handle wafer 20.

At this stage the front surfaces 100 and 200 of top wafer 10 and handle wafer 20 can undergo preliminary treatments for preparing the surfaces to be bonded. These preliminary treatments can include a Chemical-Mechanical Polishing (CMP) and/or one or more cleanings with a cleaning solution (such as RCA, SPM+RCA, ...).

The top wafer 10 can be made of Si, SiGe, Ge, SiC, or in any other semiconductor material.

The handle wafer 20 can be made of Si, fused silica, SiC, glass (all these materials being possibly in crystalline, polycrystalline or amorphous form), or in any other semiconductor material.

The embrittlement zone 11 can have been made by introduction of species in the top wafer (this "introduction being carried out e.g. as an implantation and/or by diffusion, or by any other known technique).

In the case where the "introduction" of species is an implantation of species, such implantation can be an implantation of only one species (such as e.g. H or He). It can also have been made by implantation of several species (i.e. co-implantation), for example H and He.

Here again, the front surface 100 of the top wafer is the surface of an oxide layer (e.g. a deposit of SiO2, or an oxidized region of the underlying material).

Figure 2b illustrates an activation step, during which the front surface 100 of the top is exposed to a plasma.

This activation step – like all activation steps mentioned in the different embodiments described in this text – more generally corresponds to a treatment step of a surface to be bonded, with a generation of a contamination on the surface of the wafer which is opposite to the surface treated.

The back surface 110 of top 10 is therefore covered by a region 111 which is contaminated with metallic contaminants such as those mentioned above (see figure 2c).

And as mentioned above, this contamination on the back surface of the top wafer corresponds to contaminant concentrations which is typically higher than the maximum concentration generally tolerated.

It shall be noted that during this activation step, only the top wafer is exposed to a plasma in order to be activated.

The handle wafer 20 is not exposed to any plasma. Therefore, no contamination is deposited on the surfaces of said handle wafer.

This selective exposure of the donor top wafer only is specific to this first embodiment of the invention.

In the known experiments for using a plasma activation in a DBTP, both front surfaces of the top and of the handle wafers were exposed for activation by a plasma. In such experiments, the drawbacks associated to the contamination of a multilayer structure which could undergo further high temperature treatments had not been pointed out.

It is to be noted that a reports on one of such experiments (see "Ultra-thin strained-silicon-on-insulator and SiGe-on-insulator created using low-temperature wafer bonding and metastable layers", Taraschi et al., J. Electrochem. Soc. Vol. 151, N° 1, p. 47 (2004)) mentions the plasma activation of only one of the wafers to be bonded.

But this mention makes reference to the activation of the handle wafer, and not of the top wafer. And not surprisingly, there is no mention in this article of any problem associated to the contamination resulting from the plasma activation.

The following step is the direct bonding of the top wafer and the handle wafer, for making an intermediate multilayer wafer 30 (Figure 2d).

The excess material from the top is then removed.

In the illustration of this first embodiment presented on figures 2a-2e, this removal is carried out by detaching the excess material as delimited in the top by the embrittlement zone 11.

In this particular case which refers to a Smart Cut™-type method, the remainder 15 of the top is detached from the intermediate wafer 30.

The removal can also be carried out according to any method known for BTPs.

This removal can therefore be carried out by etching the back face of the top wafer 10 (i.e. the face of the top wafer which is opposed to the front surface 100), on the intermediate wafer 30.

In such case (which corresponds to a BESOI-type method), it is not necessary that any implantation has been carried out on the top wafer.

The removal step can also be performed in accordance with the ELTRAN® method.

In such case, the embrittlement zone has previously been made by porous material, and here again no implantation is necessary.

In the case of a Smart Cut™-type or ELTRAN™-type method, a remainder 15 shall be obtained.

In every cases (i.e. whatever the method used for removing the excess material of the top), the multilayer wafer 35 obtained does not comprise a heavy contamination generated on a back surface of a wafer whose front surface would have been exposed to a plasma for its activation.

Indeed, in all cases the heavy contamination region 111 which is on the back surface of the top wafer has been removed from the multilayer wafer 35.

This is particularly advantageous since this multilayer wafer shall then undergo additional thermal treatments, some of these thermal treatments being as mentioned before carried out at high temperatures (e.g. smoothing annealing at temperatures above 1000°C).

And exposing a wafer comprising heavy concentrations of contaminants (e.g. concentrations above 10^{11} atoms/cm2) would generate an unacceptable and irreversible diffusion of the contaminants into the wafer.

In the case of a method generating a remainder 15, the only heavy contamination (region 111) is on said remainder, the multilayer wafer 35 being totally free of such heavy contamination.

Therefore, this first embodiment of the invention allows to make a multilayer wafer with a DBTP, without having said multilayer wafer polluted by a heavy concentration of contaminants.

It is specified that the contaminant concentrations which can be observed on the front face of the exposed top after the activation step are in the order of 2.10^{10} atoms/cm2, which is a generally acceptable concentration level.

The removal step illustrated in figure 2e is carried out by detaching the top wafer at the implanted embrittlement zone 11.

This detachment can result from a mechanical and/or thermal action.

In the case of a thermal action (i.e. a splitting annealing), the temperature should be kept at moderated values, in order to avoid any diffusion of contaminants which would have been generated on the front surfaces 100, 200 (and would therefore be located in the vicinity of the bonding interface).

Typical values of moderated temperatures for such splitting annealing are 300-500°C, for a multilayer wafer such as an SOI.

And always in the specific case of the use of a Smart Cut™-type method as illustrated in figures 1a-1e, the implantation of the top for creating the embrittlement zone 11 can advantageously be made with more than one species (co-implantation, e.g. of H+He).

Indeed, such co-implantation allows a reduction of the temperature for the splitting annealing : the splitting at an embrittlement zone created by co-implantation (e.g; H+He into a Si top wafer) occurs (for a given global implantation dose – i.e. the sum of the doses of all implanted species - which can typically be a "standard" implantation dose of e.g. 5.10^{16} atoms/cm^2 – and more generally a few 10^{16} atoms/cm^2) at lower temperatures than it would have occurred in the same top wafer implanted with the same global implantation dose, but with only one species.

For more details on the conditions of such a co-implantation which allows a reduction of the temperature for the splitting annealing, with a "standard" global dose, reference is made to WO/042779.

A co-implantation (e.g. with H+He) therefore constitutes a favourable feature for performing a splitting annealing at moderated temperatures as mentioned above. And such co-implantation even allows a further reduction of the temperature for the splitting annealing.

For a H+He co-implantation in a Si top with a global implantation dose of a few 10^{16} atoms/cm^2, this temperature can remain under 350°C – it can in particular be in a range as low as 200-300°C.

Second embodiment

Figure 3 (which comprises figures 3a-3f) shows the main steps of a second embodiment of the invention.

Figure 3a illustrates – as figures 1a and 2a – a top wafer 10 and a handle wafer 20.

The materials of the top and the handle wafers can be the identical to the materials mentioned in reference to the first embodiment described above.

Here again, the top wafer has been implanted with one or more species for generating an embrittlement zone 11.

But here again, such implanted embrittlement zone is only a particular illustration corresponding to the case where the invention is

embodied with a Smart Cut™-type method, whereas any type of DBTP can be used.

And more generally, unless otherwise specified, all information given above for the first embodiment is applicable to this second embodiment.

Figure 3b illustrates the step of activation through exposure to a plasma.

During this step, the front surface of the top wafer 10 and/or of the handle wafer 20 can be exposed.

If only the top wafer 10 is exposed to a plasma for activation, the first embodiment described above can be combined with the second embodiment.

Figures 3b-3d illustrate the particular case where both top and handle wafers are activated by a plasma.

Figure 3c thus illustrates highly contaminated regions 111 and 211 respectively associated to the back surfaces of the top and the handle wafers.

Of course, if only the top wafer is activated there would be only a region 111 and if only the handle wafer is activated there would be only a region 211.

Figure 3d illustrates the direct bonding of the top and handle wafers, with their front surfaces contacted.

In this second embodiment, the bonding is followed (preferably immediately followed) by a cleaning step (figure 3e) for removing the contaminants from the highly contaminated regions 111 and 211 on the intermediate multilayer wafer 30 (or from the region 111 or 211 which has been formed, if only one such highly contaminated region has been formed because only one wafer was activated by a plasma before bonding).

The region 111 is said to be associated to a first "main" surface of the intermediate multilayer wafer 30, and the region 211 is said to be associated to a second "main" surface of the intermediate multilayer wafer 30.

This cleaning step is carried out on the intermediate multilayer wafer 30 which has been made by the direct bonding of the top and handle wafers, with a cleaning solution able to eliminate contaminants. A SC2 solution or a HF solution can be used for that purpose.

The cleaning step is carried out before the wafer undergoes any high temperature treatment (i.e. any thermal treatment above 900°C).

The "cleaning step" illustrated in figure 3e can be composed of several successive cleanings.

Such cleaning is carried out on the intermediate multilayer wafer 30. This differs from the cleaning operations known in the art since these cleaning are usually carried out on single-layer wafers such as bulk silicon wafers.

Each cleaning of the cleaning step can be carried out as a wet cleaning, i.e. by immersing the wafer to be cleaned in a bath made of the cleaning solution.

It is however also possible to perform such cleaning with a monoface cleaning equipment, which projects a controlled spray or jet of cleaning solution selectively, only on the surface to be cleaned.

Concerning the cleaning step it is to be noted that the applicant has observed that contrary to what one might have expected, the use of a cleaning solution on a multilayer wafer 30 whose layers have already been bonded together produces very satisfactory results.

Indeed, the prior art tends to indicate that such cleaning should be avoided because the cleaning solution might be infiltrated at the bonding interface (see e.g. "Semiconductor on Wafer Bonding: Science and Technology" – Tong and Gösele, sponsored by the Electrochemical Society, Inc., a Wiley-Interscience Publication, 1999). Such infiltrations would be associated to risks of degrading the quality of the bonding, or even undo the bond between the bonded wafers.

In addition, when considering the prior art one would consider that the manipulations associated to a cleaning step would favour debonding of the bonded wafers.

Moreover, one would also consider that the cleaning step would most probably lower the bonding energy at the edge of the bonding interface of the bonded wafer.

Therefore, a cleaning step carried out as in this second embodiment goes against the teachings of the prior art.

And the specific process provided by this second embodiment, which has the cleaning performed after the bonding, further allows to use a solution such as a SC2 or HF solution, which is known to efficiently remove metallic contaminants.

A SC2 or HF solution would indeed have been associated to problems if used for cleaning the top and/or handle wafer before their bonding together : in such case, the SC2 or HF solution would have removed the undesirable contaminants, but would also have deactivated the surfaces to be bonded – thus losing the benefit of the plasma activation.

It therefore appears that the specific method proposed in this second embodiment also corresponds to an advantageous process which allows the manufacturing of a multilayer wafer through a DBTP, with a LT BHT.

Figure 3f illustrates the removal step of the excess material of the top. Here again, all comments made above about the first embodiment are applicable.

An advantage of this second embodiment is that in the case of a removal carried out in a way which generates a remainder (as illustrated in the left part of figure 3f), such remainder has already been cleaned by the cleaning step.

It is specified that if the description given above of embodiments of the invention is focused on the case of an activation (or several activations) carried out through the exposure to a plasma ("plasma activation"), such activation can alternatively be carried out under different forms (e.g. oxidation and/or chemical activation ...).

In all cases the activation is:

- intended to enhance the bonding energy associated to a bonding of the surface which is activated (said surface can generally be be referred to as a "front" surface),
- associated to the generation of a heavy contamination on the "back" surface which is opposed to the "front" surface to be activated (with a "heavy" contamination being understood as corresponding to a contaminant concentration above 10^{11} atoms/cm^2).

And in all embodiments the invention ensures that no wafer surfaces can undergo high temperature thermal treatments if said surface is heavily contaminated.

CLAIMS

1. Method for transferring from a top donor wafer (10) a layer of material onto a receiving handle wafer (20), the method comprising:

a treatment step for treating at least a surface to be bonded, the treatment of a given surface of a wafer generating on the opposed surface of said wafer a contamination,

a bonding step for direct bonding the surfaces to be bonded of the top and handle wafers, in order to form an intermediate multilayer wafer (30),

a removal step for removing excess material from the top wafer,

the method being characterized in that it comprises between the bonding step and the removal step a cleaning step for removing from the exposed main surfaces of the intermediate multilayer wafer contaminants brought by the treatment step.

2. Method according to the claim 1 characterized in that said treatment step is a surface activation step.

3. Method according to claims 1 or 2 characterized in that said contamination of the wafer surface which is opposed to the activated surface corresponds to a contaminants concentration above 10^{11} atoms/cm^2.

4. Method according to any of the preceding claims characterized in that said treatment is carried out through the exposure of the surface(s) to be treated to a plasma.

5. Method according to any of the preceding claims characterized in that during the treatment step only a surface of the top wafer is treated.

6. Method according to any of the preceding claims characterized in that said cleaning step is carried out immediately after said bonding step.

7. Method according to any of the preceding claims characterized in that said cleaning step is carried out before any high temperature thermal treatment carried out at temperatures higher than 900°C.

8. Method according to any of the preceding claims characterized in that said cleaning step is a wet cleaning.

9. Method according to the preceding claim characterized in that said cleaning step is carried out with a SC2 solution and/or a HF solution.

10. Method according to any of the preceding claims characterized in that said cleaning step is carried out with a mono face cleaning equipment.

11. Method according to any of the preceding claims characterized in that said removal step is carried out by detaching said excess material from the top wafer.

12. Method according to claim 11 characterized in that said detachment is carried out at an embrittlement zone (11) which has been made by introduction of at least one species in the top wafer.

13. Method according to claim 12 characterized in that said introduction of species is carried out through an implantation of species.

14. Method according to claim 13 characterized in that said implantation is a co-implantation of at least two species.

15. Method according to claim 14 characterized in that said implantation is carried out with a global implantation dose of a few 10^{16} atoms/cm^2.

16. Method according to claim 14 or 15 characterized in that said removal step is carried out through a splitting annealing carried out at temperatures remaining under 350°C.

17. Method according to claim 16 characterized in that said temperature for the splitting annealing is in a range between 200°C and 300°C.

18. Method according to any of the preceding claims characterized in that the top wafer is made of Si, or SiGe, SiC, or Ge.

19. Method according to any of the preceding claims characterized in that the handle wafer is made of Si, fused silica, SiC_1 or glass.

20. Method according to any of the preceding claims characterized in that the method further comprises a high temperature thermal treatment of the structure which comprises the handle wafer and the part of the top wafer which has not been removed,

said high temperature thermal treatment being carried out at temperatures higher than 900°C.

21. Method according to claim 12 wherein said detachment being conducted by annealing between 300°C and 500°C.