Title

METHOD OF FORMING SEMICONDUCTOR DEVICE

Background of the Invention

1. Field of the Invention

The present invention relates generally to semiconductor technology, and more particularly to a method of fabricating a semiconductor transistor device with uniform gate dielectric layer, which is capable of improving breakdown voltage (BV) characteristic of the semiconductor transistor device.

2. Description of the Prior Art

Shallow trench isolation (STI) is an integrated circuit feature which prevents electrical current leakage between adjacent semiconductor device components.

FIG. 1 to FIG. 3 schematically depict a conventional method of fabricating a shallow trench isolation.

Referring to FIG. 1, a typical STI process involves growing a pad oxide layer 12 and a nitride layer 14 successively on a substrate 10. A patterned photoresist (not shown) is then applied to define an STI opening pattern on the nitride layer 14. As shown in FIG. 2, the nitride layer 14 and the pad oxide layer 12 underneath are then etched. An STI trench 16 is etched into the substrate 10. After that, the patterned photoresist is stripped off.

In FIG. 3, a sharp diffusion corner 18 is defined by a vertically oriented sidewall of the STI trench 16 and the main surface of substrate 10. The STI trench 16 is then filled with an insulating material 20, such as HDPCVD oxide. Later, the surface of the insulating material 20 may be planarized by a chemical-mechanical polishing (CMP) process using the nitride layer 14 as a polish stop layer. Subsequently, the nitride layer 14 is removed. Next, a wet-etching process is performed to remove the pad oxide layer 12 to complete a STI

24. After the STI 24 is formed, a gate dielectric layer may be formed by thermal oxidation.

However, since the wet-etching process for removing the pad oxide layer 12 is isotropic, a part of the insulating material 20 is also etched away during the wet-etching process. A gap 22 is formed between the insulating layer 20 and the sharp diffusion corner 18. It is difficult to grow a uniform gate dielectric layer at the sharp diffusion corner 18. Typically, the gate dielectric layer is thinner around the sharp diffusion corner 18 than a gate oxide layer grown on the horizontal main surface of the substrate 10. The variation of the thickness of gate dielectric layer results in poor breakdown voltage (BV) characteristic of the semiconductor transistor device, especially high-voltage transistor, and poor gate dielectric layer integrity.

Summary of the Invention

According to a preferred embodiment of the present invention, a method of forming a high voltage device, includes: providing a substrate having at least one isolation element embedded in the substrate, the at least one isolation element including a trench in the substrate and an insulating layer filling the trench, the insulating layer having a top surface and a side surface, wherein a gap is located between the side surface of the insulating layer and the substrate, and a sharp diffusion corner is defined by a vertical sidewall of the trench and a main surface of substrate. Later, a dielectric layer having a first thickness is formed on the substrate, on the top surface of the insulating layer, and in the gap. Then, the dielectric layer is densified. Next, a gate is formed on the dielectric layer. Finally, doping regions are formed at two sides of the gate in the substrate.

According to a preferred embodiment of the present

invention, the dielectric layer having the first thickness is formed by chemical vapor deposition, atomic layer deposition or spin on glass, and densified by an annealing process.

According to another preferred embodiment of the present invention, the aforesaid dielectric layer is a gate dielectric layer of a high voltage device such as a high voltage transistor.

According to another preferred embodiment of the present invention, a method of forming a semiconductor device, the semiconductor device is formed on a substrate having a low voltage device region and a high voltage device region, a plurality of isolation elements embedded in the low voltage device region and the high voltage device region, the steps of forming the semiconductor device comprising: forming a first dielectric layer having a first thickness uniformly on the substrate within the low voltage device region and the high voltage device region. Then, the first dielectric layer is densified. After that, the first dielectric layer within the low voltage device region is removed. Later, the substrate is oxidized thermally to form a second dielectric layer within the low voltage device region and the high voltage device region. Subsequently, a gate line is formed on the first dielectric layer within the high voltage device region. Finally, two doping regions are formed at two sides of the gate line in the substrate.

It is one feature of the present invention that the dielectric layer has an even thickness across the substrate including the sharp diffusion corner of the substrate. Therefore, the gate dielectric integrity is maintained, and the break down voltage can be kept stable.

These and other objectives of the present invention will no

doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

FIG. 1 to FIG. 3 schematically depict a conventional method of fabricating a shallow trench isolation.

FIG. 4 to FIG. 9 schematically depicts a method of forming a semiconductor device according to a preferred embodiment of the present invention.

Detailed Description

FIG. 4 to FIG. 9 schematically depicts a method of forming a semiconductor device according to a preferred embodiment of the present invention. FIG. 7 is a schematic top view of a semiconductor device layout. FIG. 8 is a sectional view of a high voltage device taken along line AA′ in FIG. 7. FIG. 9 is a sectional view of a high voltage device taken along line BB′ in FIG. 7.

As shown in FIG. 4, a substrate 30 having a high voltage device region HV and a low voltage device region LV with at least one isolation element 44 embedded therein respectively are provided. At least one high voltage device such as a high voltage MOS transistor will be formed in the high voltage device region HV later. The isolation element 44 can be an STI 44 formed by the method described in FIG. 1 to FIG. 3. The STI 44 is made of a shallow trench 36 filled with an insulating material 40. The insulating material 40 has a top surface 50 and a side surface 52. The top surface 50 of the insulating material 40 is higher than a main surface 31 of the substrate 30. After STI process, a vertically oriented sidewall of the shallow trench 36 and the main surface 31 of substrate 30 define a sharp diffusion corner 38. A gap 42 is located between the side surface 52 of the insulating material 40 and the substrate 30.

Still refer to FIG. 4, a gate dielectric layer 54 is formed conformally and uniformly on the main surface 31 of the substrate 30 within the high voltage device region HV and the low voltage device region LV, the top surface 50 of the insulating material 40, the sharp diffusion corner 38 and in the gap 42. The gate dielectric layer 54 can be formed by chemical vapor deposition, atomic layer deposition, spin on glass, or other fabricating methods which can form an even dielectric layer on the main surface 31 of the substrate 30, and on the sharp diffusion corner 38. The gate dielectric layer 54 has a uniform thickness, which is a first thickness T_1. Preferably the first thickness T_1 is about 22 nm, but not limited to it. Based on different requirements, the first thickness T_1 can be adjusted. The gate dielectric layer 54 can be silicon oxide, silicon oxynitride, oxide-nitride-oxide, spin-on glass (SOG), low-k materials or other dielectric materials. Moreover, the dielectric layer 54 can be a single material layer or a composite material layer made from the aforesaid materials.

Later, the gate dielectric layer 54 is densifyed by an anneal process or other suitable processes. The gate dielectric layer 54 is preferably silicon oxide. Generally, the density of the gate dielectric layer 54 formed by chemical vapor deposition, atomic layer deposition, or spin on glass is usually lower than that of a gate dielectric layer formed by thermal oxidation. The lower density leads to bad quality of the gate dielectric layer 54, and influences the break down voltage of the transistor. Therefore, the gate dielectric layer 54 needs to be densifyed to make the quality better.

As shown in FIG. 5, after the gate dielectric layer 54 is densifyed, the gate dielectric layer 54 within the low voltage device region LV is removed. For example, by utilizing a patterned mask (not shown) to cover the high voltage device region HV, and expose the low voltage device region LV. Then,

the gate dielectric layer 54 in the low voltage device region LV can be removed. After that, an implanting process can be performed to adjust the threshold voltage in the low voltage device region LV. Later, a cleaning process such as a standard RCA clean is performed to clean the particles on the gate dielectric layer 54 within the high voltage device region HV. The particles may be resulted from implanting dopants into the low voltage device region LV on the substrate 30. During the cleaning process, a thin layer of the dielectric layer 54 may be washed away uniformly by the cleaning solution. As a result, the cleaned dielectric layer 54 on the substrate 30 within the high voltage device region HV including the dielectric layer 54 on the insulating material 40 has a second thickness T_2 which is smaller than the first thickness T_1. According to a preferred embodiment, the second thickness T_2 is about 18 nm, but not limited to it.

As set forth in FIG. 6, a thermal oxidation process is performed to form a low voltage gate dielectric layer 154 for a low voltage device in the low voltage region LV. The low voltage gate dielectric layer 154 could be a tunnel oxide layer for an embedded flash. However, the thermal oxidation process oxidizes the entire substrate 30 uniformly so that the thickness of the gate dielectric layer 54 on the high voltage region HV of substrate 30 becomes thicker since the surface of the substrate 30 is oxidized to become a part of the gate dielectric layer 54. At this point, the gate dielectric layer 54 on the substrate 30 within the high voltage region HV has a third thickness T_3 which is thicker than the second thickness T_2. According to a preferred embodiment, the second thickness is about 20 nm, but not limited to it. The gate dielectric layer 54 on the insulating material 40 within the high voltage region HV remains a second thickness T_2. Therefore, the gate dielectric layer 54 on the substrate 30 and on the insulating material 40 has different thicknesses.

FIG. 7-9 described the steps of fabricating gate lines on the substrate. For the sake of simplicity, the sectional view of the low voltage region LV is omitted. As shown in FIG. 7, a gate line 56 is formed on the gate dielectric layer 54, and the low voltage gate dielectric layer 154, respectively. As shown in FIGs. 7-9, a spacer 58 is formed on the sidewall of the gate line 56 within both the low voltage region LV, and the high voltage region HV. During the formation of the spacer 58, the gate dielectric layer 54, and the low voltage gate dielectric layer 154 besides the gate line 56 is removed simultaneously. After that, doping regions 60 are formed at two opposite sides of the gate line 56 in the substrate 30. Now, a high voltage device 100 of the present invention is completed. Please refer to FIG. 8, since the gate line 56 overlaps the sharp diffusion corner 38 of the substrate 30, based on the conventional method of forming a gate dielectric layer, the gate dielectric layer around the sharp diffusion corner 38 will be very thin or there will be no the gate dielectric layer formed around the sharp diffusion corner 38. By utilizing the method provided in the present invention, the gate dielectric layer 54 is formed by the deposition process which makes the gate dielectric layer 54 have a uniform thickness on the substrate, even on the sharp diffusion corner 38. Therefore, the integrity of the gate dielectric layer 54 remains. Thus, the break down voltage of the high voltage device 100 can be maintained.

Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention.

Claims

1. A method of forming a semiconductor device, comprising:

providing a substrate having at least one isolation element embedded in the substrate, the at least one isolation element including a trench in the substrate and an insulating layer filling the trench, the insulating layer having a top surface and a side surface, wherein a gap is located between the side surface of the insulating layer and the substrate;

forming a dielectric layer having a first thickness on the substrate, on the top surface of the insulating layer, and in the gap;

densifying the dielectric layer;

cleaning a surface of the dielectric layer, causing the dielectric layer to have a second thickness, in which the first thickness is greater than the second thickness;

thermally oxidizing the entire substrate uniformly, causing the dielectric layer on the substrate and in the gap to thicken to cause the dielectric layer to have a third thickness;

maintaining the dielectric layer on the top surface of the insulating layer at the second thickness;

forming a gate line on the dielectric layer on the substrate; and

forming doping regions in the substrate on opposing sides of the gate line.

2. The method of forming a semiconductor device of claim 1, wherein the dielectric layer is selected from the group consisting of silicon oxide, silicon oxynitride, oxide-nitride-oxide, spin-on glass and low-k materials.

3. The method of forming a semiconductor device of claim 1, wherein the dielectric layer is formed by the process selected from the group consisting of chemical vapor deposition, atomic layer deposition and spin on glass.

4. The method of forming a semiconductor device of claim 1, wherein the third thickness is greater than the second thickness.

5. The method of forming a semiconductor device of claim 1, wherein the dielectric layer is a composite material layer.

6. The method of forming a semiconductor device of claim 5, wherein the composite material layer are selected from the group consisting of silicon oxide, silicon oxynitride, oxide-nitride-oxide, spin-on glass and low-k materials.

7. The method of forming a semiconductor device of claim 1, wherein the step of densifying the dielectric layer comprises an anneal process.

8. The method of forming a semiconductor device of claim 1, wherein a sharp diffusion corner is defined by a vertical sidewall of the trench and a main surface of substrate.

9. The method of forming a semiconductor device of claim 8, wherein the step of forming the dielectric layer comprises forming the dielectric layer on the sharp diffusion corner.

10. A method of forming a semiconductor device, the semiconductor device is formed on a substrate having a low voltage device region and a high voltage device region, a plurality of isolation elements embedded in the low voltage device region and the high voltage device region, the steps of forming the semiconductor device comprising:

forming a first dielectric layer having a first thickness uniformly on the substrate within the low voltage device region and the high voltage device region;

densifying the first dielectric layer;

removing the first dielectric layer within the low voltage device region;

cleaning the first dielectric layer within the high voltage device region to cause the first dielectric layer within the high voltage device region to have a second thickness;

thermally oxidizing the entire substrate uniformly to form a second dielectric layer on the substrate within the low voltage device region and to cause the first dielectric layer on the substrate within the high voltage device region to thicken to a third thickness;

maintaining the first dielectric layer on the isolation elements in the high voltage device region at the second thickness;

forming a gate line on the first dielectric layer with the increased thickness within the high voltage device region; and

forming doping regions in the substrate on opposing sides of the gate line.

11. The method of forming a semiconductor device of claim 10, wherein the second dielectric layer serves as a gate dielectric layer for a low voltage device.

12. The method of forming a semiconductor device of claim 10, wherein the first dielectric layer comprises silicon oxide, silicon oxynitride, oxide-nitride-oxide, spin-on glass or low-k materials.

13. The method of forming a semiconductor device of claim 10, wherein the first dielectric layer is a composite material layer.