WHAT IS CLAIMED IS:

1. A calibration circuit, comprising:

a differential input circuit, configured to receive a first oscillation signal and a second oscillation signal, the first oscillation signal and the second oscillation signal having a same frequency and opposite phases, a duty cycle of the first oscillation signal and a duty cycle of the second oscillation signal being in a first preset range, and the differential input circuit configured to output a first internal signal and a second internal signal;

a comparison unit, connected to an output end of the differential input circuit, and configured to compare the duty cycle of the first internal signal and/or the duty cycle of the second internal signal; and

a logical unit, connected to the comparison unit and the differential input circuit, and configured to control the differential input circuit according to an output result of the comparison unit, such that the duty cycle of the first internal signal and/or the duty cycle of the second internal signal reaches a second preset range;

wherein the comparison unit comprises:

an integral unit with a first input end and a second input end, the first input end configured to receive one of the first internal signal or the second internal signal, and the second input end configured to receive another of the second internal signal or the first internal signal; and

a comparator, connected to an output end of the integral unit;

wherein the first input end of the integral unit is configured to receive the first internal signal when a flipping identification signal is at a low level, and receive the second internal signal when the flipping identification signal is at a high level; and

the second input end of the integral unit is configured to receive the second internal signal when the flipping identification signal is at a low level, and receive the first internal signal when the flipping identification signal is at a high level.

2. The calibration circuit of claim 1, wherein the logical unit comprises:

a counter, configured to adjust the duty cycle of the first internal signal and/or the duty cycle of the second internal signal;

a first register group, configured to store a first value of the counter according to output of the comparator when the flipping identification signal is at a low level; and

a second register group, configured to store a second value of the counter according to output of the comparator when the flipping identification signal is at a high level.

3. The calibration circuit of claim 2, wherein the logical unit further comprises:

an operation component, connected to the first register group and the second register group, and configured to perform addition, subtraction, multiplication and division on output of the first register group and the second register group; and

a third register group, connected to the operation component, and configured to store an output result of the operation component.

4. The calibration circuit of claim 3, wherein the comparison unit is driven by a sampling clock, and a frequency of the sampling clock is lower than a frequency of the first internal signal and/or a frequency of the second internal signal.

5. The calibration circuit of claim 4, wherein the counter is driven by a calculator clock, and a frequency of the calculator clock is lower than the frequency of the first internal signal and/or the frequency of the second internal signal.

6. The calibration circuit of claim 5, wherein the frequency of the sampling clock is same as the frequency of the calculator clock.

7. The calibration circuit of claim 6, further comprising:

a frequency divider, configured to receive an external clock signal, and generate the sampling clock and the calculator clock.

8. The calibration circuit of claim 7, further comprising:

a fifth register group, connected with the frequency divider, and adapted to configure the frequency of the sampling clock and the frequency of the calculator clock.

9. The calibration circuit of claim 1, wherein the differential input circuit is further configured to receive a first external signal and a second external signal, and the first external signal and the second external signal have a same frequency and opposite phases.

10. The calibration circuit of claim 9, further comprising:

a selector, wherein the first oscillation signal, the second oscillation signal, the first external signal and the second external signal are connected to the differential input circuit through the selector, and by taking the first oscillation signal and the second oscillation signal as a first differential pair signal and taking the first external signal and the second external signal as a second differential pair signal, the selector is configured to select one of the first differential pair signal and the second differential pair signal to input into the differential input circuit.

11. The calibration circuit of claim 10, wherein a control end of the selector is configured to receive a calibration enable signal, when the calibration enable signal is at a low level, the first external signal and the second external signal are input into the differential input circuit, and when the calibration enable signal is at a high level, the

first oscillation signal and the second oscillation signal are input into the differential input circuit.

12. A memory, comprising:

the calibration circuit of any one of claims 1-11.

13. A calibration method, comprising:

receiving, with a differential input circuit, a first oscillation signal and a second oscillation signal, the first oscillation signal and the second oscillation signal having the same frequency and opposite phases, the duty cycle of the first oscillation signal and the duty cycle of the second oscillation signal being in a first preset range, and the differential input circuit outputting a first internal signal and a second internal signal;

receiving, with a comparison unit, the first internal signal and the second internal signal, and comparing the duty cycle of the first internal signal or the duty cycle of the second internal signal; and

controlling, with a logical unit, the differential input circuit according to an output result of the comparison unit, such that the duty cycle of the first internal signal and/or the duty cycle of the second internal signal reaches a second preset range;

wherein the receiving, with the comparison unit, the first internal signal and the second internal signal comprises:

when a flipping identification signal is at a low level, the comparison unit comparing the duty cycle of the first internal signal; and

when the flipping identification signal is at a high level, the comparison unit comparing the duty cycle of the second internal signal.

14. The calibration method of claim 13, wherein the controlling, with the logical unit, the differential input circuit according to the output result of the comparison unit comprises:

the logical unit comprising a counter, a first register group and a second register group;

when the flipping identification signal is at a low level, the counter counting from U to V, when the value of the counter is U, the duty cycle corresponding to the first internal signal being X%, when the value of the counter is V, the duty cycle corresponding to the first internal signal being Y%, and when the output result of the comparison unit is changed from the low level to the high level, the counter value corresponding to the counter at this time being stored in the first register group;

when the flipping identification signal is at a high level, the counter counting from U to V, when the value of the counter is U, the duty cycle corresponding to the second internal signal being Y%, when the value of the counter is V, the duty cycle corresponding to the second oscillation signal being X%, when the output result of the comparison unit is changed from the high level to the low level, the counter value corresponding to the counter at this time being stored in the second register group;

wherein both the U and V are integers, the U is less than V, both the X and Y are positive integers, the X is less than 50, and the Y is greater than 50.

15. The calibration method of claim 14, wherein the controlling, with the logical unit, the differential input circuit according to the output result of the comparison unit further comprises:

the logical unit further comprising an operation component and a third register group;

the operation component performing addition, subtraction, multiplication and division on output of the first register group and the second register group, and storing the obtained numerical value H in the third register group;

wherein the H is an integer, and the H is greater than or equal to the U and less than or equal to the V.

16. The calibration method of claim 15, wherein the duty cycle of the first internal signal corresponding to the H is in the second preset range.