

Description

Field of the Invention

This invention relates in general to transconductance amplifier circuits and, more particularly, to a complementary metal oxide semiconductor (CMOS) voltage to current converter circuit providing a reference current, the magnitude of the reference current varying linearly with an input voltage that may vary to the supply voltage rails, having a single ended input stable over a wide bandwidth without requiring compensation, offset correction, external feedback, or capacitive coupling of the input voltages.

Background of the Invention

Operational amplifiers have been widely used in the electronics industry for their many excellent circuit characteristics including high open loop gain, high input impedance, and low output impedance. General applications of the operational amplifier include circuit configurations such as voltage and current amplifiers, differentiators and integrators, comparators, active filters, oscillators, and analog to digital and digital to analog converters. Operational amplifiers may be further used to convert a voltage to a current (transconductance amplifiers) by inputting a voltage to be converted into the noninverting input of the operational amplifier, and having the output drive a Darlington transistor pair which supplies the desired output current. One drawback of the operational amplifier is a necessary trade-off between speed and accuracy. Higher speed is obtained by reducing the DC precision; likewise, a low DC error is achieved at the expense of a reduced bandwidth. Further, the operational amplifier requires differential inputs, compensation, offset correction, external feedback, and a significant amount of silicon area in its implementation. A more recent circuit development, the operational transconductance amplifier (OTA), has emerged which improves upon some of the operational amplifier characteristics. The OTA, like the operational amplifier, can be used in a wide variety of circuit and system applications. The OTA, however, offers higher performance and its performance is independent of load conditions. A major advantage of the OTA lies in the ability to couple the outputs of several OTAs together in order to sum, subtract, or multiply the voltages at the inputs of the individual OTAs. Because the outputs of the OTAs are currents, coupling additional outputs do not degrade performance. Also, because inputs are isolated, increasing the number of inputs does not degrade performance. Like the operational amplifier, however, OTAs require differential inputs and external feedback, a significant amount of silicon area, and are not able to operate linearly with an input voltage which goes all the way to the V_{SS} or V_{DD} sup-

ply rail. It is desirable to negate the need for external feedback and reduce the number of terminals required by using a single ended input versus the differential inputs required by the operational amplifier and the OTA.

Thus, what is needed is a voltage to current converter providing a reference current, the magnitude of the reference current varying linearly with an input voltage that may vary to the supply voltage rails, having a single ended input stable over a wide bandwidth without requiring compensation, offset correction, external feedback, or capacitive coupling of the input voltages.

Accordingly, an object of the present invention is to provide an improved voltage to current converter.

Another object of the present invention is to provide an improved voltage to current converter providing linear operation for an input voltage that may vary to the supply voltage rails.

A further object of the present invention is to provide a voltage to current converter with closed loop gain and a single ended input.

Yet a further object of the present invention is to provide a voltage to current converter with improved bandwidth and DC precision without requiring external feedback, compensation, or offset correction.

In carrying out the above and other objects of the invention in one form, there is provided a complementary metal oxide semiconductor (CMOS) voltage to current converter circuit comprising :

a first supply voltage terminal coupled for receiving a first supply voltage;

a second supply voltage terminal coupled for receiving a second supply voltage, the first supply voltage being greater than the second supply voltage;

an input terminal coupled for receiving a conversion voltage;

an output current sink terminal;

an output current source terminal;

voltage divider means coupled between said second supply voltage terminal and said input terminal, wherein said conversion voltage provides power for the CMOS circuit and may vary over a range extending from two threshold voltages above said second supply voltage to a transistor gate-source junction potential above said first supply voltage, said voltage divider means having a voltage reference node for providing a reference voltage relative to said conversion voltage applied at said input terminal;

voltage to current converter means coupled to said first and second supply voltage terminals and said input terminal, and coupled to said voltage reference node for providing a linear reference current whose magnitude varies linearly in response to a corresponding change in said conversion voltage; and

output means coupled between said second supply voltage terminal and said input terminal and coupled to said voltage to current converter means

for providing an output sink current and an output source current at said output current sink terminal and said output current source terminal, respectively, wherein the magnitude of said output sink and the magnitude of said output source current are a ratio of the magnitude of said linear reference current.

The above and other objects, features, and advantages of the present invention will be better understood from the following detailed description taken in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a schematic of a first embodiment of the present invention.

FIG. 2 is a schematic of a second embodiment of the present invention.

FIG. 3 is a partial block diagram of an adder circuit comprising the first embodiment.

Detailed Description of the Invention

Figure 1 illustrates a voltage to current converter circuit 10 that is manufacturable using a standard CMOS process. A field effect transistor 4 has a source connected to an input terminal 3, a gate connected to an enable terminal 5, and a drain coupled to a voltage reference node 8 by a resistor 6, and the voltage reference node 8 is coupled to a supply voltage terminal 2 operating at ground potential by a resistor 7. The field effect transistor 4 and the resistor 6 and 7 comprise a voltage divider for providing a reference voltage (V_{REF}) at the voltage reference node 8 with its magnitude determined by a conversion voltage (V_{CONV}) at the input terminal 3 and the ratio of the resistances of the resistors 6 and 7.

It is typical for the value of a resistor to vary by as much as 20 percent in a CMOS process due to process and temperature variations. A change in the value of the resistor 6 (R_6) can be offset by a corresponding change in the value of the resistor 7 (R_7) and vice versa if the two resistors 6 and 7 are placed in close proximity to one another. A stable reference voltage then, can be developed at the voltage reference node 8 by the use of monolithically integrated resistors. The reference voltage in this arrangement is determined by the relationship:

$$V_{REF} = V_{CONV}(R_7/(R_7 + R_6)).$$

Other methods to provide the reference voltage could include using ratioed field effect transistors or by the use of switched capacitor circuits. The voltage to current converter circuit can be put into a low power stand-by mode by applying a logical 1 signal at the enable terminal 5, whereby field effect transistor 4 will be in its nonconducting state and no current will flow through the resistors 6 and 7 and thus the reference voltage will equal 0.0 volts.

The linear reference current generator circuitry is

comprised of a cascode current mirror 11, a current mirror 12, and devices 13, 14, 15, and 16. The cascode current mirror 11 comprises field effect transistors 22, 23, 24, and 25, and the current mirror 12 comprises field effect transistors 19 and 21. In the cascode current mirror 11, field effect transistor 23 forms a diode having a source connected to the input terminal 3, and a gate and a drain connected to a current reference node 18. The field effect transistor 22 having a source connected to the input terminal 3, a gate connected to the current reference node 18, and a drain connected to the drain of a field effect transistor 24, mirrors a linear reference current that is produced in the field effect transistor 23. The field effect transistor 24 forms a diode having a gate connected to a drain, and a source connected to the voltage reference node 8. The field effect transistor 25 having a drain connected to the current reference node 18, a gate connected to the gate of the field effect transistor 24, and a source connected to a gain terminal 17, mirrors the mirrored linear reference current flowing in the field effect transistor 24.

In current mirror 12, the field effect transistor 21 forms a diode having a source connected to the supply voltage terminal 2, and a gate and a drain connected to a gate of a field effect transistor 19. The field effect transistor 19 having a source connected to the supply voltage terminal 2, and a drain connected to the voltage reference node 8, mirrors a feedback current flowing in the field effect transistor 21. A gain resistor 14 (R_{14}) is coupled between the gain terminal 17 and the supply voltage terminal 2 and sets the magnitude of the linear reference current flowing in the cascode current mirror 11. The gain resistor 14 could be implemented as a monolithically integrated resistor on chip, or as a field effect transistor operated in its linear region. Alternatively, an external resistor (not monolithically integrated) could be used as the gain resistor 14 (providing excellent accuracy therewith).

The field effect transistor 15 has a source connected to the input voltage terminal 3, a gate connected to the current reference node 18, and a drain connected to the source of a field effect transistor 16. The field effect transistor 16 has a gate connected to the gain terminal 17, and a drain connected to the drain of the field effect transistor 21. The field effect transistor 13 has a source connected to a supply voltage terminal 1 operating at a positive potential, such as V_{DD} , and a gate and a drain connected to the source of the field effect transistor 24 for providing a start-up current to the cascode current mirror 11 when power is initially applied to the supply voltage terminals 1 and 2, and input terminal 3.

An output stage comprises a current mirror 36, wherein a field effect transistor 28 forms a diode having a source connected to the supply voltage terminal 2, and a gate and a drain connected to the drain of a

field effect transistor 27. A field effect transistor 29 has a source connected to the supply voltage terminal 2, a gate connected to the gate of the field effect transistor 28, and a drain connected to the source of a field effect transistor 31 for mirroring a reference sink current flowing in the field effect transistor 28. A field effect transistor 26 having a source connected to the input terminal 3, a gate connected to the current reference node 18, and a drain connected to a gate and a drain of the field effect transistor 27, sources the reference sink current to the current mirror 36. The field effect transistor 27 increases the impedance between the field effect transistor 26 and the supply voltage terminal 2.

A field effect transistor 32 has a source connected to the input terminal 3, a gate connected to the current reference node 18, and a drain connected to the source of a field effect transistor 33 for providing a reference source current. The field effect transistor 31 has a gate and a drain connected to an output current sink terminal 34, and the field effect transistor 33 has a gate and drain connected to an output current source terminal 35. The purpose of the field effect transistors 31 and 33 is for increasing the output impedances at the output current sink and output current source terminals 34 and 35, respectively, therein providing the capability to couple the outputs of several voltage to current converter circuits together without degrading performance substantially.

The reference voltage, as noted earlier, is determined by the ratio of the resistances of the resistors 6 and 7. A typical value of the reference voltage could be set at 1/4 the value of the conversion voltage. To accomplish this would require the resistance of R_6 to be three times the resistance of R_7 . In order to ensure the parallel impedance of the field effect transistors 19 and 24 do not substantially affect the reference voltage, the values of the resistors 6 and 7 should be chosen such that their parallel resistance is approximately 1/10 of the parallel impedance of the field effect transistors 19 and 24.

By the action of the cascode current mirror 11, the reference voltage will be precisely tracked by a gain voltage at the gain terminal 17. A change in the conversion voltage causes a proportional change in the reference voltage which is accurately tracked at the gain terminal 17. The change in the gain voltage is accomplished by a linear change in the linear reference current through the cascode current mirror 11 since this current change is determined by the reference voltage. By way of example only, a transconductance of 1 microamp/1 volt can be obtained by satisfying the following relationships:

$$\text{set } R_6 = 3R_7, \text{ as a result } V_{REF} = V_{CONV}/4$$

$$I_{R14} = V_{CONV}/(4R_{14})$$

$$R_{14} = V_{CONV}/(4I_{R14}) = 1 \text{ volt}/4 \text{ microamps}$$

$$R_{14} = 250,000 \text{ ohms.}$$

As a result, a change in the conversion voltage of 1

volt corresponds to a change in the linear reference current of 1 microamp. A different transconductance may be produced by varying the relationship of R_6 to R_7 and by varying the value of R_{14} .

The linear reference current flowing in the gain resistor 14 is reflected to the field effect transistor 15 by the current reference node 18. An undesired fluctuation in the linear reference current is mirrored back to the cascode current mirror 11 by the action of the current mirror 12. This fluctuation in the linear reference current flows through transistor 19 instead of being dissipated in the voltage divider network which would cause an unwanted change in the reference voltage. The closed loop operation of the linear reference current generator circuit keeps the reference voltage very precise. Typically the conversion voltage would be applied to the gates of several field effect transistors, but by using the sources of transistors 15, 22, 23, 26, and 32 as the controlling nodes, it is possible to increase the usable operating range of the conversion voltage. Operation of the CMOS voltage to current converter circuit 10 will extend from the sum of a N-channel and a P-channel field effect transistor threshold voltage to a gate-source voltage (V_{GS}) above the V_{DD} supply voltage at the supply voltage terminal 1.

The linear reference current is reflected to the output stage's field effect transistors 26 and 32 by current reference node 18. The reference sink current flowing in the field effect transistor 26 will be mirrored in the field effect transistor 29 by the current mirror 36 when a load is connected to the output current sink terminal 34. The output current sink terminal 34 then, will sink an output sink current equal to the linear reference current or some ratio thereof. Likewise, when a load is connected to the output current source terminal 35, an output source current equal to the linear reference current or some ratio thereof will be sourced to the load.

The first and second embodiments of the present invention are comprised of similar devices, but the second embodiment operates with the supply voltage terminals, 1 and 2, and input terminal 3 connected in a different manner as illustrated in FIG. 2. The difference in the second embodiment includes the sources of field effect transistors 4, 15, 22, 23, 26, and 32 being connected to the supply voltage terminal 1, the sources of field effect transistors 19, 21, 28, and 29 being connected to the input terminal 3, and the resistor 7 is coupled between the voltage reference node 8 and the input terminal 3. Also, the resistor 6 is coupled between the supply voltage terminal 1 and the voltage reference node 8.

The reference voltage in the second embodiment will be determined by the ratios of resistances of the resistors 6 and 7, and by the magnitude of the conversion voltage with respect to the V_{DD} supply voltage and is calculated by:

$$V_{REF} = (V_{DD} - V_{CONV})R_7/(R_7 + R_6).$$

In this configuration, the CMOS voltage to current converter circuit 20 provides a linear reference current for a conversion voltage that may vary from the V_{SS} supply voltage less a V_{as} to the V_{DD} supply voltage less the sum of a N-channel and a P-channel threshold voltage.

An example of an adder implementation using the CMOS voltage to current converter circuit 10 is shown in FIG. 3. In this example, two voltage to current converter circuits 10 and 10', are used to add two conversion voltages, V_{CONV1} and V_{CONV2} , applied at the input terminals 3 and 3' respectively. Each CMOS voltage to current converter circuit 10 and 10' may have a different gain as set by the gain resistors 14 and 14' respectively. An output current source terminal 35 and 35' of each CMOS voltage to current converter circuit 10 and 10' is coupled to the supply voltage terminal 2 by a load resistor 37. An output source current, I_1 , flowing from the output current source terminal 35 is added to an output source current, I_2 , flowing from the output current source terminal 35', and the sum of these currents, I_3 , flows through the load resistor 37.

The conversion voltages, V_{CONV1} and V_{CONV2} may vary from the sum of an N-channel and a P-channel threshold voltage above the V_{SS} supply voltage to a V_{as} above the V_{DD} supply voltage. The voltage to current converter circuits 10 and 10' in FIG 3 may be replaced by voltage to current converter circuits 20 and 20' to provide operation wherein the conversion voltages V_{CONV1} and V_{CONV2} may vary from the sum of an N-channel and a P-channel threshold voltage below the V_{DD} supply voltage to a V_{as} below the V_{SS} supply voltage. A subtractor circuit can be implemented by replacing the output current source terminal 35 connection of the voltage to current convert circuit 10 in figure 3 with a connection to the output current sink terminal 34. As a result, I_1 will be subtracted from I_2 .

In this adder example, unlike the operational amplifier or OTA, it is possible to add signals that have different DC voltage levels without having to capacitively couple these signals to the input since each input is independent. Capacitively coupling the inputs is undesirable because the capacitors form an unwanted low pass filter and thus block the low frequency components of an input signal. Adding more than two signals could be accomplished by using more CMOS voltage to current converter circuits and coupling the output current source terminals together. Also the adder circuit example does not require external feedback or compensation. And because the inputs are single ended, offset correction is not a requirement. The CMOS voltage to current converter circuit has been illustrated as an adder circuit, as an example, but may also be used to perform many other functions including multiplication, subtraction, etc.

By now it should be appreciated that there has

been provided a CMOS voltage to current converter circuit which provides a linear reference current accurate to the supply voltage rails, having a single ended input stable over a wide bandwidth without the need for compensation, offset correction, external feedback, or capacitive coupling.

Claims

1. A complementary metal oxide semiconductor - (CMOS) voltage to current converter circuit comprising:
 - a first supply voltage terminal (1) coupled for receiving a first supply voltage;
 - a second supply voltage terminal (2) coupled for receiving a second supply voltage, the first supply voltage being greater than the second supply voltage;
 - an input terminal (3) coupled for receiving a conversion voltage;
 - an output current sink terminal (35);
 - an output current source terminal (34);
 - voltage divider means (4, 6, 7) coupled between said second supply voltage terminal and said input terminal, wherein said conversion voltage provides power for the CMOS circuit and may vary over a range extending from two threshold voltages above said second supply voltage to a transistor gate-source junction potential above said first supply voltage, said voltage divider means having a voltage reference node (8) for providing a reference voltage relative to said conversion voltage applied at said input terminal;
 - voltage to current converter means (11, 12, 14, 15, 16) coupled to said first and second supply voltage terminals and said input terminal, and coupled to said voltage reference node for providing a linear reference current whose magnitude varies linearly in response to a corresponding change in said conversion voltage; and
 - output means (26-29, 31-33) powered between said second supply voltage terminal and said input terminal and coupled to said voltage to current converter means for providing an output sink current and an output source current at said output current sink terminal and said output current source terminal, respectively, wherein the magnitude of said output sink current and the magnitude of said output source current are a ratio of the magnitude of said linear reference current.
2. The CMOS circuit of claim 1 wherein said voltage to current converter means comprises:
 - a gain terminal (17);
 - a gain resistor (14) coupled between said gain terminal and said second supply voltage terminal.



$$V_{REF} = (V_{DD} - V_{CONV})R_7/(R_7 + R_8).$$

In this configuration, the CMOS voltage to current converter circuit 20 provides a linear reference current for a conversion voltage that may vary from the V_{SS} supply voltage less a V_{as} to the V_{DD} supply voltage less the sum of a N-channel and a P-channel threshold voltage.

An example of an adder implementation using the CMOS voltage to current converter circuit 10 is shown in FIG. 3. In this example, two voltage to current converter circuits 10 and 10', are used to add two conversion voltages, V_{CONV1} and V_{CONV2} , applied at the input terminals 3 and 3' respectively. Each CMOS voltage to current converter circuit 10 and 10' may have a different gain as set by the gain resistors 14 and 14' respectively. An output current source terminal 35 and 35' of each CMOS voltage to current converter circuit 10 and 10' is coupled to the supply voltage terminal 2 by a load resistor 37. An output source current, I_1 , flowing from the output current source terminal 35 is added to an output source current, I_2 , flowing from the output current source terminal 35', and the sum of these currents, I_3 , flows through the load resistor 37.

The conversion voltages, V_{CONV1} and V_{CONV2} may vary from the sum of an N-channel and a P-channel threshold voltage above the V_{SS} supply voltage to a V_{as} above the V_{DD} supply voltage. The voltage to current converter circuits 10 and 10' in FIG 3 may be replaced by voltage to current converter circuits 20 and 20' to provide operation wherein the conversion voltages V_{CONV1} and V_{CONV2} may vary from the sum of an N-channel and a P-channel threshold voltage below the V_{DD} supply voltage to a V_{as} below the V_{SS} supply voltage. A subtractor circuit can be implemented by replacing the output current source terminal 35 connection of the voltage to current convert circuit 10 in figure 3 with a connection to the output current sink terminal 34. As a result, I_1 will be subtracted from I_2 .

In this adder example, unlike the operational amplifier or OTA, it is possible to add signals that have different DC voltage levels without having to capacitively couple these signals to the input since each input is independent. Capacitively coupling the inputs is undesirable because the capacitors form an unwanted low pass filter and thus block the low frequency components of an input signal. Adding more than two signals could be accomplished by using more CMOS voltage to current converter circuits and coupling the output current source terminals together. Also the adder circuit example does not require external feedback or compensation. And because the inputs are single ended, offset correction is not a requirement. The CMOS voltage to current converter circuit has been illustrated as an adder circuit, as an example, but may also be used to perform many other functions including multiplication, subtraction, etc.

By now it should be appreciated that there has

been provided a CMOS voltage to current converter circuit which provides a linear reference current accurate to the supply voltage rails, having a single ended input stable over a wide bandwidth without the need for compensation, offset correction, external feedback, or capacitive coupling.

Claims

1. A complementary metal oxide semiconductor - (CMOS) voltage to current converter circuit comprising:

a first supply voltage terminal (1) coupled for receiving a first supply voltage;

a second supply voltage terminal (2) coupled for receiving a second supply voltage, the first supply voltage being greater than the second supply voltage;

an input terminal (3) coupled for receiving a conversion voltage;

an output current sink terminal (35);

an output current source terminal (34);

voltage divider means (4, 6, 7) coupled between said second supply voltage terminal and said input terminal, wherein said conversion voltage provides power for the CMOS circuit and may vary over a range extending from two threshold voltages above said second supply voltage to a transistor gate-source junction potential above said first supply voltage, said voltage divider means having a voltage reference node (8) for providing a reference voltage relative to said conversion voltage applied at said input terminal;

voltage to current converter means (11, 12, 14, 15, 16) coupled to said first and second supply voltage terminals and said input terminal, and coupled to said voltage reference node for providing a linear reference current whose magnitude varies linearly in response to a corresponding change in said conversion voltage; and

output means (26-29, 31-33) powered between said second supply voltage terminal and said input terminal and coupled to said voltage to current converter means for providing an output sink current and an output source current at said output current sink terminal and said output current source terminal, respectively, wherein the magnitude of said output sink current and the magnitude of said output source current are a ratio of the magnitude of said linear reference current.

2. The CMOS circuit of claim 1 wherein said voltage to current converter means comprises:

a gain terminal (17);

a gain resistor (14) coupled between said gain terminal and said second supply voltage terminal.



terminal;

a first current mirror means (11) coupled between said input terminal and said gain terminal and coupled to said voltage reference node (8) for generating said linear reference current wherein the value of said gain resistor (14) in conjunction with the magnitude of said conversion voltage determine the magnitude of said linear reference current flowing in said first current mirror means (11);

a second current mirror means (12) coupled to said second supply voltage terminal and said voltage reference node (8) for providing a feedback current to said first current mirror means (11);

a first field effect transistor (13) having a source coupled to said first supply voltage terminal and a gate and a drain coupled to said first current mirror means (11);

a second field effect transistor (15) having a gate coupled to said first current mirror means, a source coupled to said input terminal, and having a drain; and

a third field effect transistor (16) having a source coupled to said drain of said second field effect transistor, a gate coupled to said gain terminal, and a drain coupled to said second current mirror means.

3. The CMOS circuit of claim 2 wherein said output means (26-29, 31-33) comprises:

a third current mirror means (36) coupled between said second supply voltage terminal and said output current sink terminal (34) for sinking a current from said output current sink terminal;

a fourth field effect transistor (26) having a source coupled to said input terminal, a gate coupled to said voltage to current converter means, and having a drain;

a fifth field effect transistor (27) having a source and a gate coupled to said drain of said fourth field effect transistor (26) and a drain coupled to said third current mirror means; and

a sixth field effect transistor (32) having a source coupled to said input terminal, a gate coupled to said gate of said fourth field effect transistor (26), and a drain coupled to said output current source terminal (35).

4. A complementary metal oxide semiconductor - (CMOS) voltage to current converter circuit, comprising:

a first supply voltage terminal (1);
a second supply voltage terminal (2);
an input terminal (3);
an output current sink terminal (35);
an output current source terminal (34);
a gain terminal (17);

a first resistor (6) coupled between said input terminal and a voltage reference node (8);

a second resistor (7) coupled between said voltage reference node (8) and said second supply voltage terminal;

a first field effect transistor (13) having a source coupled to said first supply voltage terminal, and having a gate and a drain;

a second field effect transistor (15) having a source coupled to said input terminal, a gate coupled to a current reference node (18), and having a drain;

a third field effect transistor (16) having a source coupled to said drain of said second field effect transistor, a gate coupled to said gain terminal, and having a drain;

a fourth field effect transistor (26) having a source coupled to said input terminal, a gate coupled to said current reference node, and having a drain;

a fifth field effect transistor (27) having a source and a gate coupled to said drain of said fourth field effect transistor, and having a drain;

a sixth field effect transistor (32) having a source coupled to said input terminal, a gate coupled to said current reference node (18), and a drain coupled to said output current source terminal (35);

a seventh field effect transistor (22) having a source coupled to said input terminal, a gate coupled to said current reference node (18), and a drain coupled to said gate and said drain of said first field effect transistor;

an eighth field effect transistor (23) having a source coupled to said input terminal, and a gate and a drain coupled to said current reference node (18);

a ninth field effect transistor (24) having a source and a gate coupled to said drain of said seventh field effect transistor, and a drain coupled to said voltage reference node (8);

a tenth field effect transistor (25) having a drain coupled to said current reference node (18), a gate coupled to said gate of said ninth field effect transistor (24), and a source coupled to said gain terminal (17);

a gain resistor (14) coupled between said gain terminal (17) and said second supply voltage terminal;

an eleventh field effect transistor (21) having a gate and a drain coupled to said drain of said third field effect transistor (16), and a source coupled to said second supply voltage terminal;

a twelfth field effect transistor (19) having a drain coupled to said voltage reference node (8), a gate coupled to said gate of said eleventh field effect transistor (21), and a source coupled to said second supply voltage terminal;



a thirteenth field effect transistor (28) having a gate and a drain coupled to said drain of said fifth field effect transistor (27), and a source coupled to said second supply voltage terminal; and a fourteenth field effect transistor (29) having a drain coupled to said output current sink terminal (34), a gate coupled to said gate of said thirteenth field effect transistor (28), and a source coupled to said second supply voltage terminal.

Patentansprüche

1. Komplementär-Metalloxid-Halbleiter (CMOS)-Spannungs-Stromumsetz-Schaltung, die umfaßt:

einen ersten Speisespannungsanschluß (1), der zur Aufnahme einer ersten Speisespannung geschaltet ist;

einen zweiten Speisespannungsanschluß (2), der zur Aufnahme einer zweiten Speisespannung geschaltet ist, wobei die erste Speisespannung höher ist als die zweite Speisespannung;

einen Eingangsanschluß, der zur Aufnahme einer Umsetzspannung geschaltet ist;

einen Ausgangsstromsenkanschluß (35);

einen Ausgangsstromquellenanschluß (34);

Spannungsteilereinrichtung (4, 6, 7), die zwischen den zweiten Speisespannungsanschluß und den Eingangsanschluß geschaltet ist, wobei die Umsetzspannung die Energie für die CMOS-Schaltung liefert und innerhalb eines Bereichs schwanken kann, der von zwei Schwellenspannungen, die über der zweiten Speisespannung liegen, bis zum Potential einer Gate-Source-Verbindung eines Transistors reicht, das über der ersten Speisespannung liegt, wobei die Spannungsteilereinrichtung einen Spannungsreferenzknoten (8) hat, der eine Referenzspannung in Bezug auf die an den Eingangsanschluß angelegte Umsetzspannung liefert;

Spannungs-Stromumsetz-Einrichtung (11, 12, 14, 15, 16), die an den ersten und den zweiten Speisespannungsanschluß und den Eingangsanschluß geschaltet ist, und zur Lieferung eines linearen Referenzstroms" dessen Größe sich in Reaktion auf eine entsprechende Änderung der Umsetzspannung linear ändert, an den Spannungsreferenzknoten geschaltet ist; und

Ausgangseinrichtung (26-29, 31-33), die zwischen dem zweiten Speisespannungsanschluß und dem Eingangsanschluß gespeist wird, an die Spannungs-Stromumsetz-Einrichtung geschaltet ist, und am Ausgangsstromsenkanschluß und am

Ausgangsstromquellenanschluß einen Ausgangssenkstrom bzw. einen Ausgangsquellenstrom liefert, wobei die Größe des Ausgangssenkstroms und die Größe des Ausgangsquellenstroms ein Teil der Größe des linearen Referenzstroms sind.

2. CMOS-Schaltung nach Anspruch 1, wobei die Spannung-Stromumsetz-Einrichtung umfaßt:
einen Verstärkungsanschluß (17);
einen Verstärkungswiderstand (14), der zwischen den Verstärkungsanschluß und den zweiten Speisespannungsanschluß geschaltet ist;

eine erste Strom-Spiegeleinrichtung (11), die zwischen den Eingangsanschluß und den Verstärkungsanschluß geschaltet ist, an den Spannungsreferenzknoten (8) geschaltet ist, und einen linearen Referenzstrom erzeugt, wobei der Widerstandswert des Verstärkungswiderstandes (14) zusammen mit der Größe der Umsetzspannung die Größe des linearen Referenzstroms bestimmt, der in der ersten Strom-Spiegeleinrichtung (11) fließt;

eine zweite Strom-Spiegeleinrichtung (12), die an den zweiten Speisespannungsanschluß und den Spannungsreferenzknoten (8) geschaltet ist, und einen Rückkopplungsstrom zur ersten Strom-Spiegeleinrichtung (11) liefert;

einen ersten Feldeffekttransistor (13), dessen Source an den ersten Speisespannungsanschluß geschaltet ist, und dessen Gate und Drain an die erste Strom-Spiegeleinrichtung (11) geschaltet sind;

einen zweiten Feldeffekttransistor (15), dessen Gate an die erste Strom-Spiegeleinrichtung geschaltet ist, dessen Source an den Eingangsanschluß geschaltet ist, und der einen Drain hat; und

einen dritten Feldeffekttransistor (16) dessen Source an den Drain des zweiten Feldeffekttransistors geschaltet ist, dessen Gate an den Verstärkungsanschluß geschaltet ist, und dessen Drain an die zweite Strom-Spiegeleinrichtung geschaltet ist.

3. CMOS-Schaltung nach Anspruch 2, wobei die Ausgangseinrichtung (26-29, 31-33) umfaßt:

eine dritte Strom-Spiegeleinrichtung (36), die zwischen den zweiten Speisespannungsanschluß und den Ausgangsstromsenkanschluß geschaltet ist, und einen Strom vom Ausgangsstromsenkanschluß senkt;

einen vierten Feldeffekttransistor (26), dessen Source an den Eingangsanschluß geschaltet ist, dessen Gate an die Spannungs-Stro-



umsetzung-Einrichtung geschaltet ist, und der einen Drain hat;

einen fünften Feldeffekttransistor (27), dessen Source und dessen Gate an den Drain des vierten Feldeffekttransistors (26) geschaltet sind, und dessen Drain an die dritte Strom-Spiegeleinrichtung geschaltet ist; und

einen sechsten Feldeffekttransistor (32), dessen Source an den Eingangsanschluß geschaltet ist, dessen Gate an das Gate des vierten Feldeffekttransistors (26) geschaltet ist, und dessen Drain an den Ausgangsstromquellenanschluß (35) geschaltet ist.

4. Komplementär-Metalloxid-Halbleiter (CMOS)-Spannung-Stromumsetzung-Schaltung, die umfaßt:

einen ersten Speisespannungsanschluß

(1);

einen zweiten Speisespannungsanschluß

(2);

einen Eingangsanschluß (3);

einen Ausgangsstromsenkanschluß (35);

einen Ausgangsstromquellenanschluß

(34);

einen Verstärkungsanschluß (17);

einen ersten Widerstand (6), der zwischen den Eingangsanschluß und den Spannungsreferenzknoten (8) geschaltet ist;

einen zweiten Widerstand (7), der zwischen den Spannungsreferenzknoten (8) und den zweiten Speisespannungsanschluß geschaltet ist;

einen ersten Feldeffekttransistor (13), dessen Source an den ersten Speisespannungsanschluß geschaltet ist, und der ein Gate und einen Drain hat;

einen zweiten Feldeffekttransistor (15), dessen Source an den Eingangsanschluß geschaltet ist, dessen Gate an einen Stromreferenzknoten (18) geschaltet ist, und der einen Drain hat;

einen dritten Feldeffekttransistor (16), dessen Source an den Drain des zweiten Feldeffekttransistors geschaltet ist, dessen Gate an den Verstärkungsanschluß geschaltet ist, und der einen Drain hat;

einen vierten Feldeffekttransistor (26), dessen Source an den Eingangsanschluß geschaltet ist, dessen Gate an den Stromreferenzknoten geschaltet, und der einen Drain hat;

einen fünften Feldeffekttransistor (27), dessen Source und dessen Gate an den Drain des vierten Feldeffekttransistors geschaltet sind, und der einen Drain hat;

einen sechsten Feldeffekttransistor (32), dessen Source an den Eingangsanschluß geschaltet ist, dessen Gate an den Stromreferenz-

knoten (18) geschaltet ist, und dessen Drain an den Ausgangsspannungsquellenanschluß (35) geschaltet ist;

einen siebenten Feldeffekttransistor (22), dessen Source an den Eingangsanschluß geschaltet ist, dessen Gate an den Stromreferenzknoten (18) geschaltet ist, und dessen Drain an das Gate und den Drain des ersten Feldeffekttransistors geschaltet ist;

einen achten Feldeffekttransistor (23), dessen Source an den Eingangsanschluß geschaltet ist und dessen Gate und dessen Drain an den Stromreferenzknoten (18) geschaltet sind;

einen neunten Feldeffekttransistor (24), dessen Source und dessen Gate an den Drain des siebenten Feldeffekttransistors geschaltet sind, und dessen Drain an den Spannungsreferenzknoten (8) geschaltet ist;

einen zehnten Feldeffekttransistor (25), dessen Drain an den Stromreferenzknoten (18) geschaltet ist, dessen Gate an das Gate des neunten Feldeffekttransistor (24) geschaltet ist, und dessen Source an den Verstärkungsanschluß (17) geschaltet ist;

einen Verstärkungswiderstand (14), der zwischen den Verstärkungsanschluß (17) und den zweiten Speisespannungsanschluß geschaltet ist;

einen elften Feldeffekttransistor (21), dessen Gate und dessen Drain an den Drain des dritten Feldeffekttransistors (16) geschaltet sind, und dessen Source an den zweiten Speisespannungsanschluß geschaltet ist;

einen zwölften Feldeffekttransistor (19), dessen Drain an den Spannungsreferenzknoten (8) geschaltet ist, dessen Gate an das Gate des elften Feldeffekttransistors (21) geschaltet ist, und dessen Source an den zweiten Speisespannungsanschluß geschaltet ist;

einen dreizehnten Feldeffekttransistor (28), dessen Gate und dessen Drain an den Drain des fünften Feldeffekttransistors (27) geschaltet sind, und dessen Source an den zweiten Speisespannungsanschluß geschaltet ist; und

einen vierzehnten Feldeffekttransistor (29), dessen Drain an den Ausgangsstromsenkanschluß (34) geschaltet ist, dessen Gate an das Gate des dreizehnten Feldeffekttransistors (28) geschaltet ist, und dessen Source an den zweiten Speisespannungsanschluß geschaltet ist.

Revendications

1. Circuit convertisseur de tension en courant à transistors métal-oxyde-semiconducteur complémentaires (CMOS), comprenant :



une première borne de tension d'alimentation (1) couplée de façon à recevoir une première tension d'alimentation ;

une deuxième borne de tension d'alimentation (2) couplée de façon à recevoir une deuxième tension d'alimentation, la première tension d'alimentation étant supérieure à la deuxième tension d'alimentation ;

une borne d'entrée (3) couplée de façon à recevoir une tension de conversion ;

une borne (35) de puits de courant de sortie ;

une borne (34) de source de courant de sortie ;

un moyen diviseur de tension (4, 6, 7) couplé entre ladite deuxième borne de tension d'alimentation et ladite borne d'entrée, où ladite tension de conversion fournit une puissance électrique au circuit CMOS et peut varier sur un intervalle s'étendant depuis deux tensions de seuil au-dessus de ladite deuxième tension d'alimentation jusqu'à un potentiel de jonction grille-source de transistor au-dessus de ladite première tension d'alimentation, ledit moyen diviseur de tension ayant un noeud de référence de tension (8) servant à fournir une tension de référence par rapport à ladite tension de conversion appliquée à ladite borne d'entrée ;

un moyen de conversion de tension en courant (11, 12, 14, 15, 16) couplé auxdites première et deuxième bornes de tension d'alimentation et à ladite borne d'entrée, et couplé audit noeud de référence de tension de façon à fournir un courant de référence linéaire dont l'intensité varie linéairement en fonction d'une variation correspondante de ladite tension de conversion ; et

un moyen de sortie (26 à 29, 31 à 33) électriquement alimenté entre ladite deuxième borne de tension d'alimentation et ladite borne d'entrée et couplé audit moyen convertisseur de tension en courant de façon à produire respectivement un courant de puits de sortie et un courant de source de sortie sur ladite borne de puits de courant de sortie et ladite borne de source de courant de sortie, où l'intensité dudit courant de puits de sortie et l'intensité dudit courant de source de sortie sont une fraction de l'intensité dudit courant de référence linéaire.

2. Circuit CMOS selon la revendication 1, où ledit moyen convertisseur de tension en courant comprend :

une borne de gain (17) ;

une résistance de gain (14) couplée entre ladite borne de gain et ladite deuxième borne de tension d'alimentation ;

un premier moyen miroir de courant (11)

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couplé entre ladite borne d'entrée et ladite borne de gain et couplé audit noeud de référence de tension (8) de façon à produire ledit courant de référence linéaire, où la valeur de ladite résistance de gain (14) détermine, en relation avec l'amplitude de ladite tension de conversion, l'intensité dudit courant de référence linéaire circulant dans ledit premier moyen miroir de courant (11) ;

un deuxième moyen miroir de courant (12) couplé à ladite deuxième borne de tension d'alimentation et audit noeud de référence de tension (8) de façon à fournir un courant de réaction audit premier moyen miroir de courant (11) ;

un premier transistor à effet de champ (13) possédant une source qui est couplée à ladite première borne de tension d'alimentation ainsi qu'une grille et un drain qui sont couplés audit premier moyen miroir de courant (11) ;

un deuxième transistor à effet de champ (15) possédant une grille qui est couplée audit premier moyen miroir de courant, une source qui est couplée à ladite borne d'entrée, et possédant un drain ; et

un troisième transistor à effet de champ (16) possédant une source qui est couplée audit drain dudit deuxième transistor à effet de champ, une grille qui est couplée à ladite borne de gain, et un drain qui est couplé audit deuxième moyen miroir de courant.

3. Circuit CMOS selon la revendication 2, où ledit moyen de sortie (26 à 29, 31 à 33) comprend :

un troisième moyen miroir de courant (36) couplé entre ladite deuxième borne de tension d'alimentation et ladite borne (34) de puits de courant de sortie de façon à absorber le courant venant de ladite borne de puits de courant de sortie ;

un quatrième transistor à effet de champ (26) possédant une source qui est couplée à ladite borne d'entrée, une grille qui est couplée audit moyen de conversion de tension en courant, et possédant un drain ;

un cinquième transistor à effet de champ (27) possédant une source et une grille couplées audit drain dudit quatrième transistor à effet de champ (26) et un drain couplé audit troisième moyen miroir de courant ; et

un sixième transistor à effet de champ (32) possédant une source qui est couplée à ladite borne d'entrée, une grille qui est couplée à ladite grille dudit quatrième transistor à effet de champ (26), et un drain qui est couplé à ladite borne (35) de source de courant de sortie.

4. Circuit convertisseur de tension en courant à transistors métal-oxyde-semiconducteur complémentaires (CMOS), comprenant :



une première borne de tension d'alimentation (1);

une deuxième borne de tension d'alimentation (2);

une borne d'entrée (3);

une borne de puits de courant de sortie (35);

une borne de source de courant de sortie (34);

une borne de gain (17);

une première résistance (6) couplée entre ladite borne d'entrée et un noeud de référence de tension (8);

une deuxième résistance (7) couplée entre ledit noeud de référence de tension (8) et ladite deuxième borne de tension d'alimentation;

un premier transistor à effet de champ (13) possédant une source qui est couplée à ladite première borne de tension d'alimentation, et possédant une grille et un drain;

un deuxième transistor à effet de champ (15) possédant une source qui est couplée à ladite borne d'entrée, une grille qui est couplée à un noeud de référence de courant (18), et possédant un drain;

un troisième transistor à effet de champ (16) possédant une source qui est couplée audit drain dudit deuxième transistor à effet de champ, une grille qui est couplée à ladite borne de gain, et possédant un drain;

un quatrième transistor à effet de champ (26) possédant une source qui est couplée à ladite borne d'entrée, une grille qui est couplée audit noeud de référence de courant, et possédant un drain;

un cinquième transistor à effet de champ (27) possédant une source et une grille qui sont couplées audit drain dudit quatrième transistor à effet de champ, et possédant un drain;

un sixième transistor à effet de champ (32) possédant une source qui est couplée à ladite borne d'entrée, une grille qui est couplée audit noeud de référence de courant (18), et un drain qui est couplé à ladite borne de source de courant de sortie (35);

un septième transistor à effet de champ (22) possédant une source qui est couplée à ladite borne d'entrée, une grille qui est couplée audit noeud de référence de courant (18), et un drain qui est couplé à ladite grille et audit drain dudit premier transistor à effet de champ;

un huitième transistor à effet de champ (23) possédant une source qui est couplée à ladite borne d'entrée, et une grille et un drain qui sont couplés audit noeud de référence de courant (18);

un neuvième transistor à effet de champ (24) possédant une source et une grille qui sont

couplées audit drain dudit septième transistor à effet de champ, et un drain qui est couplé audit noeud de référence de tension (8);

un dixième transistor à effet de champ (25) possédant un drain qui est couplé audit noeud de référence de courant (18), une grille qui est couplée à ladite grille dudit neuvième transistor à effet de champ (24), et une source qui est couplée à ladite borne de gain (17);

une résistance de gain (14) couplée entre ladite borne de gain (17) et ladite deuxième borne de tension d'alimentation;

un onzième transistor à effet de champ (21) possédant une grille et un drain qui sont couplés audit drain dudit troisième transistor à effet de champ (16), et une source couplée à ladite deuxième borne de tension d'alimentation;

un douzième transistor à effet de champ (19) possédant un drain qui est couplé audit noeud de référence de tension (8), une grille qui est couplée à ladite grille dudit onzième transistor à effet de champ (21), et une source qui est couplée à ladite deuxième borne de tension d'alimentation;

un treizième transistor à effet de champ (28) possédant une grille et un drain qui sont couplés audit drain dudit cinquième transistor à effet de champ (27), et une source qui est couplée à ladite deuxième borne de tension d'alimentation; et

un quatorzième transistor à effet de champ (29) possédant un drain qui est couplé à ladite borne de puits de courant de sortie (34), une grille qui est couplée à ladite grille dudit treizième transistor à effet de champ (28), et une source qui est couplée à ladite deuxième borne de tension d'alimentation.

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