Description

BACKGROUND OF THE INVENTION, EXEMPLARY PRIOR ART

The invention relates to a semiconductor memory, comprising a memory matrix of rows and columns of memory cells for storing, per row, data information and also error protective redundant information, said memory comprising an on-chip error correction device which is fed by column outputs of the memory matrix, for receiving one symbol for each accessed column, and first column selection means which are fed by said error correction device in order to present output signals for further use.

A semiconductor memory of this kind is described in United States Patent Specification 4,604,749. The known memory is a read-only memory (ROM). In addition to the first column selection means, the memory also comprises second column selection means which are connected between the memory matrix and the correction device. These second column selection means select a comparatively small number of columns, so that a comparatively short code word is presented to the error correction device. It will be apparent that the terms "columns" and "rows" can be interchanged throughout in the reference. The described code is a so-called shortened (38, 32, 3) Hamming code with 38 code bits, 32 data bits and a minimum distance of 3 over the bits. As a result, a single-bit error can be corrected in 32 data bits, using a redundancy of 6/32 = 19%. The first column selection means select each time a single byte (8 bits) from the 32-bit word, which byte appears on an output. The efficiency of this code is comparatively low. Improvement of the efficiency would necessitate a longer code word, however, the implementation is already complex for an 38-bit code word. On the one hand this requires a comparatively large surface area on the integrated circuit and on the other hand the time required for decoding is comparatively long, so that the memory will be slower. Finally, the described organization is not suitable for a random access memory (RAM).

SUMMARY OF THE INVENTION

Among other things, it is an object of the invention to provide an improved semiconductor memory with a degree of error protection which can be adapted to the desired reliability and with an efficiency which is higher than that of the known memory, if desired; in which memory the delay incurred amounts to only a few gate delay times, and its set-up being suitable for a multitude of applications; it is a secondary object to enable the correction of incidental errors occurring during operation as well as of permanent (stuck-at) errors occurring during manufacture or at a later stage by means of the selected correction facilities, which errors may have a random configuration as well as be concentrated on a given column, so that the operating quality of an installed semiconductor memory can be maintained, or that a semiconductor memory containing errors can act as an error-free memory vis-à-vis the environment, so that in the latter case the yield of the manufacturing process can be increased or the price per circuit can be reduced.

According to the invention as claimed in claim 1 these objects are reached in that in that the memory matrix in the row direction comprises a succession of at least two patterns of each at most n columns each, in that the error correction device is connected to the column outputs according to an analogous repetitous pattern for operating according to an (n,k) spatial convolutional code, wherein (n > k), inasmuch as within a said pattern the redundant information is assigned to only fill a predetermined number of (n-k) columns of the pattern in question completely in order to render each time a data symbol of the convolution code correctable for any constraint length of the code, as expressed in the number of columns, while exchanging syndrome bits and subsidiary syndrome bits between neighbouring pattern periods.

In the above, a symbol is a bit group of standard length that is uniform over the code, e.g. one, two, four, eight bits, other lengths being applicable as well. All calculations are done in the appropriate Galois field. In the scope of the invention a column may store one symbol per row and therefore the word column may have a wider stract meaning than according to standard memory technology that restricts to single bit symbols. On a technology level, the present invention need not depart from conventional bit-organized storage, it is only that a plurality of bit storage position form part of a single-symbol column.

The code may either be systematic or non-systematic on the level of a symbol. Systematic codes are easier to decode, non-systematic codes have shorter constraint length sometimes and therefore a higher correction capability.

A spatial convolution code is to be understood to mean a code for which the delay operator D of the generating polynomial does not have the meaning of a symbol cell delay in time, but rather the meaning of a shift in space over one pattern. The patterns may be arranged in a finite series. In that case the first complete pattern is not preceded by any neighbouring pattern in the first direction. The last complete pattern is then followed in the second direction by a series of one or more incomplete

patterns or the first pattern is preceded by one or more incomplete patterns. The patterns may also be arranged in a quasi-infinite series. In that case the first complete pattern is preceded in the first direction directly by the last pattern in the second direction in that the necessary looping through for signals is provided. In that case no incomplete patterns need be provided. Alternatively, there may be formed a combination so that in the first and/or the second direction one or more incomplete final patterns are present, a given looping through of signals also being provided.

A pattern is a notional group of columns. In principle these groups can be arranged so as to be interleaved; this can be realized by means of the second column selection means. This arrangement may sometimes be advantageous, for example when "burst errors" occur. These burst errors can occur if the effect of a so-called pinhole is likely to extend across two (or more) adjoining columns. Another advantage may be that connection lines could be shorter and/or the surface area required could be smaller and/or the delay times could be shorter.

The invention can be used notably in very large semiconductor memories, for example 1 Mbit per chip. Due to the repetitive patterns, at least one symbol error can be corrected per constraint length which is a term known from the theory of convolution codes. In contrast therewith, the cited semiconductor memory uses a block code. At the end of the series of patterns only a small amount of additional redundancy may be required. The code can be systematic at the bit level; this results in a simple correction device. The code may also be non-systematic at the bit level. This necessitates matrix inversion (known per se) after the correction. The advantage of a non-systematic code sometimes consists of the smaller constraint length, so that the correction capability is de facto increased. If some steps are taken, the invention can also be used for a random access memory (RAM) or even for a dynamic RAM memory for the realization of the refresh organization. Furthermore, the error protection thus realized can be combined extremely well with the protection against faulty rows of memory cells by means of redundant rows of cells which can act as substitutes. In principle, the efficiency of the code in accordance with the invention may be either higher or lower than that of the known memory.

FURTHER ASPECTS OF THE INVENTION

Preferably, second column selection means are connected between the memory matrix and the correction device. Such second column selection means are known from the state of the art, but the proportioning in accordance with the invention is usually completely different. In the case of a 1 Mbit memory, there will be 1024 data columns (32 words of 32 bits). The known memory then comprises, for example 32x38=1216 columns in total. The selection factor of the second column selection means then amounts to 32; the selection factor of the first column selection means then amounts to only 4. In accordance with the present invention, in the case of a (9, 8) looped-through code there are, for example 128x9=1152 columns. The selection factor of the second column selection means then amounts to, for example 4: from every four successive columns (4p, 4p+1, 4p+2, 4p+3), where p = 0, 1, 2, ..., each time the column 4p+q is then selected, where q is independent of p and selectable as 0, 1, 2, 3. The selection factor of the first column selection means then amounts to, for example 32. It will be apparent that the proportioning may also be different.

The invention also relates to an integrated circuit comprising a semiconductor memory of the described kind. Such a circuit may comprise, for example, several semiconductor memories which are provided all or in part with an on-chip error correction device. Alternatively, other sub-systems may be present, for example an arithmetic and logic unit, an input/output sub-system and an interconnecting bus system, a memory management unit, and others.

Further aspects of the invention are recited in the other Claims.

BRIEF DESCRIPTION OF THE FIGURES

The invention will be described in detail hereinafter with reference to the Figures in particular relating to an (n, n-1) code that is systematic and has single bit symbols. Other convolutional codes are known in the art, principally for use with data communication along serial lines. In the Figures

Figure 1 shows a block diagram of a memory in accordance with the invention;

Figure 2 shows a block diagram of an error correction device with a code efficiency amounting to 1/2;

Figure 3 shows a similar block diagram for an efficiency amounting to 3/4;

Figure 4 shows a similar block diagram for an efficiency amounting to 7/8;

Figure 5 shows an elaboration of Figure 2 in order to form a random access memory.

SYSTEM DESCRIPTION

Figure 1 shows a block diagram of a memory in accordance with the invention. The entire device

is accommodated on a single integrated circuit.

Element 22 is the row decoder; this decoder receives a row address, for example consisting of bits, whereby one of at the most 1024 rows of memory cells is addressed. The row decoder may include a permanent translation of the address of one or more rows found to be faulty into the address of a respective substitute redundant row. Assume that the aim is to have 1024 information bits available per row after correction. In accordance with a code having an efficiency amounting to 3/4, to be desdribed hereinafter, a row should then contain 1367 code bits which appear on the data outputs of the memory matrix after the addressing of the row. (In practice, for example in order to save electric power, a matrix of 1024x1367 cells will usually be subdivided into four submatrices of 512 rows and a number of columns which is slightly larger than 1367:2, for example, 385, the exact number being determined by the implementation; however, this subdivision will not be elaborated herein). Element 24 is an error correction device which has a mainly modular construction and which will be described in detail hereinafter. For an efficiency amounting to 3/4, the total 1 Mbit matrix can now output 1024 data bits. These data bits will be corrected for many errors, even though it always remains possible that non-correctable errors were present. When these errors concern manufacturing errors, they can be detected during manufacture. However, during this detection the error correction device can be deactivated by a special user-controlled test signal. Further hard errors can also arise during later use. The resultant number of 1024 is not output in parallel. To this end there are provided first column selection means (column decoder) 26. If only 1 bit is to be selected, this decoder receives a 10-bit column address. When the data connection has a path width of 8 bits, a 7-bit address suffices. The column decoder 26 thus has a known multiplexer function.

The error correction device receives a series of patterns of bits, for example each time n = 2, 4, 8 or 16 bits per pattern. At one or at both ends these patterns may be supplemented by a number of partial patterns as will be described hereinafter. For each pattern each time n = 1, 3, 7, 15... bits are output in a preferred embodiment. For the partial patterns this number is smaller than the standard number for the relevant code. In a preferred embodiment, all codes are systematic at the bit level as will be explained hereinafter. Further, convolution in the time domain is known per se. The present invention, however, utilizes convolution codes in the spatial domain; moreover, the use in matrix memories has far-reaching consequences for the decoding.

In addition to the described components, the semiconductor memory shown in Figure 1 may also comprise further components such as :

- a second and further memory matrices,
- components for data processing, such as ALU, buses, I/O organization;
- second column selection means which are connected between the matrix and the associated error correction device for effecting spatial interleaving; these means select each time one column from each group of two, four, etc. columns in order to connect it to the input of the error correction device. The selection factor of these second column selection means is then smaller than that of the first column selection means;
- means for initiating also write operations with associated encoding in order to form the necessary redundancy per pattern;
- a refresh control system which regularly presents memory addresses in accordance with some procedure or other in order to read the part of the memory thus addressed and fill it again with the same information (corrected or not). Various strategies are feasible for the formation of the addresses.

DESCRIPTION OF SOME ERROR CORRECTION DEVICES

Figure 2 shows a block diagram of an error correction device having a code efficiency amounting to 1/2. Between the vertical broken lines a single pattern period is shown. This sample example involves one parity bit line (column line) 40 and one data bit line (42). When a row of memory cells is activated, one bit appears on all activated column lines. In an input stage 44 a presyndrome bit (am) is formed from these two bits by means of an EXCLUSIVE-OR function. Furthermore, in this simple case the data bit is treated as a first subsidiary syndrome bit. In the second stage of the error correction device the subsidiary syndrome bit of the left-neighbouring pattern period and the local presyndrome bit are used to form a syndrome bit sm by means of an EXCLUSIVE-OR element 46. If there is no left-neighbouring period, bm = 0 and the element 46 may be omitted, if desired. In a combination stage a modification bit is formed from the local syndrome bit sm and the syndrome bit of the right-neighbouring pattern period by means of an AND-gate 48. The digits stated in the supply leads for the bits originating from the memory cells indicate in which pattern period the relevant bit is used. The first 1 indicates that both bits are used for the relevant period. The second bit indicates whether the relevant bit received is used (1) or not (0) for the right-next pattern period. In this case

only the data bit is used. When the pattern period in question (m) is the last complete pattern period, only the parity column need be provided for the next pattern period, the full correction capability still being maintained for the last complete pattern period. For this additional parity period the elements 44, 48, 50 could in principle be omitted. The various possibilities for the terminating columns will be described hereinafter. Finally, in the modification stage 50 the data to be output is modified, if necessary, by means of an EXCLUSIVE-OR function.

Figure 3 shows a similar block diagram for an efficiency amounting to 3/4. The bits fetched from the memory cells appear on four column lines 60, 62, 64, 66. The three bits given for each incoming bit line indicate the pattern period for which the respective bit is relevant.

In the correction device a presyndrome bit am is formed in a first stage from the four bits received,using three EXCLUSIVE-OR functions 68, 70, 72. If none of the four bits received is disturbed, this presyndrome bit has the value zero. Furthermore, in parallel therewith, the presyndrome bit b(m+1) is formed by means of the EXCLUSIVE-OR function 74. Furthermore, again in parallel therewith, a second subsidiary syndrome bit c(m+2) is formed by means of the EXCLUSIVE-OR function 70 which has also been used for the presyndrome. A suitable choice of the respective EXCLUSIVE-OR functions aims to minimize the number of these functions and also to realize a short delay time for the signals.

Using the local syndrome bit sm, the first subsidiary syndrome bit of the left-neighbouring pattern period (bm) and the second subsidiary syndrome bit (cm) of the left-neighbouring pattern period but one, the local syndrome bit sm is formed in a second stage by means of EXCLUSIVE-OR functions 76, 78.

The third stage consists of three AND-gates 80, 82, 84, each gate for a respective data bit to be output, comprising partly inverted inputs which are denoted by a circle. Each of these three AND-gates receives the local and non-inverted syndrome bit. They all receive also (possibly inverted) the syndrome bit s(m+1) of the right-neighbouring pattern period and also the syndrome bit s(m+2) of the right-neighbouring pattern period but one. The gate 80 also receives (inverted) the syndrome signal of the left-neighbouring pattern period. The inversion of the data bits for correction is again realized by means of three EXCLUSIVE-OR functions 86, 88, 90.

The code used resembles the code in the time domain proposed by Wyner and Ash (Peterson and Weldon, Error correcting codes, M I T Press, Cambridge Mass./London, 1972, page 402). In the present application, however, the decoding is unconventional. For example, the syndrome is not updated for errors corrected in other pattern periods because that would cause in an excessive delay. In principle each time only 1 bit error can be corrected within the constraint length. This constraint length amounts to 17 bits in Figure 3. This means that two arbitrary, incorrect bits can be corrected with certainty if they are separated by at least 17 non-disturbed (code) bits. The constraint length relates to the most unfavourable case. In given error configurations the distance may be less than 17 bits. The constraint length can usually be further reduced by utilizing a non-systematic code.

Figure 4 shows a diagram which corresponds to Figure 3 for an efficiency amounting to 7/8. The constraint length is 51 bits, so that always 1 bit can be corrected for at the most 52 bits. On the bit line 100 a parity bit appears, while a data bit appears each time on the lines 102-114. The EXCLUSIVE-OR gates 116, 120, 122, 126, 132, 134, 136 form a presyndrome bit. Furthermore, the following subsidiary syndrome bits are formed for use in other pattern periods:

- the bit b(m+1) for the right-next pattern period by means of the EXCLUSIVE-OR gates 118, 124, 128;
- the bit c(m+2) for the right-next pattern period but one by means of the EXCLUSIVE-OR gates 120, 126, 130;
- the bit d(m+3) for the right-next pattern period but two by means of the EXCLUSIVE-OR gates 122, 126, 130.

In the second stage the corresponding subsidiary syndrome bits bm, cm, dm are processed in order to form the local syndrome bit sm from the local presyndrome bit am, that is to say in the following EXCLUSIVE-OR gates:

bm : 142, 138, 140
cm : 142, 138, 140
dm : 140.

The third stage consists of seven AND-gates with partly inverted inputs 144-156, i.e. one for each data bit to be output. In these combination gates the syndrome bit of the current pattern period is combined with the syndrome bit of the first, the second and the third most-neighbouring periods at the right and with the syndrome bits of the first and the second most-neighbouring pattern periods at the left.

In a fourth stage, the respective bits read are updated by means of the EXCLUSIVE-OR gates 158-170, utilizing the modification bits formed in the gates 144-156.

In the above, it is possible in principle for any pattern to have a lesser number of non-redundant columns. This is solved by feeding the decoder with logical zeroes for this column and omitting the

associated bit output. Often, further simplifications may then be introduced.

IE FACILITIES AT THE TERMINATIONS

Figures 2-4 show the situation for a quasi-infinite row of pattern periods. In Figure 2 at least one further pattern period is provided at each end; in Figure 3 at least two of such periods are provided at both ends, while in Figure 4 at least three of such pattern periods are provided at both ends. This condition is not satisfied at the beginning of the series of pattern periods.

In Figure 2 the subsidiary syndrome bit bm standard has the value zero, or it is not provided; the output of the syndrome bit sm to the left can be omitted. In Figure 3 the subsidiary syndrome bits bm, cm, cm+1, standard have the value zero, or they are not provided and the EXCLUSIVE-OR gates fed thereby can be omitted, if desired. The output of the syndrome bits sm, s(m+1) to the left can then be omitted. The applied syndrome bit s-(m-1) standard has the value 0, or the relevant input of the gate 80 is not provided. In Figure 4 the subsidiary syndrome bits bm, sm, c(m+1), dm, d-(m+1), d(m+2) standard have the value zero, or they are not provided, and the EXCLUSIVE-OR gates fed thereby can be omitted, if desired. The output of the syndrome bits sm, s(m+1), s(m+2) to the left can be omitted. The applied syndrome bits s(m-2), s(m-1), standard have the value 0, or the relevant inputs of the gates 144, 146, 148 are not provided (all these gates receive the inverted values of these signals!). The termination of the series of pattern periods to the left in this manner does not affect the correction capability of the spatial convolution code.

Generally, specific steps for correctly terminating the series must also be taken at the right-hand end of the series of pattern periods. A first possibility consists in the provision of partial pattern periods at the right-hand end. In Figure 2 the bit line 40 concerns only the current pattern period and in the sole partial pattern period at the right-hand end this bit line should be provided. The bit line 42 would then also concern a non-existing pattern period, so that the latter need not be provided. The sequence of the bit lines at the right-hand end is then ... 40, 42-40, 42-40.

In the configuration shown in Figure 3, the bit line 60 (code 100) is relevant only for the respective pattern period. At the end of a series of pattern periods, this line (in a partial period) must still be provided as the last one. The other three lines of that period would also concern non-existing pattern periods, so that they would not make sense. The last period but one may then comprise at the most the bit lines 60, 62 (the lines 64, 66 with the code ..., ..., 1 would then concern a non-existing pattern period and hence would not make sense). The last pattern period but two may be complete. The sequence of the bit lines at the end of the row may therefore be:
(60, 62, 64, 66) - (60, 62) - (60).

Similarly, in Figure 4 the following bit lines may be provided at the end of the row of pattern periods:
(100,102,104,106,108,110,112,114)-
(100,102,104,106)-(100,102)-(100).

The foregoing can be modified by omitting given bit lines (not the parity bit lines 40, 60, 100) if they are superfluous for the use of the memory. Example: 512:7=73+1. In the case of Figure 4, different combinations of the lines 102-106 could be omitted from the last three partial periods. Generally, non-redundant columns of memory cells may be omitted at random (at least in the case of a systematic code). For example, an (8,7) code can be converted into a (7, 6) code if this would be advantageous for the capacity of the memory.

The opposite can also take place, so that only complete pattern periods are provided, but the irrelevant column lines are not taken into account. In the case of a CAD system this could be advantageous because of the increased correspondence between successive pattern periods.

A third possibility where the surface area is also reduced consists in the cyclic looping through of the pattern periods. However, the total width of the memory must then be larger than the constraint length, because otherwise the code would be ineffective. In Figure 4 the following signals are then output at the right-hand side: b(m+1), c(m+2), c-(M+1), d(m+3), d(m+2), d(m+1), s(m-1), sm. Moreover, at this side the following signals are input: s(m+1), s(m+2), s(m+3). These eleven signals can be looped through in the row direction from one side of the series of pattern periods to the other side in order to be used in the relevant pattern periods. In Figure 4 the drawbacks of these eleven signal paths must be considered in relation to three redundant memory columns. Depending on the dimensions of the memory, one solution or the other will be more attractive. In the solution given in Figure 3, the trade-off would be four additional signal lines versus two additional columns of memory cells. Intermediate solutions are also feasible: if the series of pattern periods comprises the following numbers of bit lines: ..., 8, 4, 2, 1 in Figure 4, exclusively the last column of redundant memory cells can be included in the first complete pattern period; however, a large number of signals must then still be looped through.

FURTHER ELABORATIONS AND SUPPLEMENTS TO THE INVENTION

The invention can be extended and supplemented in various ways. First of all, the dimension of a pattern period can be modified. It can be extended, for example to 16, 32 columns. On the one hand the redundancy is thus reduced. On the other hand, the constraint length thus increases rapidly, so that the overall correction capability decreases. The determination of the optimum value, that is the optimum yield of the manufacturing process, is then co-determined by the number of expected errors, for example so-called pinholes.

A further drawback of the larger pattern period consists in that the logic depth of the error correction circuit increases, so that the circuit becomes slower. The de-activation of the error correction circuit in order to perfrom a test or to increase the processing speed in normal user circumstances is realized as follows. All AND-gates (so 144 ... 156 in Figure 4) are provided with an additional input. In the normal user condition, all additional inputs are activated with a logic "1", so that the error correction device operates in the described manner. In the test mode, all additional inputs are activated by means of a logic "0". As a result, all AND-gates output a logic "0" and the EXCLUSIVE-OR gates 158-170 operate as non-inverting gating elements. As a result, an external test can be performed on the data pattern delivered. However, in the example, the redundant column of memory cells itself cannot be tested in this manner. If strictly necessary, the data thereof can be applied to one of the external outputs by way of a multiplexer which has been omitted for the sake of simplicity.

Figure 5 shows an extension of Figure 2 in the form of a random access memory. The elements 40, 42, 44, 46, 48, 50 have already been described with reference to Figure 2. The following additional parts are provided. First of all, there are provided bidirectional connecting stages 200/202 for each column of memory cells, possibly with an additional control line for activating only one of the two feasible directions. There is also provided an encoding/decoding control input 204. This input controls first of all the circuit 206. In a simple embodiment, the element 214 is omitted, but the data output of the column 42 is connected directly to inputs of EXCLUSIVE-OR elements 44 of the first stage and 50 of the modification stage. In an improved solution, a multiplexer 214 is connected therebetween, which multiplexer conducts its upper input upon decoding. During the decoding operation, the circuit 206 conducts the signal on the column 40 so that the signals am, sm and the possibly corrected data bit on the output 208 are formed in the previously described manner. Furthermore, during the decoding operation the series combination of the multiplexer 212 and the latch circuit 210 operates so that the corrected data thus formed does not initiate the writing of modified data: multiplexer 212 is generally maintained in the left-hand position and the decoding signal blocks the latch 210 so that the latter does not supply a signal. The multiplexer 212 is set to the right-hand position only by the write address (WA) for the columns for which new data is to be written. Another solution for the element 206 is formed by a logic AND-gate which is blocked by the encoding signal. During writing, the signal on the line 204 is initially activated for all columns in the same way as for a read operation. However, the signal for the multiplexer 212 is set to the right-hand position only for the columns to be selected (by means of the first column selection means). During writing it is also necessary to determine the redundancy to be written, which redundancy depends on the data bits to be newly written as well as on the data bits already present. Therefore, in principle the entire redundancy is determined anew. It would be possible to leave redundancy bits which are situated "far away" unaffected, but the comparatively complex control circuitry then required is not provided. During a first phase, the data to be newly written is stored, via the multiplexer 212, in the latch circuit 210 under the control of the encoding signal (212 is in the right-hand position). For the data bits to be maintained, the multiplexer 212 is in the left-hand position so that these bits are stored in the relevant latch circuits 210. If present, the multiplexer 214 is in the lower position so that this new data bit takes the place of the data bit thus far present in the memory cell. If the multiplexer 214 is not provided, it is assumed that the stationary output signal of the latch circuit 210 prevails over a dynamic output signal of the element 202. The multiplexer 206 then outputs a logic 0. As a result, without the influence of the redundancy stored thus far, the new redundancy is calculated by way of the elements 44, 46. During a subsequent write phase, the redundancy bit (which is the same as the syndrome bit when the local redundancy bit has the value zero during decoding) and the data bit are written via the elements 200/202.

For the versions shown in the Figures 3, 4 and generally for (n, n-1) spatial convolution codes corresponding solutions can be used; these solutions require first of all a blocking element between the output of the redundant columns and the associated input of the correction device. Secondly they require a hold element for all data bits and a controllable selection element, so that the newly received data bits as well as the data bits to be maintained can be stored therein, as desired. Finally, they require a feedback for applying the

syndrome bits to the relevant columns of redundant memory cells. It is to be noted that in the described realization the syndrome bit is co-determined by already stored data bits of other parts of the memory (in this case represented by the bit bm; in the Figures 3, 4 by all signals bm (..), c(..), d(..) described). Because the modifications are upon correction performed only in the modification stage (which stage is idle during the encoding), the correct redundant information will be stored. Other solutions are also possible, for example, solution where the data bits to be maintained are read but not written again. To this end, the read/write control signal for the element 201 is co-determined by the write address WA. This will usually be a less attractive solution.

In a random access memory in dynamic MOS technology, refresh cycles must also be executed. In a simple embodiment, the information may remain unmodified. This can be realized in that the read/write elements 200, 202 have a sufficient node capacity for charging the cell node to an adequate voltage level during the sample mode after a precharge phase. A more refined solution consists in that a given degree of correction can be introduced by means of a circuit as shown in Figure 5. However, in that case the control deviates from that in the case of a write operation. First of all, all multiplexers then occupy to the left-hand position. Moreover, during the read operation all elements 206 are controlled so as to be conductive for the redundancy bits. As a result, corrections are performed on the redundancy bit (via the elements 44, 46) as well as on the data bit (via the elements 44, 46, 48, 50), be it of course no more than once within the actual constraint length.

The code can be extended, if desired, to an (n, n-j) code, where j = 2, 3, ... Generally, decoding will then be more complex. The solution shown in Figure 4 can be extended to n = 16, 32, ...; a higher efficiency will then be obtained.

Claims

1. A semiconductor memory comprising a memory matrix (20) of rows and columns of memory cells for storing, per row, data information and also error protective redundant information, said memory comprising an on-chip error correction device that is fed by column outputs of the memory matrix, for receiving one symbol for each accessed column, and first column selection means (26) that are fed by said error correction device in order to present output signals for further use, characterized in that the memory matrix (20) in the row direction comprises a succession of at least two patterns of at most n columns each, in that the error correction device (24) is connected to the column outputs according to an analogous repetitious pattern for operating according to an (n,k) spatial convolutional code, wherein (n > k), inasmuch as within a said pattern the redundant information is assigned to only fill a predetermined number of (n-k) columns of the pattern in question completely in order to render each time a data symbol of the convolution code correctable for any constraint length of the code, as expressed in the number of columns, while exchanging syndrome bits and subsidiary syndrome bits between neighbouring pattern periods.

2. A semiconductor memory as claimed in claim 1, said error correction device comprising the following four functional stages for each complete pattern:
   a. an input stage for forming a presyndrome (a_m) and at least one subsidiary syndrome symbol (b_{m+1},c_{m+2},d_{m+3}) from the information received from the memory cells;
   b. a second stage for receiving at least one subsidiary syndrome symbol (b_m,c_m,d_m) from a neighbouring pattern in a first direction, if present, and for forming a local syndrome (S_m) by means of the local presyndrome and of the at least one subsidiary syndrome symbol;
   c. a combination stage for forming, from the local syndrome and at least one syndrome symbol (S_{m+1},S_{m+2},S_{m+3}) of a neighbouring pattern in a second direction, if present, a modification signal for each information signal to be applied to the first column selection means;
   d. a modification stage for modifying an information signal under the control of a respective modification signal.

3. A semiconductor memory as claimed in Claim 1 or 2, characterized in that said at least two patterns have mutually identical column configurations.

4. A semiconductor memory as claimed in any of Claims 1, 2 or 3, characterized in that said spatial convolution code is a systematic code in that within each said pattern there are n-k columns devoted exclusively to storing redundant information.

5. A semiconductor memory as claimed in any of Claims 1 to 4, characterized in that each symbol consists of a single bit.



syndrome bits to the relevant columns of redundant memory cells. It is to be noted that in the described realization the syndrome bit is co-determined by already stored data bits of other parts of the memory (in this case represented by the bit bm; in the Figures 3, 4 by all signals bm (..), c(..), d(..) described). Because the modifications are upon correction performed only in the modification stage (which stage is idle during the encoding), the correct redundant information will be stored. Other solutions are also possible, for example, solution where the data bits to be maintained are read but not written again. To this end, the read/write control signal for the element 201 is co-determined by the write address WA. This will usually be a less attractive solution.

In a random access memory in dynamic MOS technology, refresh cycles must also be executed. In a simple embodiment, the information may remain unmodified. This can be realized in that the read/write elements 200, 202 have a sufficient node capacity for charging the cell node to an adequate voltage level during the sample mode after a precharge phase. A more refined solution consists in that a given degree of correction can be introduced by means of a circuit as shown in Figure 5. However, in that case the control deviates from that in the case of a write operation. First of all, all multiplexers then occupy to the left-hand position. Moreover, during the read operation all elements 206 are controlled so as to be conductive for the redundancy bits. As a result, corrections are performed on the redundancy bit (via the elements 44, 46) as well as on the data bit (via the elements 44, 46, 48, 50), be it of course no more than once within the actual constraint length.

The code can be extended, if desired, to an (n, n-j) code, where j = 2, 3, ... Generally, decoding will then be more complex. The solution shown in Figure 4 can be extended to n = 16, 32, ...; a higher efficiency will then be obtained.

Claims

1. A semiconductor memory comprising a memory matrix (20) of rows and columns of memory cells for storing, per row, data information and also error protective redundant information, said memory comprising an on-chip error correction device that is fed by column outputs of the memory matrix, for receiving one symbol for each accessed column, and first column selection means (26) that are fed by said error correction device in order to present output signals for further use, characterized in that the memory matrix (20) in the row direction comprises a succession of at least two patterns of at most n columns each, in that the error correction device (24) is connected to the column outputs according to an analogous repetitious pattern for operating according to an (n,k) spatial convolutional code, wherein (n > k), inasmuch as within a said pattern the redundant information is assigned to only fill a predetermined number of (n-k) columns of the pattern in question completely in order to render each time a data symbol of the convolution code correctable for any constraint length of the code, as expressed in the number of columns, while exchanging syndrome bits and subsidiary syndrome bits between neighbouring pattern periods.

2. A semiconductor memory as claimed in claim 1, said error correction device comprising the following four functional stages for each complete pattern:
   a. an input stage for forming a presyndrome (a_m) and at least one subsidiary syndrome symbol (b_{m+1},c_{m+2},d_{m+3}) from the information received from the memory cells;
   b. a second stage for receiving at least one subsidiary syndrome symbol (b_m,c_m,d_m) from a neighbouring pattern in a first direction, if present, and for forming a local syndrome (S_m) by means of the local presyndrome and of the at least one subsidiary syndrome symbol;
   c. a combination stage for forming, from the local syndrome and at least one syndrome symbol (S_{m+1},S_{m+2},S_{m+3}) of a neighbouring pattern in a second direction, if present, a modification signal for each information signal to be applied to the first column selection means;
   d. a modification stage for modifying an information signal under the control of a respective modification signal.

3. A semiconductor memory as claimed in Claim 1 or 2, characterized in that said at least two patterns have mutually identical column configurations.

4. A semiconductor memory as claimed in any of Claims 1, 2 or 3, characterized in that said spatial convolution code is a systematic code in that within each said pattern there are n-k columns devoted exclusively to storing redundant information.

5. A semiconductor memory as claimed in any of Claims 1 to 4, characterized in that each symbol consists of a single bit.

6. A semiconductor memory as claimed in any of Claims 1 to 5, characterized in that the convolution code is systematic at the bit level.

7. A semiconductor memory as claimed in any of Claims 1 to 6, characterized in that the convolution code is not systematic at the bit level, the first column selection means being associated with matrix inversion means.

8. A semiconducor memory as claimed in any one of the Claims 1 to 7, characterized in that the convolution code is an (n,n-1) code.

9. A semiconductor memory as claimed in any one of the Claims 1 to 8, characterized in that second column selection means are connected between the memory matrix and the error correction device.

10. A semiconductor memory as claimed in Claim 9, characterized in that the selection factor of the second column selection means is smaller than that of the first column selection means.

11. A semiconductor memory as claimed in any one of the Claims 1 to 10, characterized in that said pattern comprises at least $n=4$ columns in order to apply for each complete pattern (n-1) bits to the first column selection means, said second stage receiving subsidiary syndrome bits (C_m), each of which is formed from at least one data bit of a directly neighbouring pattern in a first direction, if present, the combination stage of a pattern receiving syndrome bits from the directly neighbouring pattern in a first direction (S_m) and from two successive directly neighbouring patterns in the second direction (S_{m+1},S_{m+2}) if present.

12. A semiconducor memory as claimed in any one of the Claims 1 to 11, characterized in that $n=2^j$, where $j \geq 3$.

13. A semiconductor memory as claimed in any one of the Claims 1 to 12, characterized in that for $n=2^j$ at least one incomplete final pattern is provided at at least one end of the series of patterns, all incomplete final patterns comprising at least the redundancy columns provided for each complete pattern in order to form therefrom syndrome bits and/or subsidiary syndrome bits in the error correction device.

14. A semiconductor memory as claimed in any one of the Claims 1 to 13, characterized in that at the end of a series of patterns there are provided connections for looping through to the other respective end of the series of necessary syndrome bits and subsidiary syndrome bits.

15. A semiconductor memory as claimed in any one of the Claims 1 to 14, characterized in that said first column selection means are bidirectionally active, for each redundant column there being provided syndrome bit forming means, an output of which can be connected to a column input of the redundant column in order to store a restored redundancy bit by way of information received from the environment and the information remaining in the memory matrix.

16. A semiconductor memory as claimed in any one of the Claims 1 to 15, characterized in that a modification stage connected to said first column selection means ignores a possible correction under the control of an ignore correction signal.

17. A semiconductor memory as claimed in any one of the Claims 11 to 16, characterized in that there is provided a substitution mechanism for continuously addressing a substitute row of memory cells instead of a faulty row of memory cells.

18. A semiconductor memory as claimed in Claim 15, characterized in that there is provided a refresh mechanism, the correction device being activatable under the control of a recurrent refresh signal in order to correct a correctable error.

19. An integrated circuit comprising a semiconductor memory as claimed in any one of the Claims 1 to 18.

Patentansprüche

1. Halbleiterspeicher mit einer Speichermatrix (20) aus Zeilen und Spalten von Speicherzellen zum zeilenweisen Speichern von Dateninformation und zugleich redundanter Fehlerschutzinformation, wobei der Speicher eine von Spaltenausgängen der Speichermatrix gespeiste mitintegrierte Fehlerkorrekturanordnung zum Empfangen eines einziges Symbols für jede Spalte, auf die zugegriffen wird, hat, und erste von der genannten Fehlerkotrekturanordnung gespeiste Spaltenselektionsmittel (26), um Ausgangssignale zur weiteren Verwendung anzubieten, dadurch gekennzeichnet, daß die Speichermatrix (20) in der Zeilenrichtung eine Folge von mindestens zwei Mustern von höch-

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stens je n Spalten umfaßt, daß die Fehlerkorrekturanordnung (24) mit den Spaltenausgängen entsprechend einem sich analog wiederholenden Muster verbunden ist, um entsprechend einem räumlichen (n,k)-Faltungscode zu arbeiten, mit (n > k), wobei innerhalb eines genannten Musters die redundante Information so zugeordnet wird, daß nur eine vorherbestimmte Zahl von (n-k) Spalten des betreffenden Musters vollständig gefüllt wird, um für jede Einschränkungslänge des Codes, wie in der Anzahl Spalten ausgedrückt, unter Austausch von Syndrombits und Nebensyndrombits zwischen benachbarten Musterperioden jeweils ein Datensymbol des Faltungscodes korrigierbar zu machen.

2. Halbleiterspeicher nach Anspruch 1, wobei die genannte Fehlerkorrekturanordnung die folgenden vier Funktionsstufen für jedes vollständige Muster enthält:

a. eine Eingangsstufe zur Bildung eines Vorsyndroms (a_m) und mindestens eines Nebensyndromsymbols (b_{m+1}, C_{m+2}, d_{m+3}) aus der von den Speicherzellen empfangenen Information;

b. eine zweite Stufe zum Empfang mindestens eines Nebensyndromsymbols (b_m, c_m, d_m) aus einem in einer ersten Richtung benachbarten Muster, falls vorhanden, und zur Bildung eines lokalen Syndroms (S_m) mit Hilfe des lokalen Vorsyndroms und des mindestens einen Nebensyndromsymbols;

c. eine Kombinationsstufe zur Bildung, aus dem lokalen Syndrom und mindestens einem Syndromsymbol (S_{m+1}, S_{m+2}, S_{m+3}) eines in einer zweiten Richtung benachbarten Musters, falls vorhanden, eines Modifikationssignals für jedes den ersten Spaltenselektionsmitteln zuzuführende Informationssignal;

d. eine Modifikationsstufe zum Modifizieren eines Informationssignals unter der Steuerung eines jeweiligen Modifikationssignals.

3. Halbleiterspeicher nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß mindestens zwei Muster miteinander identische Spaltenkonfigurationen haben.

4. Halbleiterspeicher nach einem der Ansprüche 1, 2 oder 3, dadurch gekennzeichnet, daß der räumliche Faltungscode ein systematischer Code ist, in dem Sinne, daß innerhalb jedes genannten Musters n-k Spalten ausschließlich für die Speicherung redundanter Information bestimmt sind.

5. Halbleiterspeicher nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß jedes Symbol aus einem einzigen Bit besteht.

6. Halbleiterspeicher nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß der Faltungscode auf der Bitebene systematisch ist.

7. Halbleiterspeicher nach einem der Ansprüche 1 bis 6, dadurch gekennzeichnet, daß der Faltungscode auf der Bitebene nichtsystematisch ist, wobei die ersten Spaltenselektionsmittel zu Matrixinversionsmitteln gehören.

8. Halbleiterspeicher nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß der Faltungscode ein (n,n-1)-Code ist.

9. Halbleiterspeicher nach einem der Ansprüche 1 bis 8, dadurch gekennzeichnet, daß zweite Spaltenselektionsmittel zwischen der Speichermatrix und der Fehlerkorrekturanordnung angeordnet sind.

10. Halbleiterspeicher nach Anspruch 9, dadurch gekennzeichnet, daß der Selektionsfaktor der zweiten Spaltenselektionsmittel Kleiner ist als der der ersten Spaltenselektionsmittel.

11. Halbleiterspeicher nach einem der Ansprüche 1 bis 10, dadurch gekennzeichnet, daß das genannte Muster mindestens n = 4 Spalten umfaßt, um den ersten Spaltenselektionsmitteln für jedes vollständige Muster (n-1) Bits zuzuführen, wobei die zweite Stufe Nebensyndrombits (C_m)empfängt, von denen jedes aus mindestens einem Datenbit eines in einer ersten Richtung direkt benachbarten Musters, falls vorhanden, gebildet ist, wobei die Kombinationsstufe eines Musters Syndrombits aus dem in einer ersten Richtung direkt benachbarten Muster (S_m) und aus zwei aufeinanderfolgenden, in der zweiten Richtung direkt benachbarten Muster (S_{m+1}, S_{m+2}), falls vorhanden, empfängt.

12. Halbleiterspeicher nach einem der Ansprüche 1 bis 11, dadurch gekennzeichnet, daß $n = 2^j$, mit $j \geq 3$.

13. Halbleiterspeicher nach einem der Ansprüche 1 bis 12, dadurch gekennzeichnet, daß es für $n = 2^j$ mindestens ein unvollständiges Endmuster an mindestens einem Ende der Reihe von Mustern gibt, wobei alle unvollständigen Endmuster mindestens die für jedes vollständige Muster vorgesehenen Redundanzspalten enthalten, um daraus in der Fehlerkorrekturanord-

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nung Syndrombits und/oder Nebensyndrombits zu bilden.

14. Halbleiterspeicher nach einem der Ansprüche 1 bis 13, dadurch gekennzeichnet, daß am Ende einer Reihe von Mustern Verbindungen vorgesehen sind, um zum anderen jeweiligen Ende der Reihe notwendiger Syndrombits und Nebensyndrombits durchzuschleifen.

15. Halbleiterspeicher nach einem der Ansprüche 1 bis 14, dadurch gekennzeichnet, daß die ersten Spaltenselektionsmittel in zwei Richtungen aktiv sind, wobei für jede redundante Spalte Syndrombitbildungsmittel vorgesehen sind, von denen ein Ausgang mit einem Spalteneingang der redundanten Spalte verbunden werden kann, um ein zurückgewonnenes Redundanzbit mit Hilfe der aus der Umgebung und der in der Speichermatrix verbleibenden Information empfangenen Information zu speichern.

16. Halbleiterspeicher nach einem der Ansprüche 1 bis 15, dadurch gekennzeichnet, daß eine mit den ersten Spaltenselektionsmitteln verbundene Modifikationsstufe unter der Steuerung eines "Korrektur-Ignorieren"-Signals eine eventuelle Korrektur ignoriert.

17. Halbleiterspeicher nach einem der Ansprüche 11 bis 16, dadurch gekennzeichnet, daß ein Substitutionsmechanismus vorgesehen ist, um anstelle einer fehlerhaften Speicherzellenzeile kontinuierlich eine Ersatzzeile von Speicherzellen zu adressieren.

18. Halbleiterspeicher nach Anspruch 15, dadurch gekennzeichnet, daß es einen Auffrischmechanismus gibt, wobei die Korrekturanordnung unter der Steuerung eines regelmäßig wiederholten Auffrischsignals aktivierbar ist, um einen korrigierbaren Fehler zu korrigieren.

19. Integrierte Schaltung mit einem Halbleiterspeicher nach einem der Ansprüche 1 bis 18.

Revendications

1. Mémoire à semi-conducteurs comprenant une matrice de mémoire (20) faite de rangées et de colonnes de cellules de mémoire pour stocker, par rangée, de l'information de données et de l'information redondante de protection contre les erreurs, la mémoire comprenant un dispositif de correction d'erreurs intégré qui est alimenté par des sorties de colonnes de la matrice de mémoire afin de recevoir un symbole pour chaque colonne à laquelle il y a eu accès, et des premiers moyens de sélection de colonnes (26) qui sont alimentés par ce dispositif de correction d'erreurs afin de présenter des signaux de sortie destinés à un usage ultérieur, caractérisée en ce que, dans la direction des rangées, la matrice de mémoire (20), comprend une succession d'au moins deux configurations de chacune tout au plus n colonnes, en ce que le dispositif de correction d'erreurs (24) est connecté aux sorties de colonnes suivant une configuration répétitive analogue pour opérer suivant un code de convolution spatiale (n, k), où (n > k), dans la mesure où, dans une configuration donnée, l'information redondante n'est affectée qu'au remplissage complet d'un nombre prédéterminé de (n-k) colonnes de la configuration en question afin de rendre chaque fois un symbole de données du code de convolution corrigible pour une longueur de contrainte quelconque du code, exprimée par le nombre de colonnes, avec un échange de bits de syndrome et de bits de syndrome subsidiaire entre des périodes de configuration voisines.

2. Mémoire à semi-conducteurs suivant la revendication 1, le dispositif de correction d'erreurs comprenant les quatre étages fonctionnels suivants pour chaque configuration complète :
   a. un étage d'entrée pour former un présyndrome (a_m) et au moins un symbole de syndrome subsidiaire (b_{m+1},c_{m+2},d_{m+3}) à partir de l'information reçue des cellules de mémoire;
   b. un deuxième étage pour recevoir au moins un symbole de syndrome subsidiaire (b_m,c_m,d_m) d'une configuration voisine dans une première direction, si elle est présente, et pour former un syndrome local (S_m) au moyen d'un présyndrome local et du au moins un symbole de syndrome subsidiaire;
   c. un étage de combinaison pour former, à partir du syndrome local et d'au moins un symbole de syndrome (S_{m+1},S_{m+2},S_{m+3}) d'une configuration voisine dans une seconde direction, si elle est présente, un signal de modification pour chaque signal d'information à appliquer aux premiers moyens de sélection de colonnes;
   d. un étage de modification pour modifier un signal d'information sous la commande d'un signal de modification respectif.

3. Mémoire à semi-conducteurs suivant la revendication 1 ou 2, caractérisée en ce que lesdites au moins deux configurations comportent des configurations de colonnes mutuellement identiques.

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4. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1, 2 ou 3, caractérisée en ce que le code de convolution spatiale est un code systématique du fait que dans chaque configuration, n-k colonnes sont dévolues exclusivement au stockage d'information redondante.

5. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 4, caractérisée en ce que chaque symbole est constitué d'un seul bit.

6. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 5, caractérisée en ce que le code de convolution est systématique au niveau du bit.

7. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 6, caractérisée en ce que le code de convolution n'est pas systématique au niveau du bit, les premiers moyens de sélection de colonnes étant associés à des moyens d'inversion de matrice.

8. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 7, caractérisée en ce que le code de convolution est un code (n,n-1).

9. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 8, caractérisée en ce que des seconds moyens de sélection de colonnes sont connectés entre la matrice de mémoire et le dispositif de correction d'erreurs.

10. Mémoire à semi-conducteurs suivant la revendication 9, caractérisée en ce que le facteur de sélection des seconds moyens de sélection de colonnes est plus petit que celui des premiers moyens de sélection de colonnes.

11. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 10, caractérisée en ce que la configuration comprend au moins $n=4$ colonnes afin d'appliquer, pour chaque configuration complète, (n-1) bits au premier moyen de sélection de colonnes, le second étage recevant des bits de syndrome subsidiaire (C_m) qui sont formés chacun d'au moins un bit de données d'une configuration directement voisine dans un premier sens, si elle est présente, l'étage de combinaison d'une configuration recevant des bits de syndrome de la configuration directement voisine dans un premier sens (S_m) et de deux configurations directement voisines dans le second sens (S_{m+1},S_{m+2}) si elles sont présentes.

12. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 11, caractérisée en ce que $n=2^j$, où $j \geq 3$.

13. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 12, caractérisée en ce que pour $n=2^j$, au moins une configuration finale incomplète est prévue à au moins une extrémité de la série de configurations, toutes les configurations finales incomplètes comprenant au moins les colonnes de redondance prévues pour chaque configuration complète afin de former à partir de celles-ci des bits de syndrome et/ou des bits de syndrome subsidiaire dans le dispositif de correction d'erreurs.

14. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 13, caractérisée en ce qu'à l'extrémité d'une série de configurations sont prévues des connexions pour un bouclage itératif vers l'autre extrémité respective de la série de bits de syndrome nécessaire et de bits de syndrome subsidiaire.

15. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 14, caractérisée en ce que les premiers moyens de sélection de colonnes sont bidirectionnellement actifs, un moyen formateur de bits de syndrome étant prévu pour chaque colonne redondante et une sortie de ce moyen pouvant être connectée à une entrée de colonne de la colonne redondante afin de stocker un bit de redondance restauré à l'aide d'information reçue de l'environnement et de l'information restant dans la matrice de mémoire.

16. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 15, caractérisée en ce qu'un étage de modification connecté aux premiers moyens de sélection de colonnes ignore une correction possible sous la commande d'un signal d'omission de correction.

17. Mémoire à semi-conducteurs suivant l'une quelconque des revendications 11 à 16, caractérisée en ce qu'il est prévu un mécanisme de substitution pour adresser de manière continue une rangée de substitution de cellules de mémoire en lieu et place d'une rangée défectueuse de cellules de mémoire.

18. Mémoire à semi-conducteurs suivant la revendication 15, caractérisée en ce qu'un mécani-

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sme de régénération est prévu, le dispositif de correction pouvant être activé sous la commande d'un signal de régénération récurrent afin de corriger une erreur corrigible.

19. Circuit intégré comprenant une mémoire à semi-conducteurs suivant l'une quelconque des revendications 1 à 18.