[Fig. 1A]

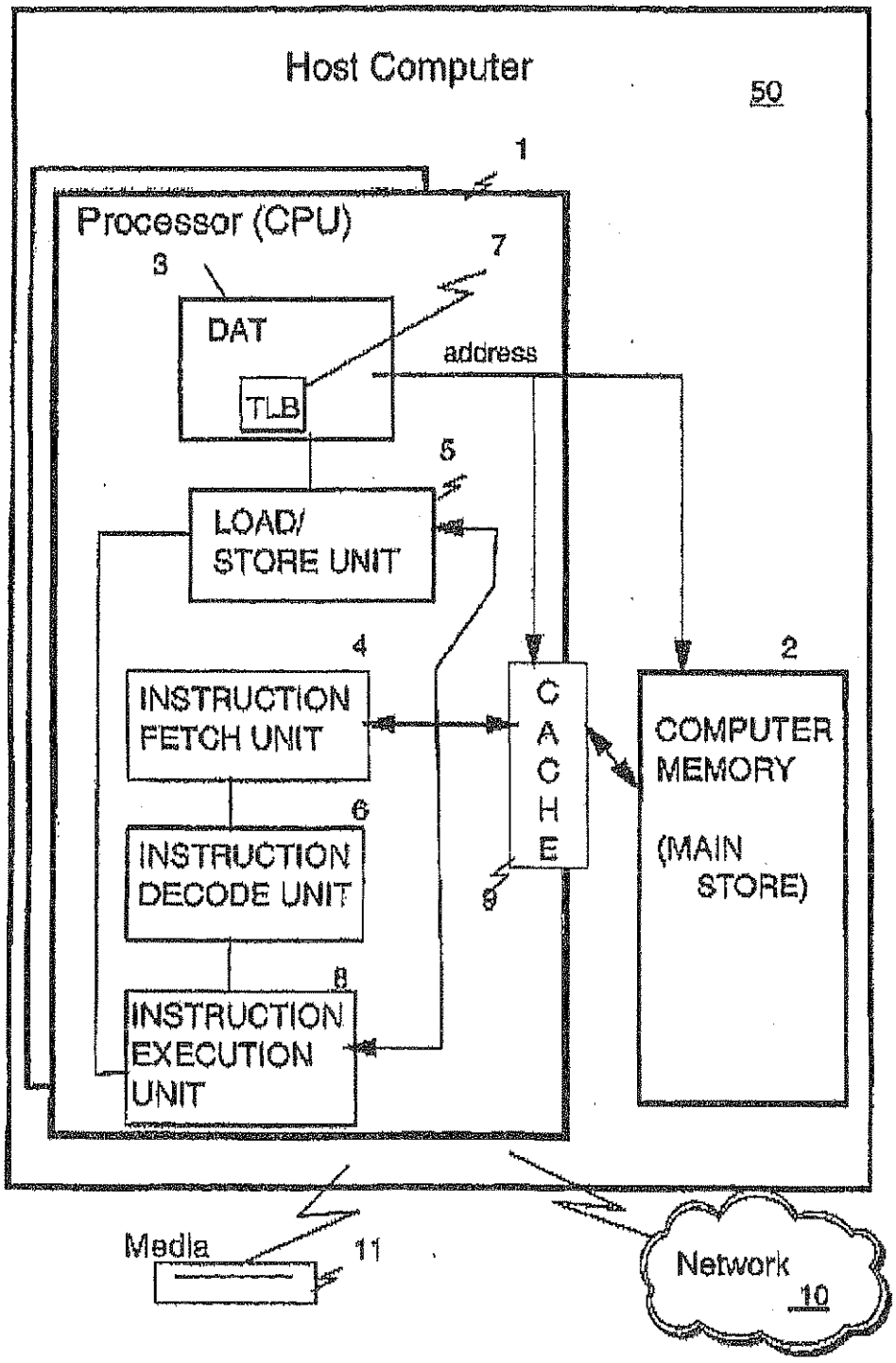
Host Computer
50
1
Processor (CPU)
3
7
DAT
address
TLB
5
LOAD/
STORE UNIT
4
2
INSTRUCTION
FETCH UNIT
C
A
C
H
E
COMPUTER
MEMORY
(MAIN
STORE)
6
INSTRUCTION
DECODE UNIT
9
8
INSTRUCTION
EXECUTION
UNIT
Media
11
Network
10

FIG. 1A

[Fig. 1B]

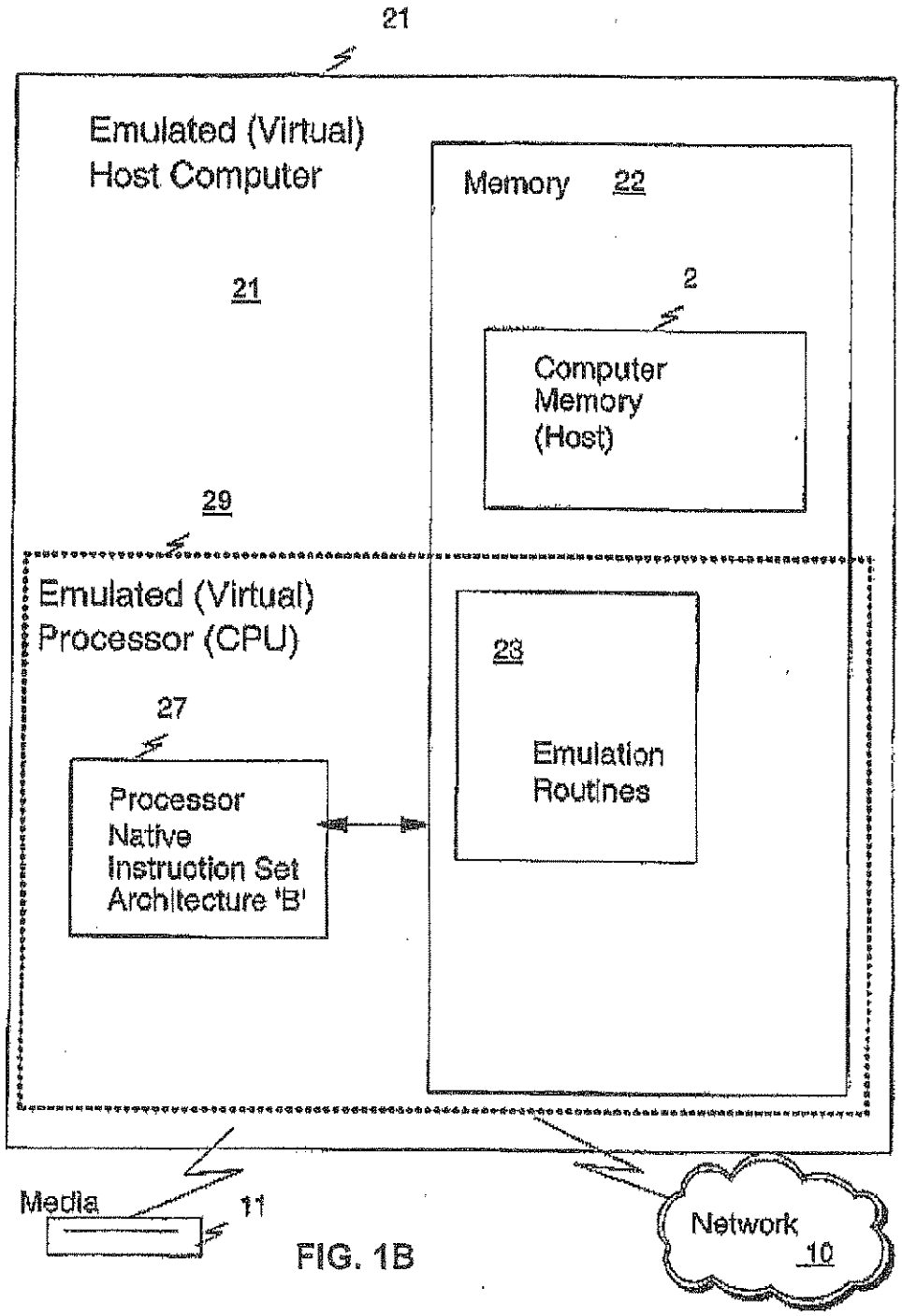
21
Emulated (Virtual)
Host Computer
Memory 22
21
2
Computer
Memory
(Host)
29
Emulated (Virtual)
Processor (CPU)
23
Emulation
Routines
27
Processor
Native
Instruction Set
Architecture 'B'
Media
11
Network
10

FIG. 1B

[Fig. 1C]

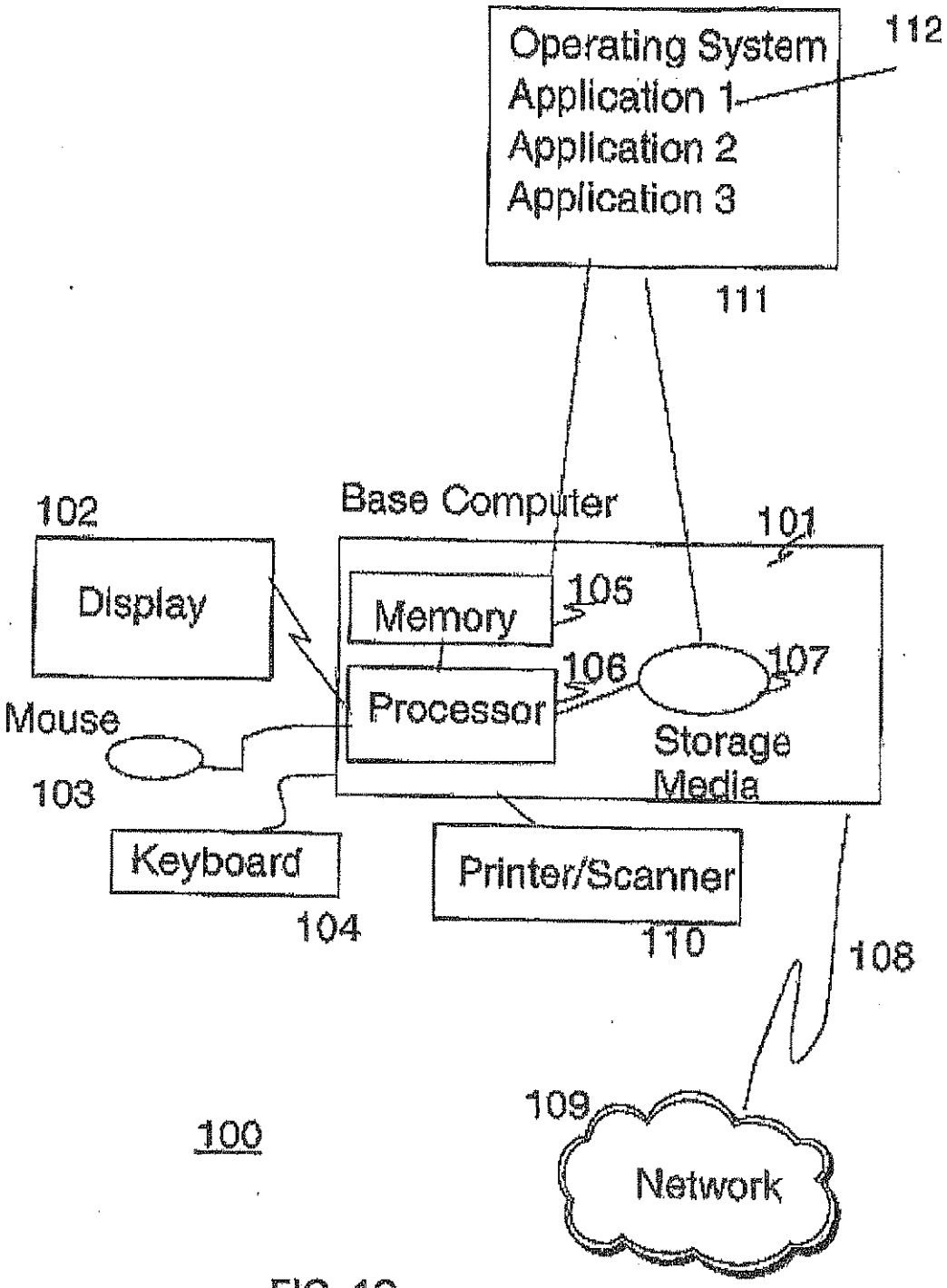
Operating System
Application 1
Application 2
Application 3
112
111
Base Computer
101
102
Display
Memory
105
106
107
Processor
Mouse
103
Storage Media
Keyboard
104
Printer/Scanner
110
108
109
Network
100

FIG. 1C

[Fig. 2]

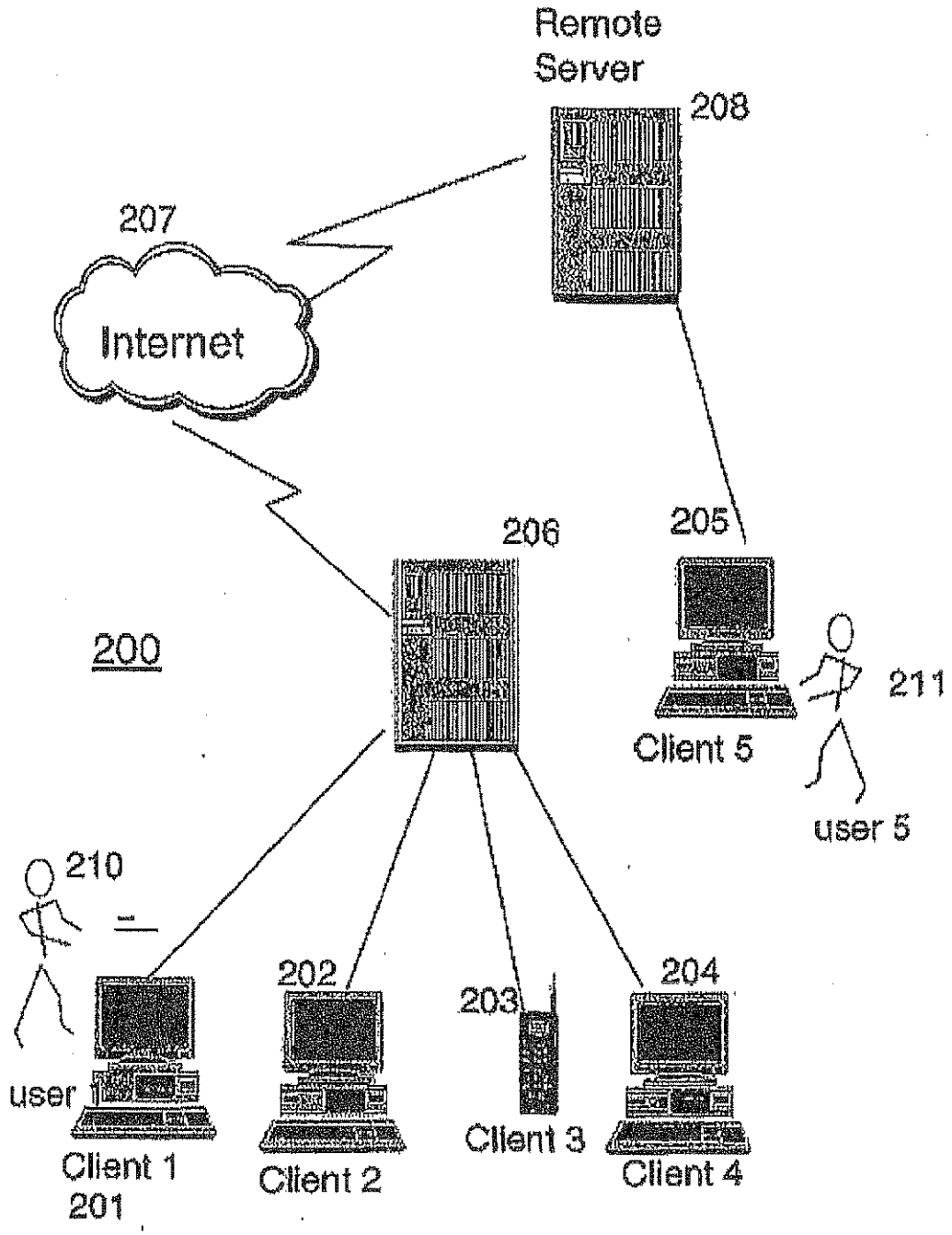
Remote
Server
208
207
Internet
206
205
200
211
Client 5
user 5
210
202
203
204
user 1
Client 1
201
Client 2
Client 3
Client 4

FIG. 2

[Fig. 3]

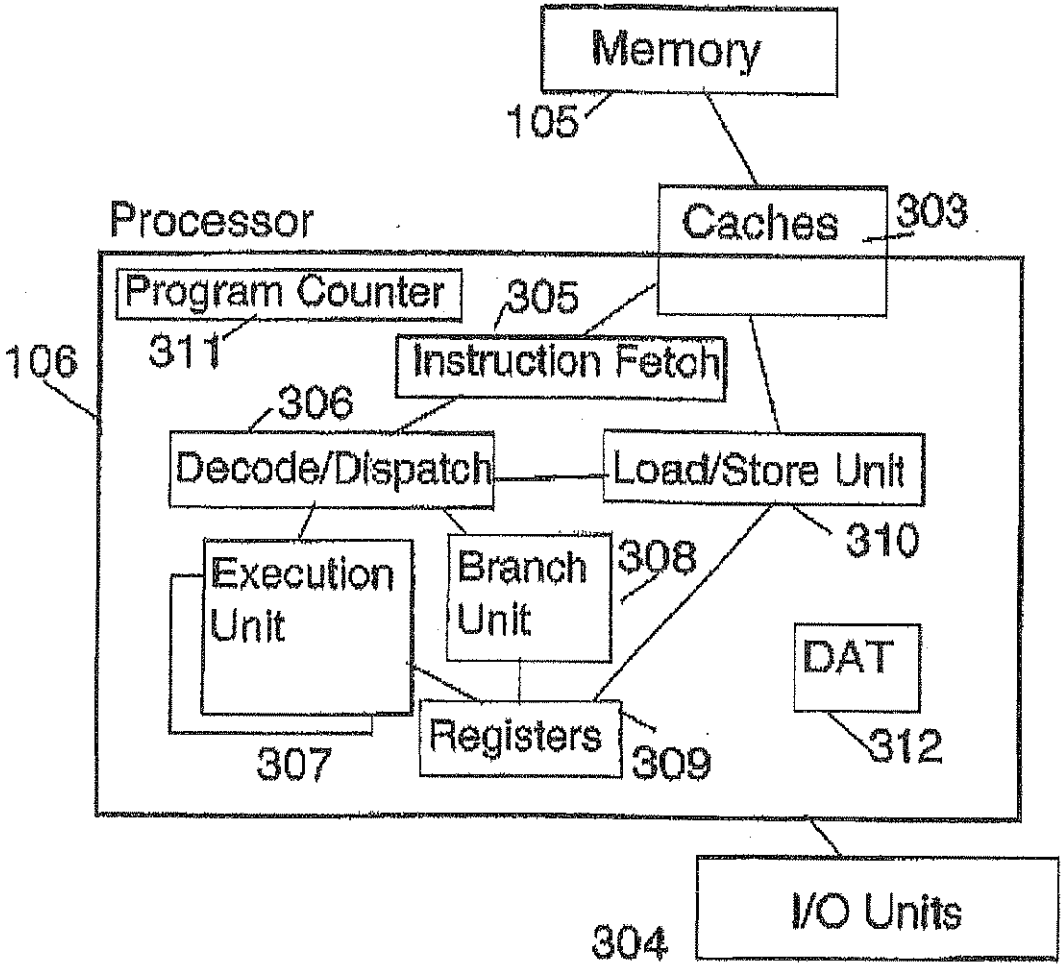
Memory
105
Caches
303
Processor
Program Counter
311
305
Instruction Fetch
106
306
Decode/Dispatch
Load/Store Unit
310
Execution Unit
Branch Unit
308
DAT
312
Registers
309
307
I/O Units
304

FIG. 3

[Fig. 4A]

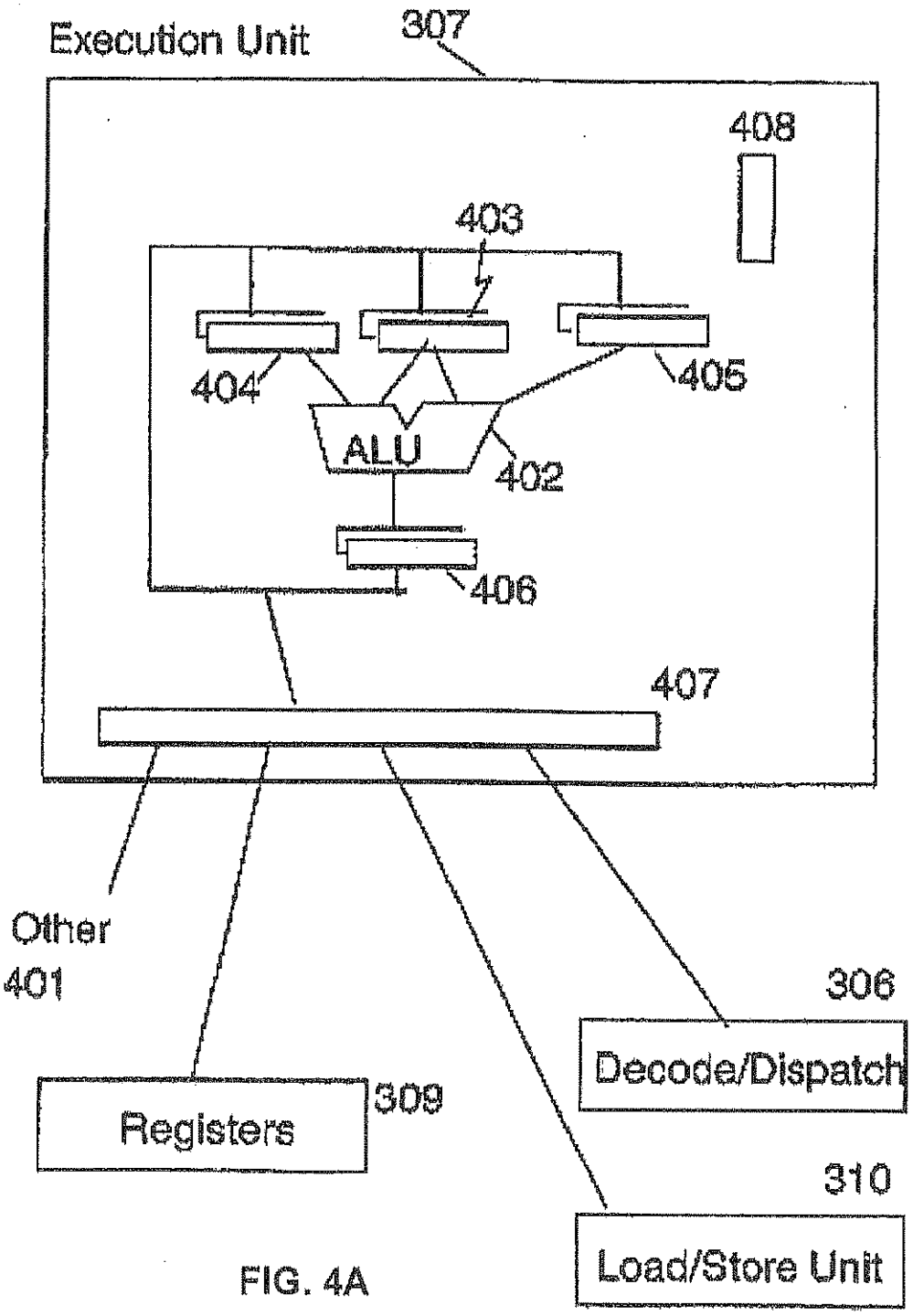
Execution Unit
307
408
403
404
405
ALU
402
406
407
Other
401
306
Decode/Dispatch
Registers
309
310
Load/Store Unit

FIG. 4A

[Fig. 4B]

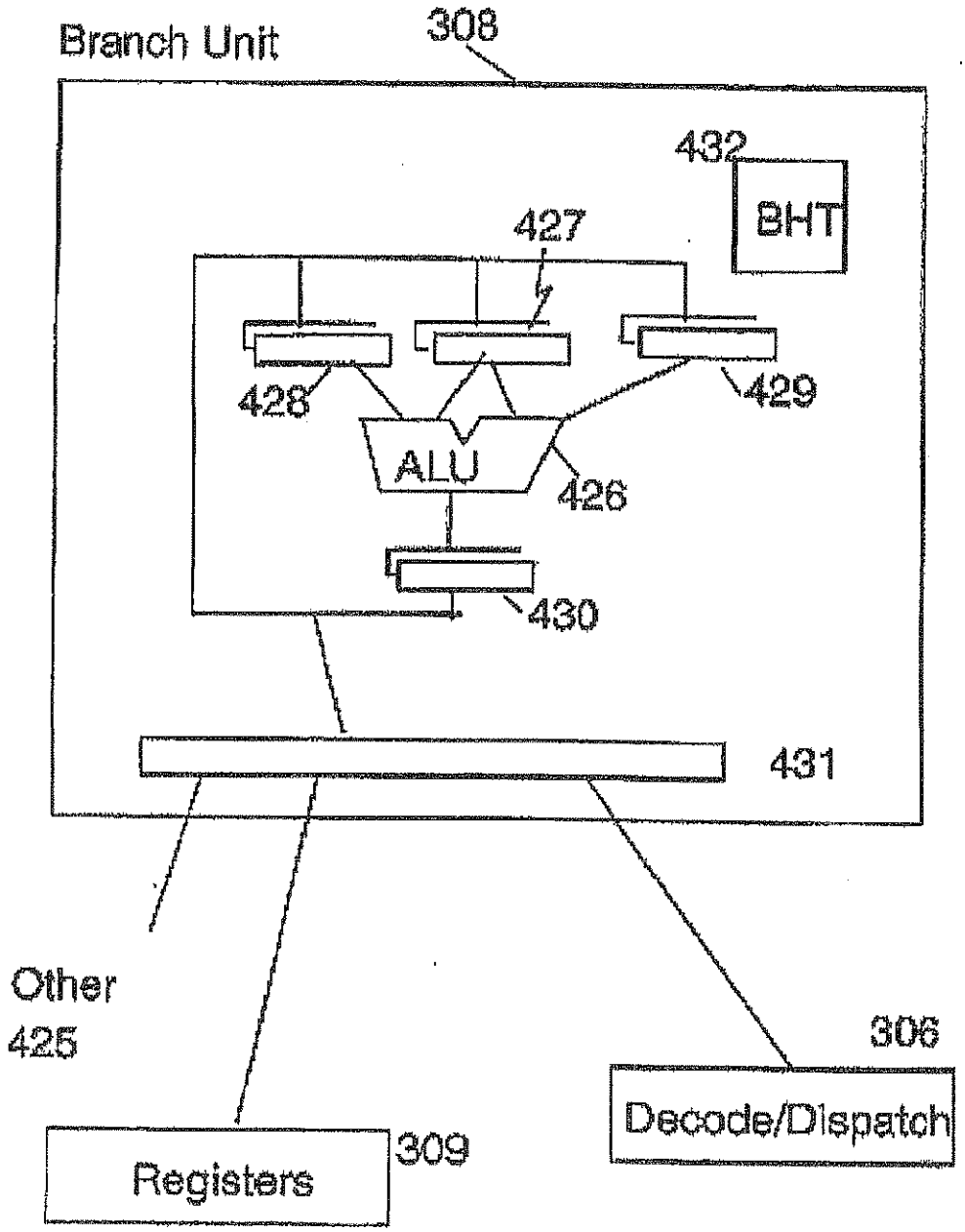
Branch Unit
308
432
BHT
427
428
429
ALU
426
430
431
Other
425
306
Decode/Dispatch
309
Registers

FIG. 4B

[Fig. 4C]

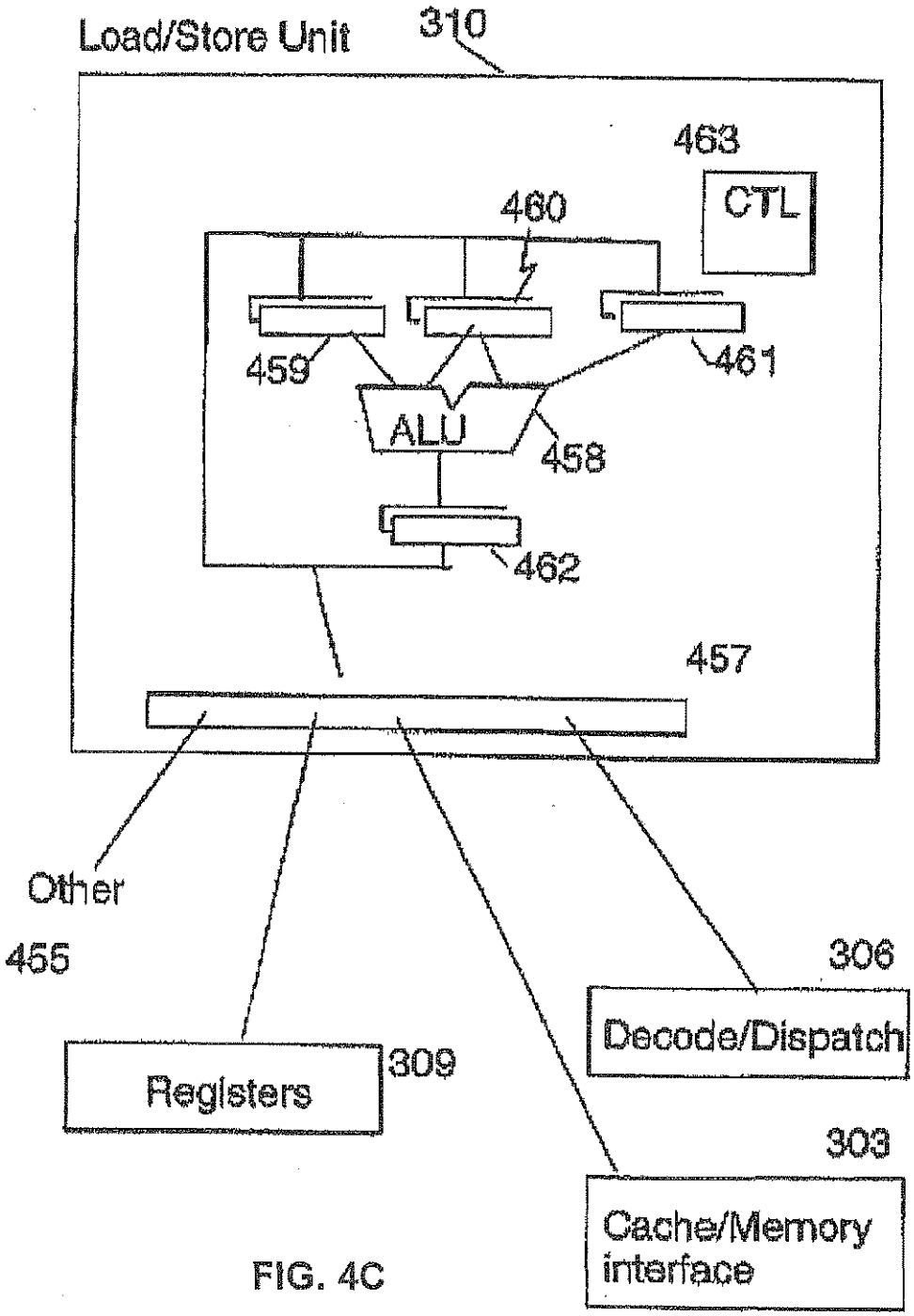
Load/Store Unit
310
463
CTL
460
459
461
ALU
458
462
457
Other
455
306
Decode/Dispatch
309
Registers
303
Cache/Memory interface

FIG. 4C

[Fig. 5]

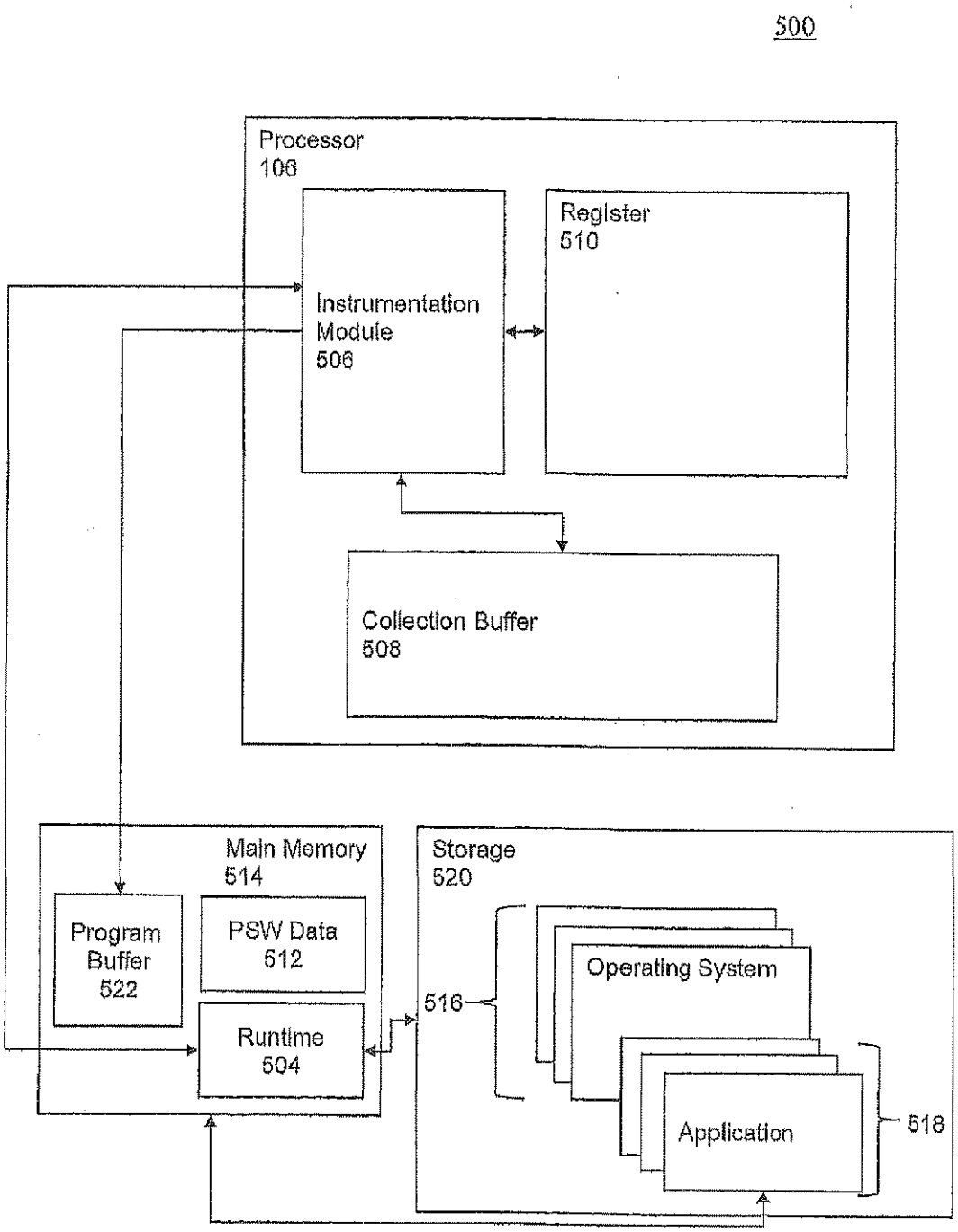
500
Processor
106
Instrumentation
Module
506
Register
510
Collection Buffer
508
Main Memory
514
Program
Buffer
522
PSW Data
512
Runtime
504
Storage
520
516
Operating System
Application
518

FIG. 5

[Fig. 6]

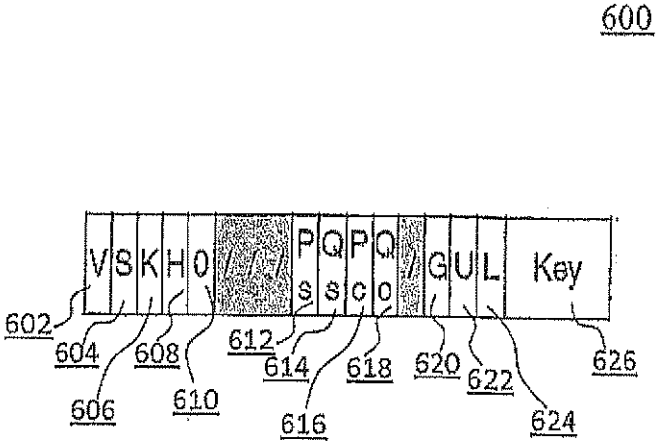
600
V
S
K
H
O
P
s
Q
s
P
c
Q
o
G
U
L
Key
602
604
606
608
610
612
614
616
618
620
622
624
626

FIG. 6

[Fig. 7]

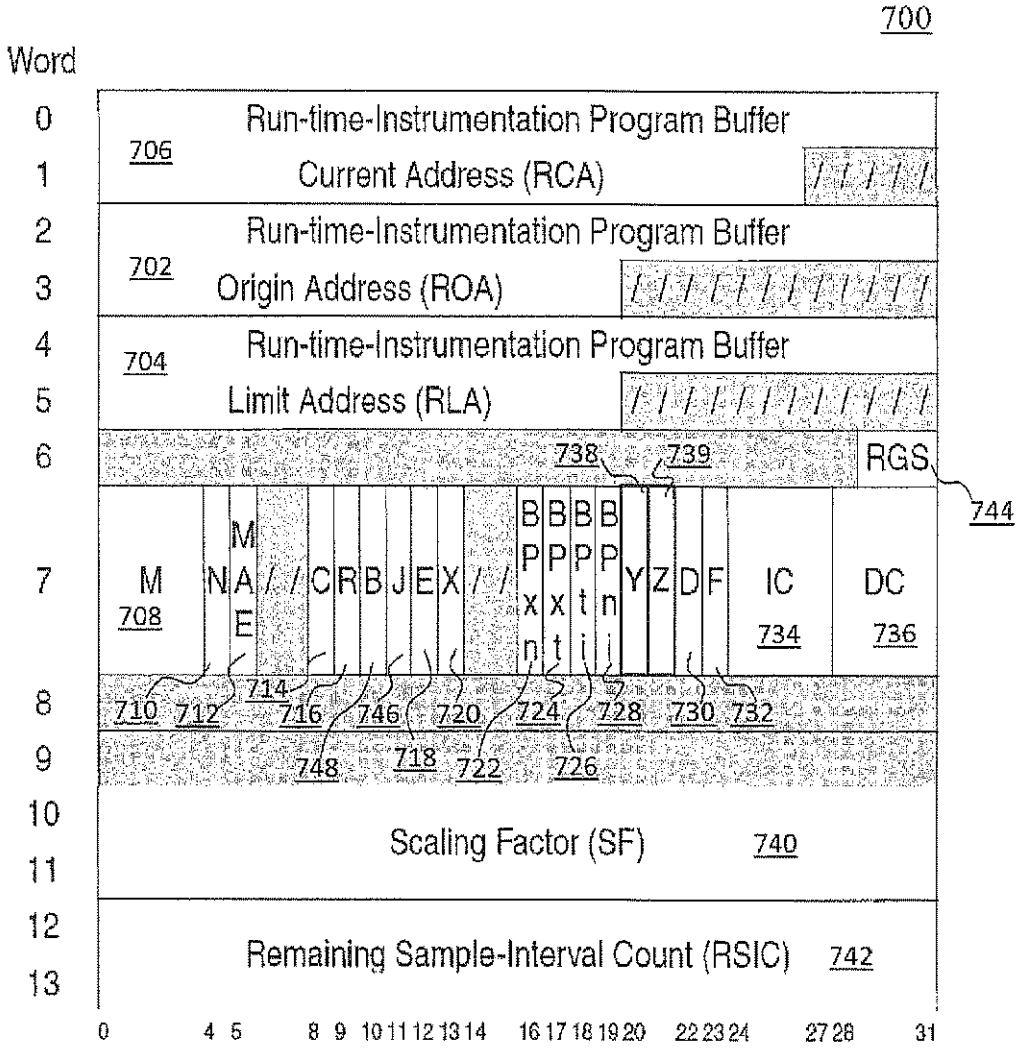
700
Word
0
1
2
3
4
5
6
7
8
9
10
11
12
13
Run-time-Instrumentation Program Buffer
706
Current Address (RCA)
Run-time-Instrumentation Program Buffer
702
Origin Address (ROA)
Run-time-Instrumentation Program Buffer
704
Limit Address (RLA)
738
739
RGS
744
M
708
NA
ME
C
R
B
J
E
X
BPxn
BPxt
BPti
BPni
Y
Z
D
F
IC
734
DC
736
710
712
714
716
746
720
724
728
730
732
748
718
722
726
Scaling Factor (SF)
740
Remaining Sample-Interval Count (RSIC)
742
0 4 5 8 9 10 11 12 13 14 16 17 18 19 20 22 23 24 27 28 31

FIG. 7

[Fig. 8]

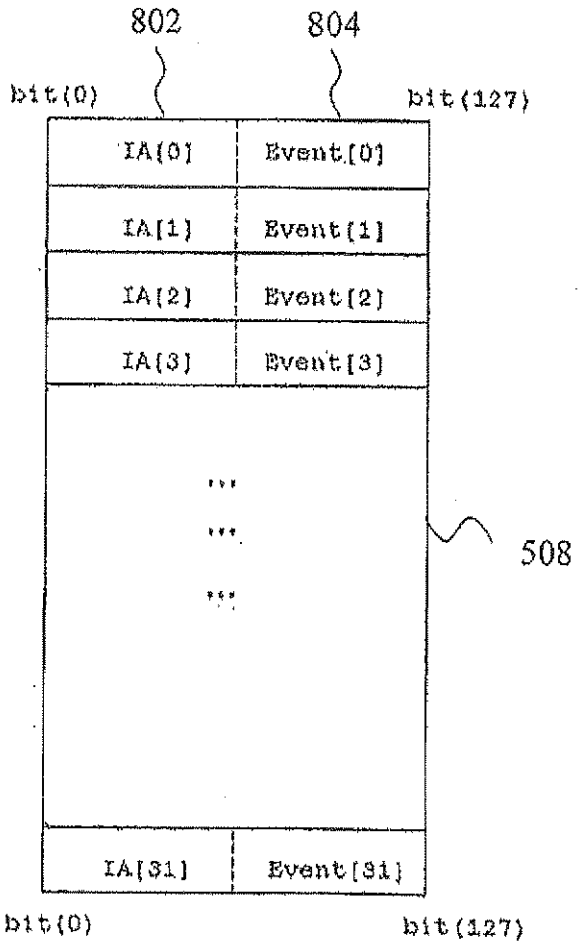
802
804
bit(0)
bit(127)
IA[0]
Event[0]
IA[1]
Event[1]
IA[2]
Event[2]
IA[3]
Event[3]
508
IA[31]
Event[31]
bit(0)
bit(127)

FIG. 8

[Fig. 9]

900

Record No.	Record Type(s)	Section
0	Begin, Timestamp	Header 902
1	Emit, TX Abort, Call, Return, Branch, Filler	Body 904
2		
3		
R_{RG}-R_{NC} (=4)		
R_{RG}-R_{NC}+1 (=5)	Extra, Model-Dependent	Extra 906
R_{RG}-2 (=6)		
R_{RG}-1	Instruction	Footer 908

FIG. 9

[Fig. 10]

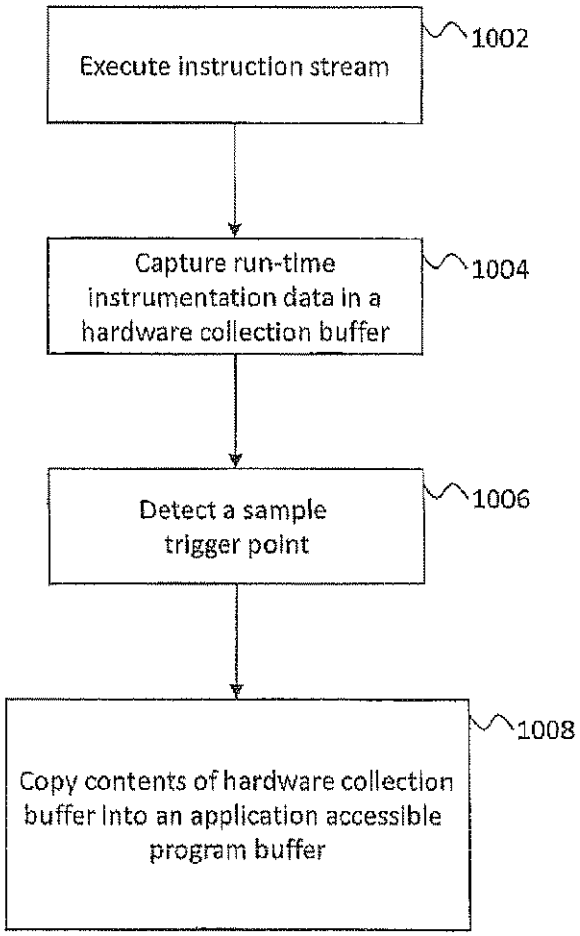
Execute instruction stream
1002
Capture run-time instrumentation data in a hardware collection buffer
1004
Detect a sample trigger point
1006
Copy contents of hardware collection buffer into an application accessible program buffer
1008

FIG. 10

[Fig. 11]

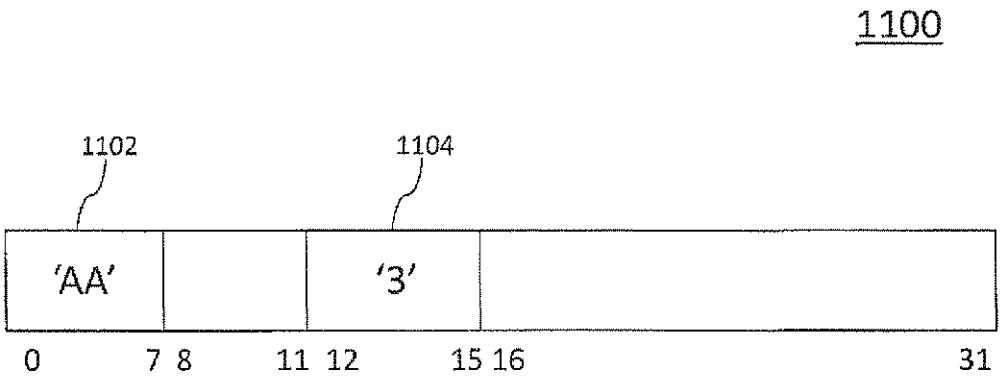

FIG. 11

[Fig. 12]

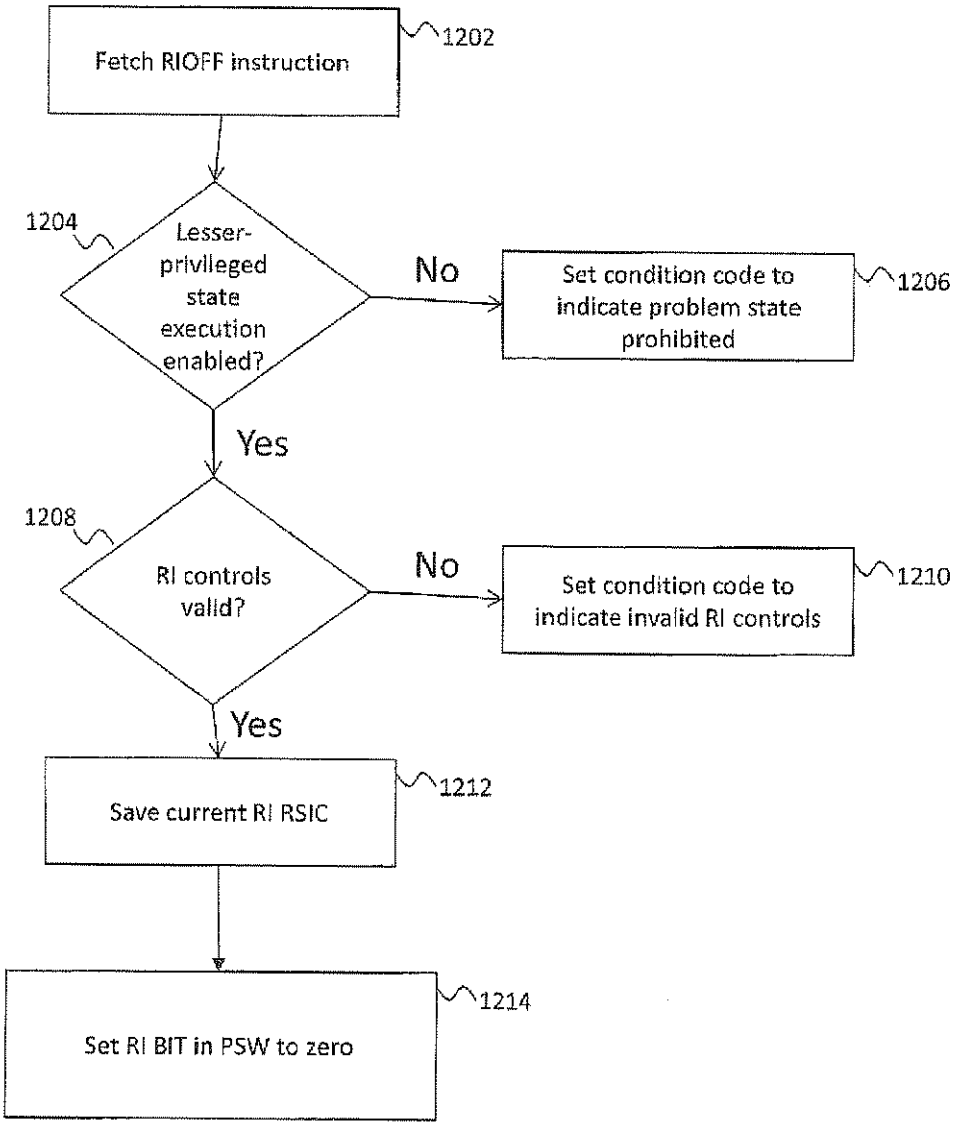
Fetch RIOFF instruction
1202
1204
Lesser-privileged state execution enabled?
No
Set condition code to indicate problem state prohibited
1206
Yes
1208
RI controls valid?
No
Set condition code to indicate invalid RI controls
1210
Yes
Save current RI RSIC
1212
Set RI BIT in PSW to zero
1214

FIG. 12

[Fig. 13]

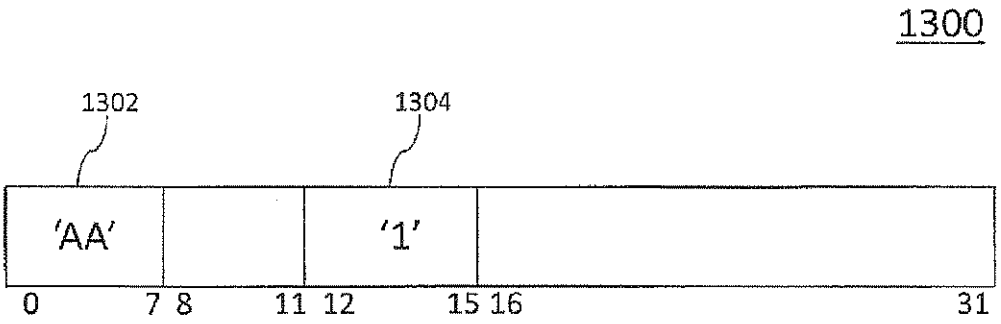

FIG. 13

[Fig. 14]

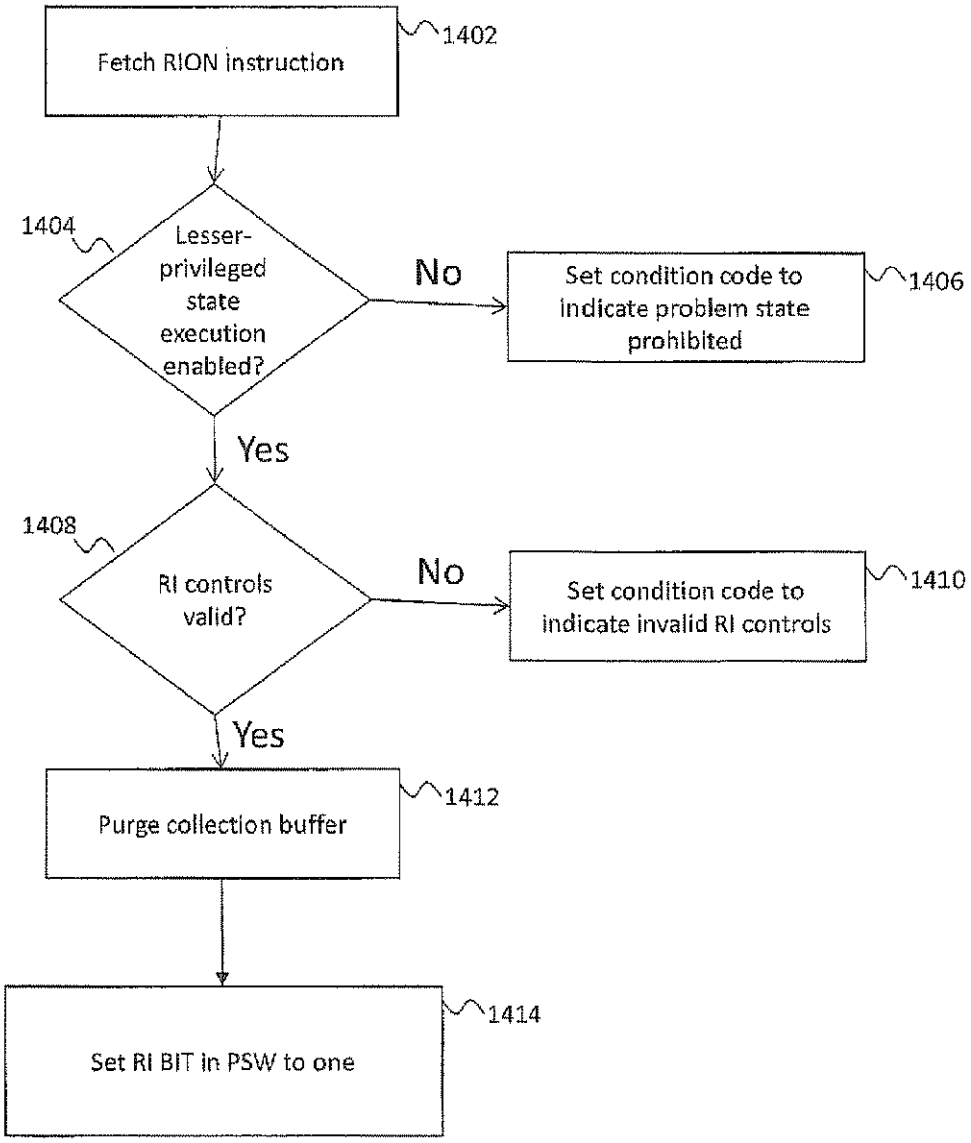
Fetch RION instruction
1402
1404
Lesser-privileged state execution enabled?
No
Set condition code to indicate problem state prohibited
1406
Yes
1408
RI controls valid?
No
Set condition code to indicate invalid RI controls
1410
Yes
Purge collection buffer
1412
Set RI BIT in PSW to one
1414

FIG. 14

[Fig. 15]

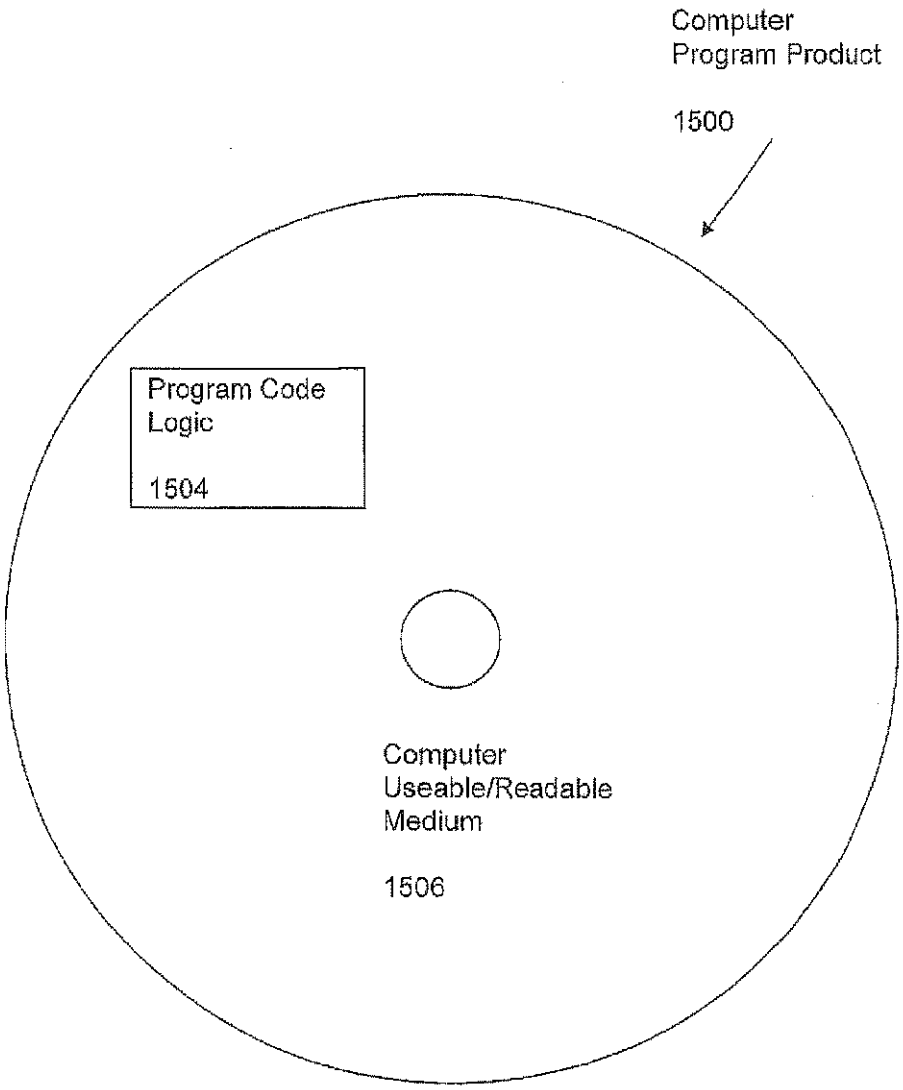
Computer
Program Product
1500
Program Code
Logic
1504
Computer
Useable/Readable
Medium
1506

FIG. 15