

PATENT SPECIFICATION (11)

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(54) IMPROVEMENTS IN OR RELATING TO CIRCUIT ARRANGEMENTS FOR PAL COLOUR TELEVISION RECEIVERS

(71) We, EMI LIMITED, a British company of Blyth Road, Hayes, Middlesex, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to circuit arrangements for PAL colour television receivers, and it relates more especially to such arrangements for ensuring that the (R-Y) component of the received chrominance signals is demodulated correctly.

The invention is applicable to PAL colour television receivers generally, whether they employ a transit time signal splitting circuit or not, and also to the kind of receiver which converts the received PAL waveform into a pseudo N.T.S.C. waveform by rejecting alternate lines of chrominance information.

According to the invention there is provided a circuit arrangement for a colour television receiver adapted to receive television information encoded in accordance with the PAL system, including a source of demodulating oscillations, gating means for applying colour synchronising signals of a selected phase to said source to synchronise the phase of said oscillations and control means for tending to prevent the application to said source of colour synchronising signals of phase different from the selected phase, the control means comprising a counting circuit for determining the interval between the last colour synchronising signal applied to said source in one field and the first colour synchronising signal applied to said source in the next succeeding field, and means for disturbing the operation of said gating means in the event that said interval is of incorrect duration.

In order that the invention may be clearly understood and readily carried into effect, one embodiment thereof will now be described by way of example only with refer-

ence to the drawings accompanying the Provisional Specification of which:—

Figure 1 shows, in block diagrammatic form, a circuit arrangement in accordance with one example of the invention,

Figure 2(a) shows the phase construction of the chrominance signals transmitted on one set of alternate lines of a television transmission and the phase of the colour synchronising signal which precedes it,

Figure 2(b) shows information similar to that shown in Figure 2(a) but relating to the chrominance signals transmitted on the intervening set of alternate lines, and

Figure 3 illustrates graphically the operation of the embodiment shown in Figure 1.

Referring now to the drawings, Figure 1 shows a circuit arrangement according to the invention as applied to a "simple-PAL" receiver, i.e. one which does not utilise a transit time signal splitting circuit. As pointed out previously, however, the invention is not limited to such an embodiment.

The full received chrominance signal is applied to terminal 1 and thence, in parallel to a pair of synchronous demodulators 2 and 3. A burst gate 4 is coupled to terminal 1 and is enabled to pass only alternate colour synchronising signals; the colour synchronising signals being commonly referred to as colour bursts. The enabling of gate 4 is achieved by pulses 5, derived from the line flyback pulses, generated in the receiver, after they have been divided by two by means of a bistable circuit 6. The arrangement in this respect is such that each of the pulses 5 causes the bistable circuit 6 to change its state, the circuit being such as to enable the gate 4 only for the duration of each of the pulses 5 which causes it to assume its set or '1' condition.

It is well known that, in the PAL colour television system, the phase of the colour bursts transmitted with successive lines of chrominance information changes through 90° so as to be indicative of the phase of

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the colour sub-carrier frequency signal which bears the (R-Y) information. This is shown in Figures 2(a) and 2(b) where the burst phases are indicated respectively by the vectors SA and SB. In both Figures 2(a) and 2(b) the phase of the sub-carrier frequency oscillations which bear the (B-Y) information is denoted by the vector B, whereas the phase of the sub-carrier frequency oscillation which bears the (R-Y) information is denoted by the vector RA in Figure 2(a) and RB in Figure 2(b).

It will now be appreciated that because the gate 4 only passes alternate colour bursts, the bursts so passed will all be of one phase, and in this example it is assumed that the bursts SA are passed by the gate 4, the bursts SB being rejected thereby. The bursts SA are applied, via a -45° phase shifting arrangement 4a to synchronise the phase of operation of a local oscillator 7 which generates oscillations of the colour sub-carrier frequency. Oscillator 7, which may be either an active or a passive oscillator, is assumed to be of the kind which locks to a phase 90° displaced from that of the synchronising oscillations applied thereto, and thus produces oscillations of the phase of the vector B. These oscillations are suitable for demodulating the (B-Y) information and are thus applied directly to the demodulator 2. The oscillations from oscillator 7 are also passed through a $+90^\circ$ phase shifter 7a and a -90° phase shifter 7b to produce oscillations of the phases of the vectors RA and RB respectively. These oscillations are applied to respective contacts of a switch 8, known as the PAL switch, the pole of which is connected to the (R-Y) demodulator 3. The PAL switch is caused to change its condition between each pair or lines of received information by a pair of connections from the bistable circuit 6, the arrangement being such that when the circuit 6 assumes its set, or '1' condition the arm of switch 8 is moved to the left and when the circuit 6 assumes its reset, or '0' condition the arm of switch 8 is moved to the right.

By this means it will be observed that when bursts of the phase of vector SA are passed via gate 4, meaning of course that the (R-Y) component of the chrominance information transmitted on that line will be modulated on a sub-carrier frequency signal of phase RA, the switch 8 is controlled to feed the oscillations of phase RA derived from phase shifter 7a to the (R-Y) demodulator 3. Furthermore when, on the subsequent line, the bistable circuit is driven to its reset condition, the burst of the phase of the vector SB is not passed through gate 4 but the switch 8 changes so as to apply the oscillations of the phase of the vector RB, derived from phase shifter 7b, to the

demodulator 3. These oscillations are of the correct phase for demodulating the R-Y component of the chrominance signal transmitted on that line, which component is modulated on a sub-carrier frequency oscillation of the phase of the vector RB.

However, as thus far described, the burst gate may be enabled to pass the colour bursts of the phase of the vector SB, which would cause the oscillator 7 to produce oscillations of the incorrect phase. The possibility of this happening must therefore be prevented, and this is achieved by means of the circuit shown within the dashed outline 9, which takes advantage of the following features of the PAL waveform as transmitted:

- (i) the last colour burst in every field has the phase of the vector SA,
- (ii) the first colour burst in every field has the phase of the vector SA, and
- (iii) between each pair of successive fields there is an interval of nine lines duration which no colour bursts are transmitted. This is the so-called burst blanking interval.

The circuit within outline 9 includes a circuit 10 connected to receive the output signals from gate 4 and to produce an enabling signal for an 'AND' gate 11 when no signal is present at the output of gate 4. The other input to gate 11 comprises the half line frequency pulses, derived from circuit 6, which are used to enable the burst gate 4. The output of gate 11 is applied to a counter 12 which, in this example comprises a six-position register. Thus each time gate 4 is opened, but passes no colour burst signal, a pulse is applied to the register 12 to step the 'ON' state of the register one place to the left.

Because of this arrangement and the three features mentioned above, if the colour bursts having the phase of the vector SA are being passed by gate 4 during one field, then during the burst blanking interval between that field and the next, the register 12 will receive four pulses via gate 11. If, however, the colour bursts having the phase of the vector SB are being passed by gate 4 during one field, then during the burst blanking interval between that field and the next, the register 12 will receive five pulses via gate 11. This latter condition is the one it is desired to prevent and so the arrangement is such that when the 'ON' state of register 12 has moved into the position which indicates a count of five, the bistable circuit 6 is held in its '1' condition, thereby enabling the colour bursts of the phase of the vector SA to be selected for the following field. The holding of bistable circuit 6 in its '1' condition is achieved by means of a connection 13 between register 12 and bistable circuit 6. The register 12 is reset

to '0' when the gate 4 passes a colour burst signal, by means of a connection 14 from the circuit 10.

The operation of the circuit arrangement may be readily understood with reference to Figure 3, wherein each cell represents an interval in which a colour burst signal may be transmitted; the total period shown in Figure 3 covering the end of field n , the beginning of field $n+1$ and the burst blanking interval between these two fields.

It will be appreciated that the invention is not limited to the embodiment described above, for example the circuit arrangement within outline 9 may be replaced by an arrangement for detecting the presence or absence of other characteristic features occurring in the burst blanking interval.

It will be appreciated that the circuit enclosed within outline 9 may be inhibited for, say, nine burst blanking intervals out of every ten and thus be effective only during selected intervals.

WHAT WE CLAIM IS:—

1. A circuit arrangement for a colour television receiver adapted to receive television information encoded in accordance with the PAL system, including a source of demodulation oscillations, gating means for applying colour synchronising signals of a selected phase to said source to synchronise the phase of said oscillations, and control means for tending to prevent the application to said source of colour synchronising signals of phase different from the selected phase, the control means comprising a counting circuit for determining the interval between the last colour synchronising signal applied to said source in one field and the first colour synchronising signal applied to said source in the next succeeding field, and means for disturbing the operation of said gating means in the event that said interval is of incorrect duration.

2. An arrangement according to Claim 1 wherein said demodulating oscillations are

applied, appropriately phased, to respective demodulating circuits for the (B-Y) and (R-Y) components of said television information, the demodulating oscillations for the (R-Y) component being changed in phase through 180° from line to line by means including a switch device, adapted to change its condition at line frequency, which is synchronised in operation with said gating means.

3. An arrangement according to either of claims 1 or 2 wherein the said gating means is controlled under the influence of locally derived line frequency pulses.

4. An arrangement according to Claim 3 wherein said pulses are applied to a bistable circuit which is adapted to open said gating means, for the duration of a colour synchronising signal, when it assumes a given one of its stable conditions.

5. An arrangement according to Claim 4 wherein said control means includes an "AND" gate which is arranged to receive a pulse each time the bistable circuit assumes said given condition, the gate being disabled when colour synchronising signals are present and enabled in the absence of said colour synchronising signals.

6. An arrangement according to Claim 5 wherein said counting circuit comprises a six-stage binary shift register, means being provided for causing said bistable circuit to assume said given position in the event that the count in said register exceeds a predetermined value, and means for resetting the count to zero when a colour synchronising signal is passed by said gating means.

7. A circuit arrangement substantially as herein described with reference to the drawings filed with the Provisional Specification.

8. A PAL television receiver including a circuit arrangement according to any preceding claim.

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Chartered Patent Agent.



to '0' when the gate 4 passes a colour burst signal, by means of a connection 14 from the circuit 10.

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10 beginning of field $n+1$ and the burst blanking interval between these two fields.

It will be appreciated that the invention is not limited to the embodiment described above, for example the circuit arrangement
15 within outline 9 may be replaced by an arrangement for detecting the presence or absence of other characteristic features occurring in the burst blanking interval.

It will be appreciated that the circuit enclosed within outline 9 may be inhibited
20 for, say, nine burst blanking intervals out of every ten and thus be effective only during selected intervals.

25 WHAT WE CLAIM IS:—

1. A circuit arrangement for a colour television receiver adapted to receive television information encoded in accordance with the PAL system, including a source of
30 demodulation oscillations, gating means for applying colour synchronising signals of a selected phase to said source to synchronise the phase of said oscillations, and control means for tending to prevent the application
35 to said source of colour synchronising signals of phase different from the selected phase, the control means comprising a counting circuit for determining the interval between the last colour synchronising signal applied
40 to said source in one field and the first colour synchronising signal applied to said source in the next succeeding field, and means for disturbing the operation of said gating means in the event that said interval
45 is of incorrect duration.

2. An arrangement according to Claim 1 wherein said demodulating oscillations are

applied, appropriately phased, to respective demodulating circuits for the (B-Y) and (R-Y) components of said television information, the demodulating oscillations for the (R-Y) component being changed in
50 phase through 180° from line to line by means including a switch device, adapted to change its condition at line frequency, which
55 is synchronised in operation with said gating means.

3. An arrangement according to either of claims 1 or 2 wherein the said gating means is controlled under the influence of
60 locally derived line frequency pulses.

4. An arrangement according to Claim 3 wherein said pulses are applied to a bistable circuit which is adapted to open said
65 gating means, for the duration of a colour synchronising signal, when it assumes a given one of its stable conditions.

5. An arrangement according to Claim 4 wherein said control means includes an "AND" gate which is arranged to receive
70 a pulse each time the bistable circuit assumes said given condition, the gate being disabled when colour synchronising signals are present and enabled in the absence of said colour synchronising signals.
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6. An arrangement according to Claim 5 wherein said counting circuit comprises a six-stage binary shift register, means being
80 provided for causing said bistable circuit to assume said given position in the event that the count in said register exceeds a predetermined value, and means for resetting the count to zero when a colour synchronising signal is passed by said gating means.

7. A circuit arrangement substantially
85 as herein described with reference to the drawings filed with the Provisional Specification.

8. A PAL television receiver including a circuit arrangement according to any
90 preceding claim.

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