

A NOVEL EMBEDDED POLYSILICON GATE MOSFET

ABSTRACT

Formation of a MOSFET with a polysilicon gate electrode embedded within a silicon trench is described. The MOSFET retains all the features of conventional MOSFETs with photolithographically patterned polysilicon gate electrodes, including robust LDD (lightly doped drain) regions formed in along the walls of the trench. Because the gate dielectric is never exposed to plasma etching or aqueous chemical etching, gate dielectric films of under 100 Angstroms may be formed without defects. The problems of over etching, and substrate spiking which are encountered in the manufacture of photolithographically patterned polysilicon gate electrodes do not occur. The entire process utilizes only two photolithographic steps. The first step defines the silicon active area by patterning a field isolation and the second defines a trench within the active area wherein the device is formed. The new process, uses the same total number of photolithographic steps to form the MOSFET device elements as a conventional process but is far more protective of the thin gate oxide.

FIGURE 7 IS SUGGESTED FOR PUBLICATION