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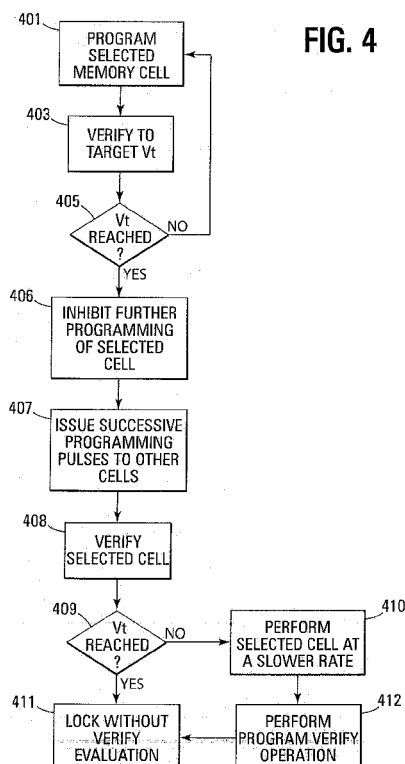
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(54) Title: CHARGE LOSS COMPENSATION DURING PROGRAMMING OF A MEMORY DEVICE



(57) Abstract: A selected memory cell on a selected word line is programmed through a plurality of programming pulses that are incremented by a step voltage. After a successful program verify operation, programming of the selected memory cell is inhibited while other memory cells of the selected word line are being programmed. Another program verify operation is performed on the selected memory cell. If the program verify operation fails, a bit line coupled to the selected cell is biased at the step voltage and a final programming pulse is issued to the selected word line. The selected memory cell is then locked from further programming without evaluating the final program verify operation.



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