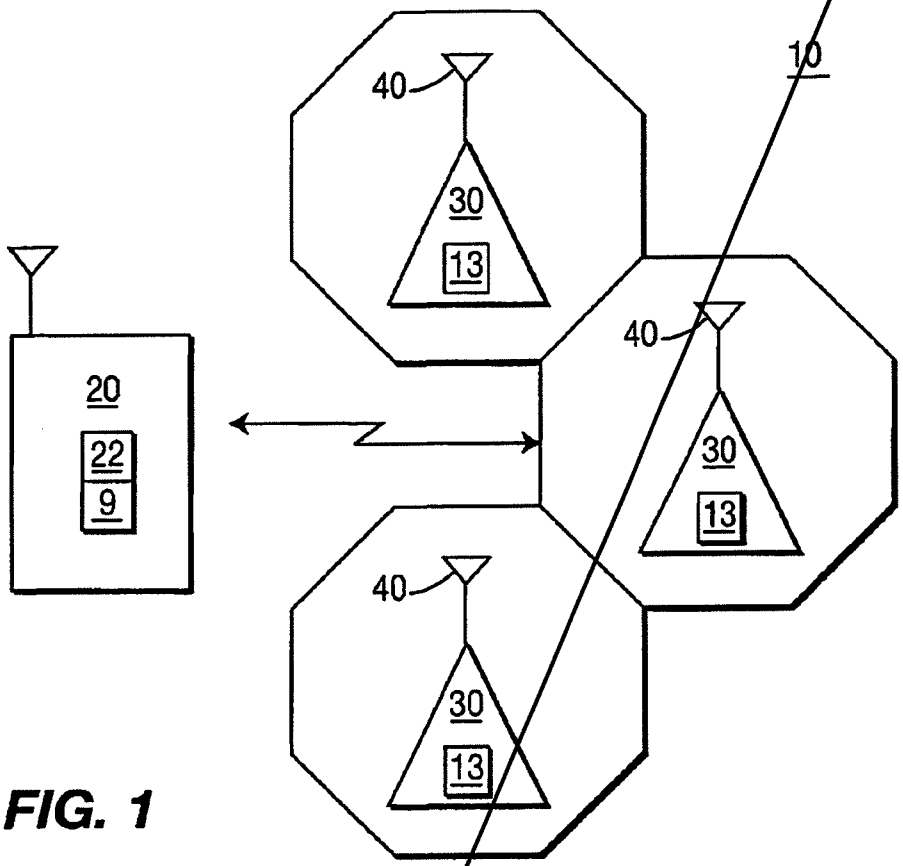
10
40
30
13
40
30
13
40
30
13
20
22
9

FIG. 1

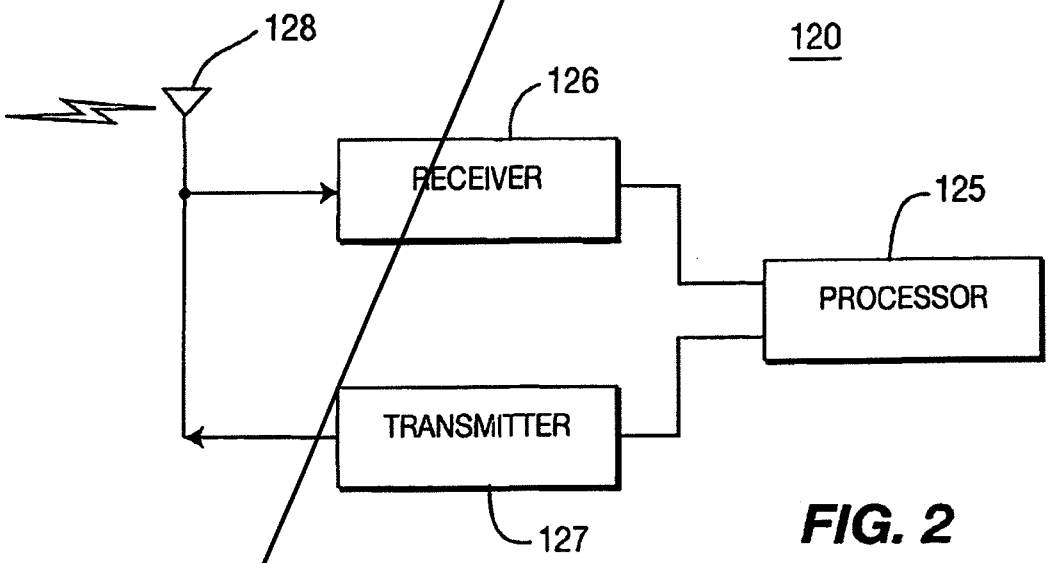
128
120
126
RECEIVER
125
PROCESSOR
TRANSMITTER
127

FIG. 2

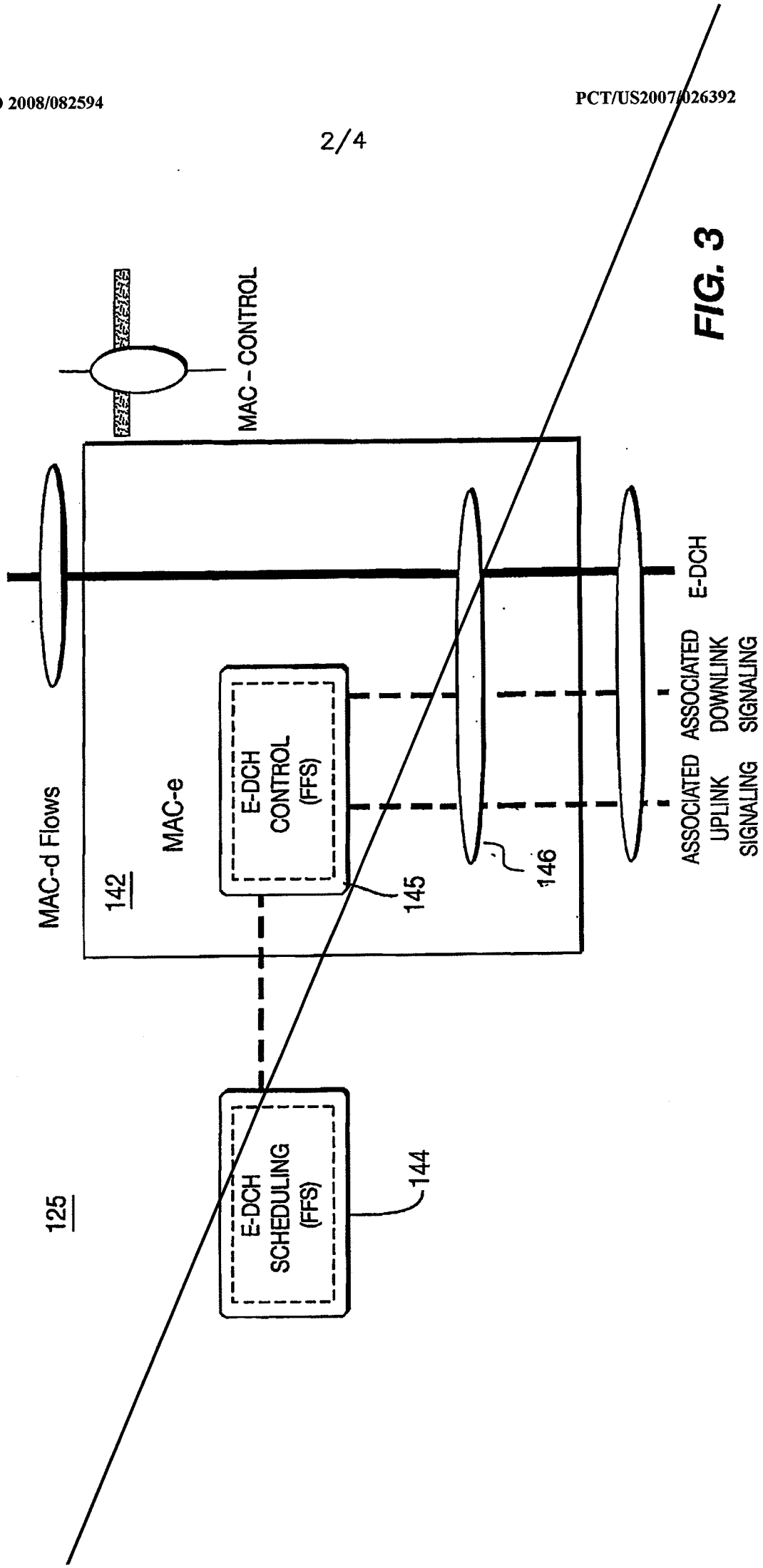
MAC-CONTROL
MAC-d Flows
142
MAC-e
E-DCH CONTROL (FFS)
145
146
E-DCH
ASSOCIATED UPLINK SIGNALING
ASSOCIATED DOWNLINK SIGNALING
125
E-DCH SCHEDULING (FFS)
144

FIG. 3

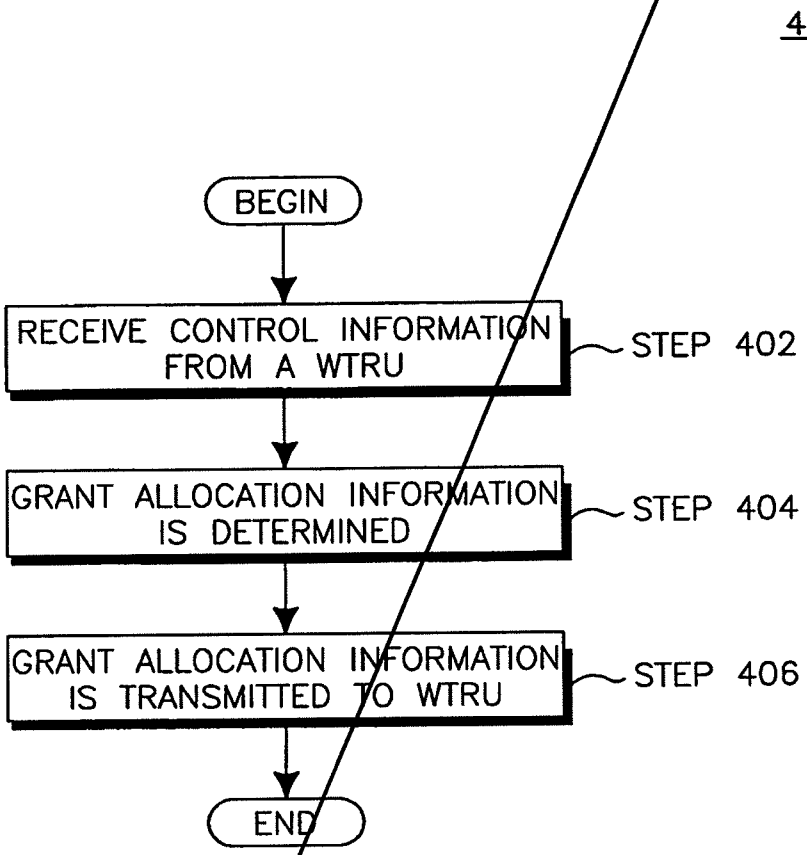
400
BEGIN
RECEIVE CONTROL INFORMATION FROM A WTRU
STEP 402
GRANT ALLOCATION INFORMATION IS DETERMINED
STEP 404
GRANT ALLOCATION INFORMATION IS TRANSMITTED TO WTRU
STEP 406
END

FIG. 4

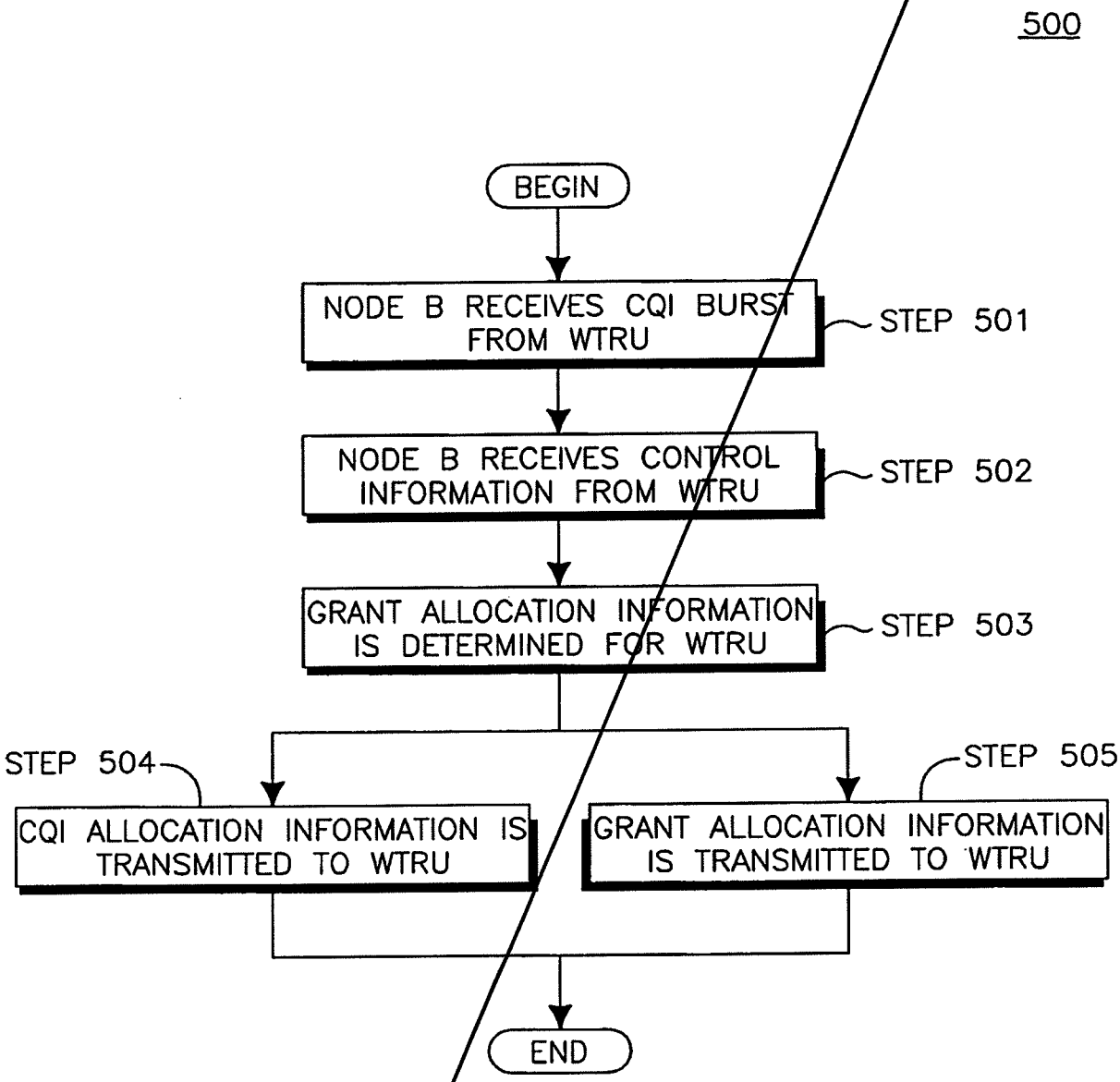
500
BEGIN
NODE B RECEIVES CQI BURST FROM WTRU
STEP 501
NODE B RECEIVES CONTROL INFORMATION FROM WTRU
STEP 502
GRANT ALLOCATION INFORMATION IS DETERMINED FOR WTRU
STEP 503
STEP 504
CQI ALLOCATION INFORMATION IS TRANSMITTED TO WTRU
STEP 505
GRANT ALLOCATION INFORMATION IS TRANSMITTED TO WTRU
END

FIG. 5

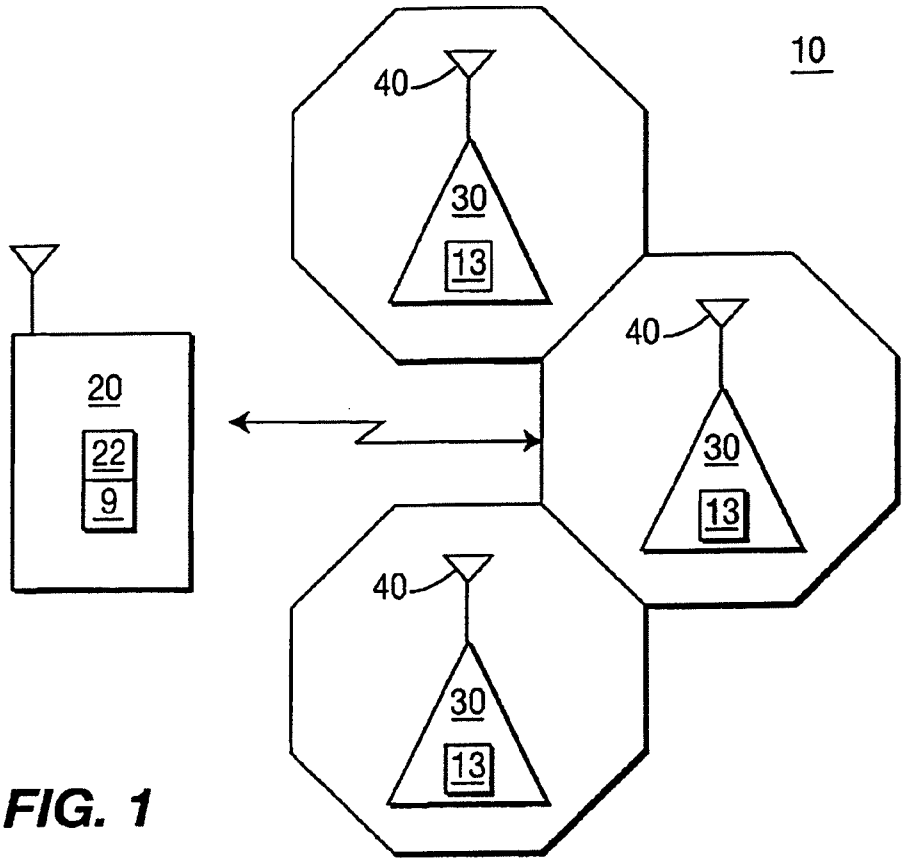
10
40
30
13
40
30
13
20
22
9
40
30
13

FIG. 1

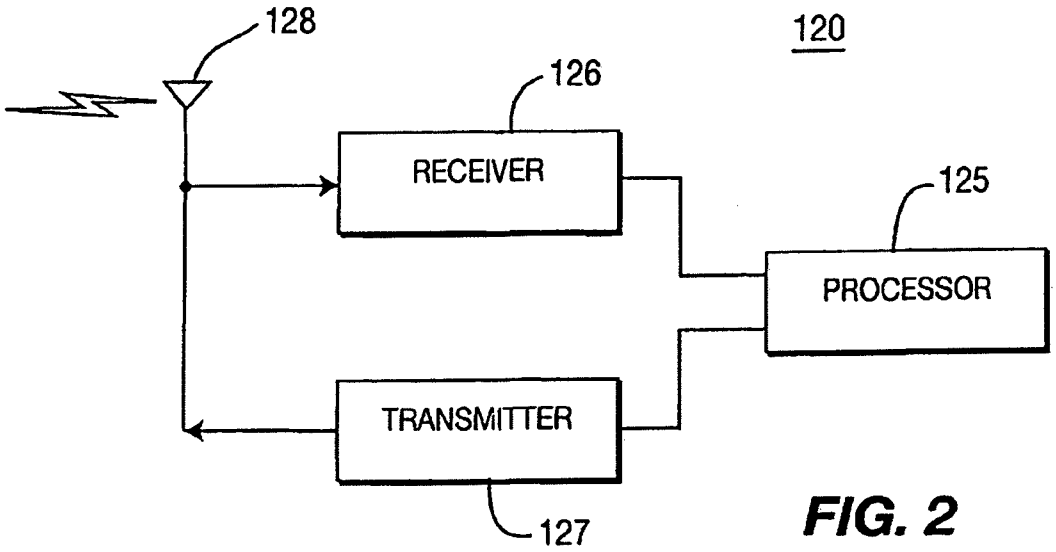
128
120
126
RECEIVER
125
PROCESSOR
TRANSMITTER
127

FIG. 2

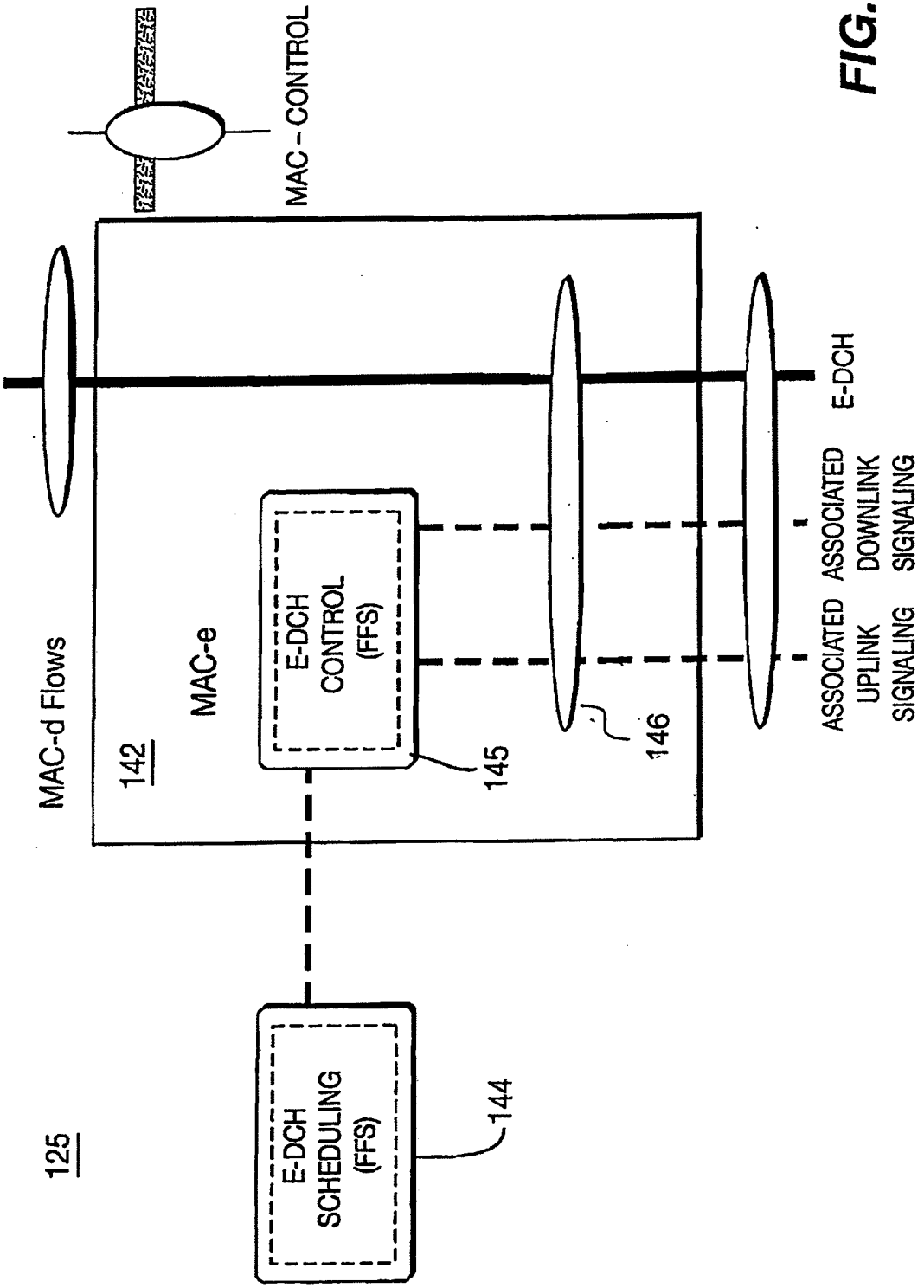
125
E-DCH SCHEDULING (FFS)
144
142
MAC-e
E-DCH CONTROL (FFS)
145
146
MAC-d Flows
MAC - CONTROL
E-DCH
ASSOCIATED UPLINK SIGNALING
ASSOCIATED DOWNLINK SIGNALING

FIG. 3

400

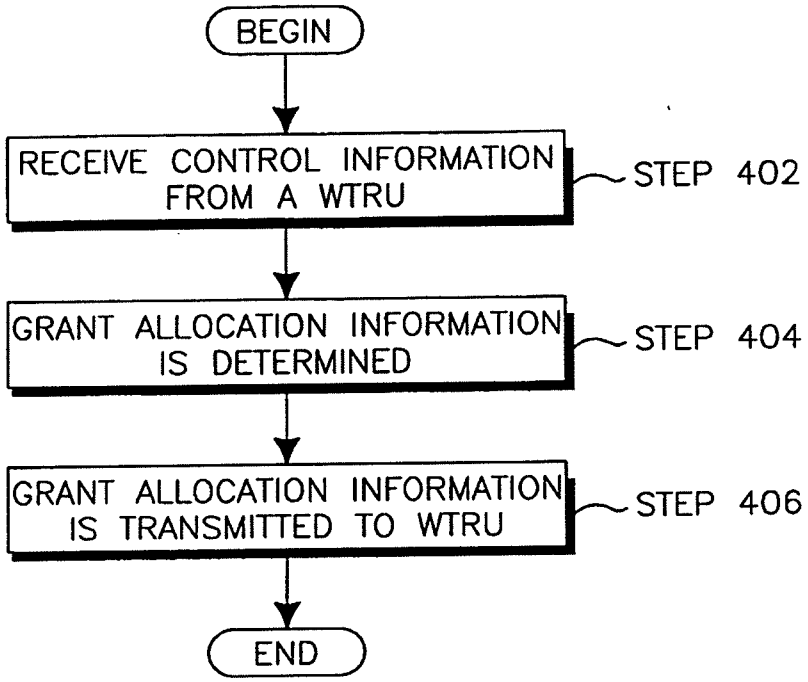
BEGIN
RECEIVE CONTROL INFORMATION FROM A WTRU
STEP 402
GRANT ALLOCATION INFORMATION IS DETERMINED
STEP 404
GRANT ALLOCATION INFORMATION IS TRANSMITTED TO WTRU
STEP 406
END

FIG. 4

500

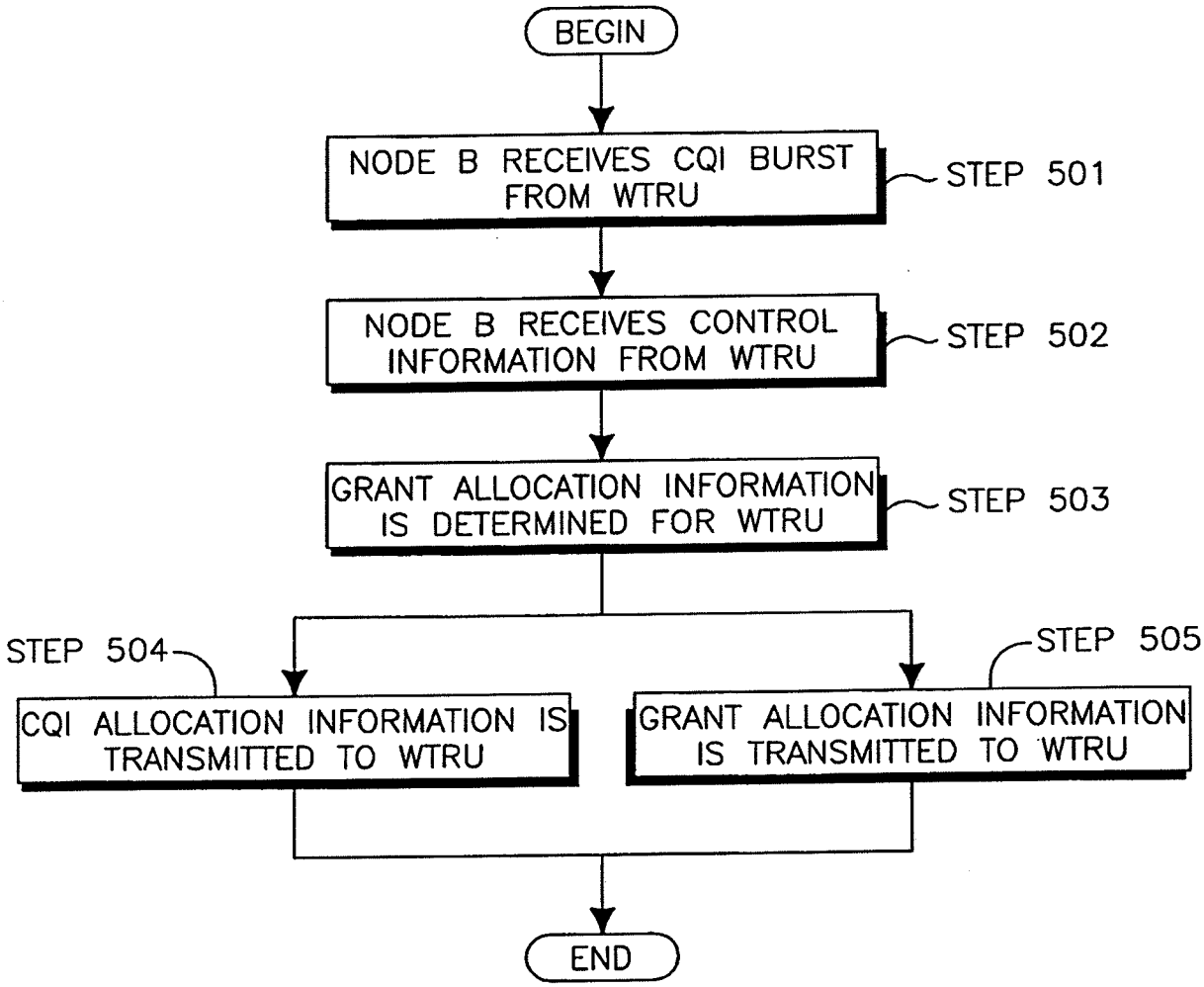
BEGIN
NODE B RECEIVES CQI BURST FROM WTRU
STEP 501
NODE B RECEIVES CONTROL INFORMATION FROM WTRU
STEP 502
GRANT ALLOCATION INFORMATION IS DETERMINED FOR WTRU
STEP 503
STEP 504
CQI ALLOCATION INFORMATION IS TRANSMITTED TO WTRU
STEP 505
GRANT ALLOCATION INFORMATION IS TRANSMITTED TO WTRU
END

FIG. 5