

DESCRIPTION**TITLE: Process for fabricating a strained layer**

This application is based on and claims priority of French patent application number FR 23/08447 filed on August 3, 2023, entitled "Procédé de fabrication d'une couche contrainte", which is incorporated herein by reference within the limits provided by law.

Technical field

[0001] The present disclosure generally concerns the manufacturing of strained layers. Such strained layers are particularly advantageous for structures used in microelectronics, and in particular for structures of SSOI ("Strained Silicon On Insulator") type.

Prior art

[0002] Silicon-on-insulator (SOI) substrates comprise a substrate made of a semiconductor material covered by a thin oxide layer and a silicon layer. These structures are particularly advantageous because they avoid the use of a bulk substrate and also enable to increase the integration density of components.

[0003] The forming of a strained layer within these structures is of great interest for many applications.

[0004] For example, the creation of SSOIs enables to increase the performance of microprocessors [Huang et al. "Carrier mobility enhancement in strained Si-on-insulator fabricated by wafer bonding," 2001 Symposium on VLSI Technology, 2001. Digest of Technical Papers, 57-58, 2001; Mazurier et al. "High performance and low variability fully-depleted strained-SOI MOSFETs," 2010 IEEE International SOI Conference (SOI), 1-2, 2010].

[0005] The straining of a germanium film also enables to form optical devices due to the obtaining of a direct gap in the germanium [Gassenq et al. "1.9% Bi-Axial Tensile Strain in Thick Germanium Suspended Membranes Fabricated in Optical Germanium-on-Insulator Substrates for Laser Applications," *Applied Physics Letters* 107, 19, 2015, 191904].

[0006] Generally, to manufacture a strained layer, an epitaxial growth step is implemented. This type of growth enables to play on lattice parameter mismatches. However, inevitably dislocations and other crystallographic defects appear in strained layers. Thus, it is difficult in an SSOI structure to obtain less than 10^5 dislocations/cm².

[0007] Otherwise, in order to better control the strain in the SSOI structure, it is possible to manufacture these structures by implementing hot bonding [Abadie et al. "Germanium Thin Film Manufacturing Using Covalent Bonding Process," *Semiconductor Science and Technology* 37, 4, 2022, 045012] or by bonding under an imposed curvature, as described in patent EP1570509 B1. These different bonding techniques enable to impose strain in the structure while avoiding the occurrence of crystallographic defects.

[0008] However, after hot bonding, the bonded structure needs to withstand the return to room temperature despite the differences in expansion coefficients of the bonded materials. However, since the bonded materials have large thicknesses (typically greater than 100 μm), the stored elastic energy reaches significant values, likely to induce defects or breakage in the bonded structure. It is therefore necessary to limit the hot bonding temperature, which limits the accessible level of strain.

Summary of the invention

[0009] There is a need to obtain a method of manufacturing tensilely or compressively strained layers, the resulting strained layers needing to exhibit a high level of strain (in particular greater than 200 MPa, preferably greater than 700 MPa or even greater than 1 GPa) and a low rate of crystallographic defects, or even no crystallographic defect at all.

[0010] This aim is achieved by a method of manufacturing a strained layer comprising the following steps:

- a) Providing, on the one hand, a first elementary structure comprising a first support substrate made of a first material having a thickness, for example, greater than 100 μm , preferably greater than 500 μm , for example greater than 700 μm , covered by a metal or semiconductor or insulating layer having a thickness smaller than 10 μm , made of a material different from the first material, and, on the other hand, a second elementary structure comprising a second support substrate having a thickness, for example, greater than 100 μm , preferably greater than 500 μm , for example greater than 700 μm , the first support substrate and the second support substrate being selected so that the coefficient of thermal expansion of the first support substrate is different from the coefficient of thermal expansion of the second support substrate and so that the coefficient of thermal expansion of the first support substrate and the coefficient of thermal expansion of the second support substrate induce a desired level of strain in the metal or semiconductor or insulating layer during step c),
- b) Transferring the metal or semiconductor or insulating layer onto the second elementary structure by assembling the first elementary structure and the second elementary structure by

bonding at a bonding temperature T_c such that $T_c > 70^\circ\text{C}$, whereby a bonded structure is obtained in which the metal or semiconductor or insulating layer is strained to a first level of strain, then removing the first support substrate at a temperature T_t such that $T_c - 50^\circ\text{C} < T_t < T_c + 50^\circ\text{C}$ and such that $T_t > 70^\circ\text{C}$, between the bonding and the removal of the first support substrate, the temperature of the bonded structure being maintained at a temperature both higher than 70°C and varying by no more than 50°C with respect to the bonding temperature, so that the metal or semiconductor or insulating layer, once transferred, is strained with the first level of strain on the second support substrate,

c) Cooling the resulting assembly, whereby a tensilely or compressively strained metal or semiconductor or insulating layer at the desired level of strain is obtained.

[0011] The desired level of strain is equal to the first level of strain if the material of the useful layer is the same as that of the second support substrate. If the material of the useful layer and the material of the second support substrate are different, the strain of the useful layer will be modified according to the difference in CTE between the two materials.

[0012] The invention differs fundamentally from prior art by the implementation at high temperature of all the transfer steps, that is, not only is the elementary structure bonding step carried out at high temperature, but also the step of removal of the first support substrate. At high temperature means a temperature above 70°C .

[0013] Further, between the bonding of the two elementary structures and the removal of the first support substrate, the temperature of the bonded structure is maintained at a temperature T_t such that $T_c - 50^\circ\text{C} < T_t < T_c + 50^\circ\text{C}$ and such that

$T_t > 70^{\circ}\text{C}$. In other words, the bonded structure is always at a temperature higher than 70°C .

[0014] Since the layer has a low thickness (smaller than $10\text{ }\mu\text{m}$), during the heating, high strain appears in the layer but not, or relatively little, in the first support substrate, since the latter is much thicker. The stored elastic energy will then be sufficiently low to prevent any breakage or generation of defects in the support substrate.

[0015] Further, since the layer has a low thickness (smaller than $10\text{ }\mu\text{m}$), during the cooling, high strain appears in the layer but not, or relatively little, in the second support substrate, since the latter is much thicker. The stored elastic energy will then be sufficiently low to prevent any breakage or generation of defects in the support substrate.

[0016] An assembly comprising the second support substrate, virtually free of strain, covered by the metal or semiconductor or insulating layer, within which the internal strain is relatively homogeneous and higher than that initially present in the same layer on the first support before heating, is thus obtained.

[0017] During step c), temperature T_t may be identical to the bonding temperature T_c or close to the bonding temperature T_c . By close, there is meant that it varies by no more than 50°C , or even by no more than 20°C , from the bonding temperature and, preferably, that it does not vary by more than 10°C from the bonding temperature. The temperature will be selected according to the layer which is desired to be strained and so as not to adversely affect the transfer step.

[0018] The bonding is carried out at high temperature ($T_c > 70^{\circ}\text{C}$) and the temperature of the bonded structure is maintained within a temperature range having end values which

do not vary by more than 50°C, or even 20°C, and preferably 10°C, from the bonding temperature.

[0019] The smaller the temperature difference, the more the CTEs of the two substrates can be different and the greater the obtained strain will be.

[0020] Advantageously, the metal or semiconductor or insulating layer is a semiconductor layer, preferably made of silicon.

[0021] The first structure may comprise one or more additional layers positioned above and/or below the metal or semiconductor or insulating layer.

[0022] The second structure may comprise one or more additional layers positioned on the second support substrate.

[0023] The presence of these additional layers may enable to facilitate hot bonding and/or to protect the metal or semiconductor or insulating layer.

[0024] The additional layers may be selected, for example, from among oxide layers, nitride layers, and layers of amorphous semiconductor material.

[0025] Advantageously, the first elementary structure comprises the first support substrate, the metal or semiconductor or insulating layer and a first layer of amorphous semiconductor material and/or the second elementary structure comprises the second support substrate and a second layer of amorphous semiconductor material. According to this advantageous embodiment, at step b), the first layer of amorphous semiconductor material is bonded to the second layer of amorphous semiconductor material.

[0026] Advantageously, the first support substrate and the second support substrate are selected from among substrates made of germanium, SiC, sapphire, copper, stainless steel, silicon, SiGe, GaN, silica, InP, AsGa, and diamond. The

support substrates are selected according to the layer to be transferred.

[0027] According to a first advantageous embodiment, the first support substrate is made of sapphire and the second support substrate is made of silica.

[0028] According to a second embodiment, the first support substrate is made of copper and the second support substrate is made of silica.

[0029] These first two variants are advantageous to apply tension to a layer, for example a silicon layer.

[0030] According to a third advantageous alternative embodiment, the first support substrate is made of silicon and the second support substrate is made of copper.

[0031] Advantageously, on assembly of the first elementary structure with the second elementary structure, a so-called curved bonding may be performed to adapt the level of strain.

[0032] Advantageously, a plurality of iterations of steps b) and c) will be performed in order to increase the strain within the layer. Preferably, according to this advantageous variant, the method comprises, after step c), the following steps:

d) bonding the metal or semiconductor or insulating layer to a third support substrate, preferably identical to the first support substrate,

e) removing the second support substrate,

f) transferring the metal or semiconductor or insulating layer onto a fourth support substrate, preferably identical to the second support substrate, by implementing step b),

g) cooling the assembly obtained at step f).

[0033] Advantageously, the metal or semiconductor or insulating layer is a semiconductor layer and the method comprises a subsequent step, after step c) or after step g),

during which said layer is transferred onto a semiconductor substrate covered by an oxide layer, whereby a structure on insulator (an SSOI if the layer of interest is silicon) is formed.

Brief description of the drawings

[0034] These features and advantages, as well as others, will be described in detail in the following description of specific embodiments given by way of illustration and not limitation with reference to the accompanying drawings, in which:

[0035] Figure 1A, Figure 1B, and Figure 1C schematically show different steps of a method of manufacturing a strained layer according to a first specific embodiment of the invention;

[0036] Figure 2A, Figure 2B, and Figure 2C schematically show different steps of a method of manufacturing a strained layer according to another specific embodiment of the invention;

[0037] Figure 3A, Figure 3B, and Figure 3C schematically show different steps of a method of manufacturing an elementary structure comprising a layer to be strained according to a specific embodiment of the invention;

[0038] Figure 4A, Figure 4B, Figure 4C, and Figure 4D schematically show different steps of a method of manufacturing an elementary structure comprising a layer to be strained according to another specific embodiment of the invention; and

[0039] Figure 5 shows, schematically and in cross-section, an SSOI structure comprising a strained layer according to a specific embodiment of the invention.

[0040] For reasons of clarity of the drawings, the various elements are not shown to a homogeneous scale.

Description of embodiments

[0041] The same elements have been designated by the same references in the various drawings. In particular, structural and/or functional elements common to the different embodiments may have the same references and may have identical structural, dimensional and material properties.

[0042] For the sake of clarity, only those steps and elements that are useful for understanding the described embodiments have been shown and have been described in detail.

[0043] In the following description, when reference is made to relative positional qualifiers, such as the terms "on," "under," etc., reference is made unless otherwise specified to the orientation of the drawings.

[0044] Unless specified otherwise, the expressions "about", "approximately", "substantially", and "in the order of" signify plus or minus 10%, preferably of plus or minus 5%.

[0045] The method of manufacturing a strained metal or semiconductor or insulating layer will now be described in more detail, first referring to Figures 1A to 1C as well as to Figures 2A to 2C. The layer may be tensilely or compressively strained depending on the use of the strained layer.

[0046] The method of manufacturing the strained metal or semiconductor or insulating layer comprises a step during which the metal or semiconductor or insulating layer 11 is transferred from a first support substrate 10 to a second support substrate 20, the support substrates 10, 20 having different coefficient of thermal expansions. The bonding and transfer step is carried out at high temperature. After removal of the first support substrate, the resulting structure is cooled, whereby a metal or semiconductor or

insulating layer 11 under tensile or compressive strain is obtained.

[0047] More specifically, the method comprises the following steps:

a) providing, on the one hand, a first elementary structure S1 comprising a first support substrate 10 covered by a metal or semiconductor or insulating layer 11 having a thickness smaller than 10 μm , and on the other hand, a second elementary structure S2 comprising a second support substrate 20, the coefficient of thermal expansion of the first support substrate 10 being different from the coefficient of thermal expansion of the second support substrate 20 (Figures 1A and 2A),

b) transferring the metal or semiconductor or insulating layer 11 from the first support substrate 10 onto the second support substrate 20:

- by assembling the first elementary structure S1 and the second elementary structure S2 by bonding at a bonding temperature T_c such that $T_c > 70^\circ\text{C}$ (Figures 1B and 2B), whereby a bonded structure is obtained, then

- by removing the first support substrate 10 at a temperature T_t such that $T_t > 70^\circ\text{C}$ and such that $T_c - 50^\circ\text{C} < T_t < T_c + 50^\circ\text{C}$, and preferably $T_c - 20^\circ\text{C} < T_t < T_c + 20^\circ\text{C}$, and more preferably $T_c - 10^\circ\text{C} < T_t < T_c + 10^\circ\text{C}$ (Figures 1C and 2C),

between the bonding and the removal of the first support substrate, the temperature of the bonded structure always being at a temperature higher than 70°C and at a temperature varying by no more than 50°C , preferably varying by no more than 20°C and preferably varying by no more than 10°C from the bonding temperature,

c) cooling the assembly obtained at step b), whereby a metal or semiconductor or insulating layer 11 under tensile or compressive strain is obtained.

[0048] The layer 11 to be strained may be a metal layer, a semiconductor layer, or an insulating layer. By insulating layer, there is meant an electrically-insulating layer. Preferably, it is a semiconductor layer and, even more preferably, it is a semiconductor layer made of silicon or SiGe. The semiconductor layer may be an amorphous layer or a crystalline (preferably monocrystalline) layer. The insulating layer may be silica.

[0049] The layer 11 to be strained has a thickness smaller than 10 μm , preferably smaller than 2 μm . The thickness of the layer may be smaller than 500 nm, or even smaller than 200 nm. Preferably, the thickness of layer 11 is greater than 5 nm and even more preferably greater than 10 nm. Depending on its thickness, this layer may also be called a film.

[0050] The coefficient of thermal expansion (CTE) of the first support substrate 10 is different from the coefficient of thermal expansion of the second support substrate 20. The substrates are selected according to the desired strain (tension or compression) and to the nature of the layer to be strained.

[0051] The material of the first support substrate 10 is different from the material of layer 11. Thus, the coefficient of thermal expansion of the first support substrate 10 is different from the coefficient of thermal expansion of layer 11. The difference in CTE between the material of layer 11 and the material of the first support substrate 10 will induce, during the temperature rise, prior to the bonding, either a compression or tensioning of layer 11. The layer then is in a first level of strain. By selecting the appropriate material for the second support substrate, it is possible to increase or decrease this tension or compression in order to obtain the desired level of strain in layer 11 at the end of the method.

[0052] The coefficient of thermal expansions of the support substrates 10, 20 may be higher or lower than the coefficient of thermal expansion of the layer 11 to be strained. Preferably, the coefficient of thermal expansion of one of the support substrates 10, 20 is higher than that of the layer 11 to be strained, and the coefficient of thermal expansion of the other support substrate 10, 20 is lower than that of the layer 11 to be strained.

[0053] The support substrates 10, 20 are selected from among substrates made of germanium, SiC, sapphire, copper, stainless steel, silicon, SiGe, GaN, silica, InP, AsGa, and diamond.

[0054] For example, to apply tension to a layer 11, with a silicon layer, the first support substrate 10 and the second support substrate 20 may be selected from among one of the following pairs:

- a first support substrate 10 made of sapphire and a second support substrate 20 made of silica,
- a first support substrate 10 made of copper and a second support substrate 20 made of silica.

[0055] As an example, silica has a CTE of approximately 0.5 ppm, which varies little with temperature.

[0056] On the contrary, silicon has a CTE which typically varies between 2 ppm at room temperature (that is, at a temperature in the range from 20 to 25°C) and 4 ppm around 450°C.

[0057] Copper has a CTE which typically varies between 16 ppm at room temperature and 20 ppm around 450°C.

[0058] Sapphire has a CTE which typically varies between 6.5 ppm at room temperature and 7.5 ppm around 450°C.

[0059] Thus, when the first structure S1 is heated during step b), the copper or sapphire support substrate 10 expands

more than the silicon, leading to expansion of silicon layer 11. The expanded silicon layer 11 is hot-assembled with the second support substrate 20 made of silica, which almost does not expand. The first support substrate 10 is removed at high temperature. When the temperature decreases back, silica support substrate 10 hardly contracts at all, and silicon layer 11, which tends to contract, sees its tension further increased.

[0060] If the first support substrate was not removed before cooling, the assembly formed by the assembling of the first elementary structure and of the second elementary structure would break due to the internal strain generated by difference in coefficients of thermal expansion between the two support substrates.

[0061] The first structure S1 may be formed of the first support substrate 10 covered by the layer to be strained 11.

[0062] According to an advantageous alternative embodiment, the first structure S1 further comprises a first layer 13 of material capable of facilitating or allowing hot bonding. The first layer 13 may also advantageously protect layer 10 during the bonding and transfer. This layer may in particular be made of an amorphous semiconductor material such as amorphous silicon (Figure 1A).

[0063] According to a specific alternative embodiment, the first structure S1 further comprises an oxide layer 12 positioned between the layer 11 to be strained and amorphous silicon layer 13 (Figure 2A). Generically, it is possible to have one/a plurality of multilayer(s) above and/or below layer 11.

[0064] The first structure S1 may also comprise, between the first support substrate 10 and the layer to be strained 11, a layer or a multilayer allowing detachment during step b),

particularly in the case of a laser lift-off (LLO). It may be a bilayer comprising a GaN layer and an oxide layer, for example, in the case of a first support substrate 10 made of sapphire. It may also be a $\text{SiO}_2/\text{AlN}/\text{SiO}_2$ or $\text{SiO}_2/\text{TiN}/\text{SiO}_2$ trilayer, for example, in the case of a first support substrate 10 made of silicon. It may also be a silicon layer or a silicon/oxide bilayer in the case of the use of the Smart Cut™ process to perform the transfer. The fracture due to the Smart Cut™ process occurs in this silicon layer and not in layer 11. This silicon layer may be polycrystalline. As a variant, the fracture may occur in layer 11.

[0065] As shown in Figures 3A to 3C and in Figures 4A to 4C, the first structure S1 can be obtained by bonding to the first support substrate 10 or, where applicable, to the detachment layer or multilayer, an SOI substrate comprising a semiconductor substrate 14 covered by an oxide layer 12 and a semiconductor layer 11, and then removing the semiconductor substrate 14 and, optionally, the oxide layer 14. This enables to obtain the structure which will be bonded and transferred at high temperature.

[0066] The second structure S2 may be formed of the first support substrate 20.

[0067] According to an advantageous alternative embodiment, the second structure S2 may be formed of the second support substrate 20 covered by a second layer 21 of material capable of facilitating or allowing hot bonding. This layer may in particular be made of an amorphous semiconductor material such as amorphous silicon (Figure 1A).

[0068] Preferably, the first layer of amorphous semiconductor material 13 and the second layer of amorphous semiconductor material 21 are made of silicon.

[0069] The first layer of amorphous semiconductor material 13 and the second layer of amorphous semiconductor material 21 may be formed, for example, by a chemical vapor deposition technique, in particular by low-pressure chemical vapor deposition (LPCVD).

[0070] In step b), the layer to be strained 11 is transferred from the first elementary structure S1 to the second elementary structure S2. The transfer consists, in a first step, of assembling at high temperature the first elementary structure S1 to the second elementary structure S2 in order to position layer 11 on the second elementary structure S2, and then removing at high temperature the first support substrate 10.

[0071] First, the two elementary structures S1 and S2 are assembled by hot bonding. For example, the elementary structures S1 and S2 are assembled by bringing into contact the surfaces of the layers of amorphous semiconductor material 13, 21, if they are present.

[0072] In order to facilitate the bonding, the surfaces to be bonded may be previously subjected to various treatments, for example a mechanical and/or chemical polishing, a chemical treatment, a UV/ozone treatment, a RIE (Reactive Ion Etching), plasma, or a hydrogen anneal, etc.

[0073] The bonding may be performed under ultra-high vacuum (UHV).

[0074] Preferably, the bonding is a SAB ("Surface Activated Bonding"). For this purpose, the surfaces of structures S1 and S2 are ionically bombarded under ultra-high vacuum before being brought into contact.

[0075] In the case of a SAB bonding and of a second support substrate 20 made of silica, a second layer 21 of amorphous

silicon may be previously deposited on the second support substrate 20 in order to facilitate the SAB bonding.

[0076] It is possible to cover the layer 11 to be strained with an oxide layer and then with a layer 13 of amorphous silicon. The oxide layer avoids damaging layer 11, and in particular creating on the surface an undesirable amorphous area during the SAB method. Amorphous silicon layer 13 facilitates the SAB bonding.

[0077] Alternatively, the bonding is an ADB ("Activated Diffusion Bonding"). A filler metal may be used to assemble the surfaces to be bonded. It may also be a semiconductor layer such as silicon or germanium.

[0078] According to an embodiment, the bonding may be a so-called curved bonding. The curvature of the layers of amorphous semiconductor material 13, 21 will be selected so as to allow transfer of the layer to be strained 11 (metal, semiconductor or insulating layer). The bonding will then be carried out at high temperature and with a curvature.

[0079] To perform a curved bonding, before bringing into contact the two amorphous layers 13, 21, a state difference in the tangential strain between the two surfaces to be assembled is created. This difference can be obtained by curving each of the two elementary structures S1, S2 to be assembled, for example by applying mechanical forces. For example, the use of electrostatic supports ("chucks") having a curvature enables to impose a curvature on S1 and S2 on application of the electrostatic force. Advantageously, structures S1 and S2 are curved so that the two surfaces to be assembled are complementary. For example, one of the surfaces may be concave and the other surface may be convex.

[0080] The bonding of amorphous layers 13, 21 is carried out at a bonding temperature referred to as T_c . The bonding

temperature is determined according to the materials to be bonded. Advantageously, temperature T_c may be maintained after the bonding for a period in the range from 1 min to 10 h. The bonding temperature T_c is higher than the ambient temperature (T_A) by at least 50°C , that is, for a typical 20°C ambient temperature, the bonding temperature T_c is higher than 70°C . Advantageously, $T_c > RT + 380^\circ\text{C}$ (in other words, $T_c > 400^\circ\text{C}$ if $RT = 20^\circ\text{C}$) or even $T_c > RT + 880^\circ\text{C}$ (in other words, $T_c > 900^\circ\text{C}$ if $RT = 20^\circ\text{C}$).

[0081] During the bonding, elementary structures S_1 and S_2 may each be held by electrostatic supports ("chucks") capable of being heated to identical or different temperatures.

[0082] According to a first alternative embodiment, during the bonding, the first elementary structure S_1 and the second elementary structure S_2 are at identical temperatures.

[0083] According to another alternative embodiment, during the bonding, the first elementary structure S_1 and the second elementary structure S_2 are at different temperatures. The bonding temperature T_c is then considered as the highest temperature.

[0084] After bonding, the first support substrate 10 is removed at a high temperature T_t . Temperature T_t may be identical to bonding temperature T_c or close to bonding temperature T_c . Between the transfer and the bonding, the bonded structure remains close to T_c .

[0085] By close, there is meant that it does not vary by more than 20°C and, preferably, that it does not vary by more than 10°C . In other words, step c) is carried out at a temperature T_t such that $T_c - 20^\circ\text{C} < T_t < T_c + 20^\circ\text{C}$, and preferably such that $T_c - 10^\circ\text{C} < T_t < T_c + 10^\circ\text{C}$.

[0086] Advantageously, temperature T_t may be maintained for a period in the range from 1 min to 10 h.

[0087] Depending on the transfer technique used, a portion of layer 11 may also be removed. This is particularly the case in a Smart Cut™ type process. The removed thickness however remains small as compared with the thickness of the layer at the time of its bonding. In particular, less than 90% or, more specifically, less than 50% or less than 10% of the thickness of the layer are removed. In order not to change the thickness of layer 11, it is possible to perform the Smart Cut™ in a layer positioned under layer 11.

[0088] In order to implement the Smart Cut™-type method, a step of implantation of ionic species, such as hydrogen and/or helium, possibly combined with boron, is carried out in layer 11 so as to form an embrittlement zone delimiting the portion of layer 11 to be transferred. The fracture of the first elementary structure S1 takes place along the embrittlement zone, which enables to detach the remainder of elementary structure S1 and to transfer thin layer 11. The implantation step is carried out before implementing step b).

[0089] According to another embodiment, the removal of the first support substrate 10 may be carried out by a laser lift-off (LLO) process, for example by the Nanocleave™ process. In the case of a laser lift-off (LLO) process, a layer or multilayer allowing detachment is positioned between the first support substrate 10 and the metal or semiconductor or insulating layer 11.

[0090] Alternatively, the removal of the first support substrate 10 may be achieved by a process implementing a porous material (for example, porous SiOCH) or a process implementing the melting of a sacrificial layer with a mechanical separation ("slide off").

[0091] During step c), the assembly obtained after transfer of the metal or semiconductor or insulating layer 11 is cooled. The assembly is preferably cooled to room temperature. By

room temperature, there is meant a temperature in the range from 20 to 25°C.

[0092] At the end of step c), an assembly comprising the second support substrate 20, possibly amorphous layers 13, 21, potentially one or more additional layers necessary for the final structure and/or the implementation of the method, and the metal or semiconductor or insulating layer 11 under tensile or compressive strain, is obtained.

[0093] To increase the strain within the layer, the method may further comprise, after step c), the following steps:

d) Bonding the metal or semiconductor or insulating layer 11 to a third substrate, preferably identical to the first substrate 10,

e) Removing the second substrate 20,

f) Cooling the assembly obtained at step f).

[0094] Step d) is preferably carried out by direct bonding and, even more preferably, by SAB or ADB.

[0095] Step f) enables to transfer the metal or semiconductor or insulating layer 11 by hot bonding and removal of the third substrate while hot.

[0096] At the end of step f), a metal or semiconductor-conductive layer 11 having a higher level of strain than that obtained at the end of step b) is obtained.

[0097] Thus, by repeating this sequence several times, it is possible to significantly increase the strain within layer 11.

[0098] The number of iterations will be selected according to the desired level of strain and thickness of the metal or semiconductor or insulating layer 11. In fact, at each transfer step, a portion of layer 11 may be removed. Advantageously, additional layers are cleverly arranged to carry out the transfers.

[0099] This method enables to obtain a layer, for example made of silicon, under tensile or compressive strain.

[0100] The obtained layer exhibits a strain higher than 200 MPa, preferably higher than 400 MPa, even more preferably higher than 700 MPa, and most preferably higher than 1 GPa.

[0101] Such a layer is particularly advantageous for applications in microelectronics, especially in the high-frequency range, charge carriers then having a greater mobility.

[0102] Thus, at the end of step c) or step g), the layer 11 under tensile or compressive strain may be advantageously deposited on a substrate of interest. For example, in the case of a semiconductor layer 11, particularly made of silicon, this layer may be deposited on a substrate of interest comprising a silicon substrate 30 and an oxide layer 31 to form an SSOI substrate (Figure 5).

[0103] The SSOI structure successively comprises a semiconductor substrate, an oxide layer, and a semiconductor layer under tensile or compressive strain, the semiconductor layer having a strain higher than 200 MPa, preferably higher than 400 MPa, even more preferably higher than 700 MPa, and most preferably higher than 1 GPa in absolute value. The tensilely or compressively strained semiconductor layer is preferably defect-free.

[0104] Various embodiments and variants have been described. Those skilled in the art will understand that certain features of these various embodiments and variants could be combined, and other variants will occur to those skilled in the art.

[0105] Finally, the practical implementation of the described embodiments and variants is within the abilities of those skilled in the art based on the functional indications given hereabove.

[0106] **Illustrative and non-limiting examples of different specific embodiments**

[0107] First example: manufacturing of an SSOI implementing a Smart Cut™ step from a sapphire substrate and a silica substrate

[0108] In this first example, to begin with, an SOI substrate is bonded to a first sapphire support substrate by direct bonding.

[0109] The SOI substrate is a commercial SOI substrate formed of a silicon substrate having a 200-mm diameter and a 725- μm thickness, covered with a 500-nm oxide and a 1,000-nm thin silicon film.

[0110] The first sapphire substrate is a substrate with a 200-mm diameter and a 725- μm thickness.

[0111] Before bonding, a nitrogen plasma treatment is carried out on the SOI substrate, after which ethylenediamine (diluted to 10^{-4} M) is added to this same substrate. After bonding, a thermal anneal at 150°C is performed (the maximum temperature above which such a bonding breaks is approximately 200°C).

[0112] A lapping step is carried out on the silicon substrate to decrease the substrate thickness down to approximately 50 μm . A chemical etching based on HF/HNO₃ enables to remove the remaining portion of the substrate. The concentration is, for example, 1% by volume of HF (50%) in HNO₃ (70%). This step can be performed in a machine, for example in a machine which treats only one side, such as an SEZ-type machine. The oxide, which was used to stop the chemical etching, then undergoes a chemical mechanical polishing (CMP) to decrease its thickness down to 100 nm and decrease its roughness to below 0.3 nm RMS to make it compatible with direct bonding.

[0113] A 30-nm amorphous silicon layer is then deposited by low-pressure chemical vapor deposition (LPCVD) at 550°C.

[0114] The silicon layer is implanted with a hydrogen dose of 8E^{16} at/cm² at a 76-keV energy.

[0115] In parallel, a second support substrate (plate) made of fused silica having a 200-mm diameter and a 725- μm thickness, is polished by CMP to obtain a surface compatible with direct bonding. A 30-nm amorphous silicon layer identical to that of the first structure is deposited on the silica plate. The amorphous silicon layers are bonded to each other by SAB ("Surface Advanced Bonding") at 400°C. For this purpose, after being placed under ultra-high vacuum (UHV or "High Ultra Vacuum") at 10^{-8} mbar, the surfaces to be bonded are subjected to an argon ion beam at 200 eV and 150 mA for 60 seconds. The substrates are then placed on electrostatic supports ("chucks") preheated to 400°C. After 5 minutes of thermal stabilization, the two surfaces to be bonded are brought into contact. The bonding is then carried out without no change in the levels of strain, as both substrates are at 400°C. The heat treatment is continued for 2 h to be able to implement the Smart Cut™ process. After the Smart Cut™ separation, the first support with a portion of the silicon film and the assembly formed by the silicon layer, the amorphous silicon layers, and the second support substrate are cooled to room temperature (typically between 20 and 25°C). Approximately 800 nm of silicon are transferred from the sapphire substrate to the silica substrate.

[0116] The fact of having raised the temperature of the silicon layer bonded to the sapphire to a 400°C temperature enables to impose a +262 MPa tension thereto.

[0117] After transfer onto the silica substrate, there is no change of strain in the silicon layer because the silica is at a same temperature (here 400°C). After cooling to room temperature and separation of the substrates, the silicon

layer transferred onto the silica sees its strain increase to +465 MPa.

[0118] The various above-described steps may be repeated to increase the strain in the silicon layer.

[0119] For this purpose, the silicon layer of approximately 800 nm is polished by CMP to make it compatible with direct bonding, after which the silica substrate covered with the silicon layer is cold-bonded to a new sapphire plate. The thickness of the silicon layer is then approximately 700 nm. The silica substrate is removed by lapping and chemical etching (hydrofluoric acid). The strain of the silicon layer transferred onto the sapphire substrate is still +465 MPa.

[0120] The silicon layer is then transferred onto another silica substrate at high temperature, as previously: a layer with a 930-MPa strain and a 500-nm thickness (having adjusted the hydrogen implantation) is obtained. After a new CMP step, the silicon layer is ready for a third iteration. Its thickness is then 400 nm. 200 nm of silicon with a 1,395-MPa strain and a 100-nm thickness are then obtained after a last CMP.

[0121] This 100-nm silicon layer can finally be transferred onto a silicon substrate covered with a 20-nm oxide film by lapping and chemical etching. An SSOI with a layer having a strain of approximately 1.4 GPa is obtained.

[0122] Second example: manufacturing of an SSOI using a Smart Cut™ step from a copper substrate and a silica substrate

[0123] In this second example, an SOI substrate is first bonded to a first copper support substrate by direct bonding.

[0124] The SOI substrate is a commercial SOI substrate formed of a silicon support substrate having a 200-mm diameter and a 725- μm thickness covered with a 500-nm oxide and a 400-nm thin silicon film.

[0125] The first copper support substrate is a substrate having a 200-mm diameter and a 725- μm thickness.

[0126] The SOI substrate is bonded to the copper substrate by SAB. As previously, the silicon substrate is submitted to a lapping step to decrease the thickness of the silicon substrate down to approximately 50 μm , followed by a chemical etching process based on HF/HNO_3 (concentrations of 1% by volume of HF (50%) in HNO_3 (70%)) is carried out to remove this portion of the silicon substrate. A CMP is performed on the oxide which was used to stop the chemical etching. The oxide then regains a surface state compatible with direct bonding and a 50-nm thickness. A 30-nm amorphous silicon layer is deposited on the oxide by LPCVD at 550°C. Finally, the silicon layer is implanted, for example, with a helium-hydrogen co-implantation (with energies and doses respectively of 38 keV/1.3E16 at/cm² and 24 keV/5.25E16 at/cm²).

[0127] In parallel, a second support substrate (plate) of fused silica, having a 200-mm diameter and a 725- μm thickness, is polished by CMP to obtain a surface compatible with direct bonding. A 30-nm amorphous silicon layer is deposited on its surface.

[0128] The two amorphous silicon layers are bonded by SAB at 400°C. For this purpose, as previously, the two surfaces to be bonded are placed under ultra-high vacuum at 10^{-8} mbar and activated with an argon ion beam at 200 eV and 150 mA for 60 s. The plates are then placed on electrostatic supports ("chucks") preheated to 400°C. After 5 min of thermal stabilization, the two plates are brought into contact. The bonding is then carried out with no change in the levels of strain, as both substrates are at 400°C. The thermal anneal is continued for 2 hours in order to implement the Smart Cut®

process. A silicon layer of approximately 200 nm is thus transferred from the copper substrate to the silica substrate.

[0129] Before the bonding, the fact of heating to 400°C the silicon film bonded to the copper imposes on the silicon film a +1,030-MPa tension. After the transfer onto silica, there is no change in strain because the silica is also at 400°C. After separation of the two substrates, they are cooled to room temperature. The silicon layer transferred onto the silica sees its strain increase to +1.23 GPa. A 1,395-MPa strain and a 100-nm thickness are then obtained after a final CMP.

[0130] This 100-nm layer can then be transferred onto a silicon substrate covered with a 20-nm oxide film by lapping and chemical etching. An SSOI structure comprising a silicon layer with strain of approximately 1.4 GPa is obtained in the end. In this example, there is no need to repeat the of the method to obtain an SSOI at more than 1.2 GPa.

[0131] Third example: manufacturing of an SSOI implementing a step of transfer by a "Laser Lift OFF" (LLO) process from a sapphire substrate and a silica substrate.

[0132] First, a commercial SOI substrate formed of a 100-nm thin silicon film on a 500-nm oxide is bonded to a silicon substrate with a 200-mm diameter and a 725- μ m thickness.

[0133] Next, there are successively deposited on a first sapphire substrate a 100-nm thick layer of GaN by epitaxy, and a 200-nm oxide layer on the GaN. A CMP is performed on this oxide to make it compatible with direct bonding. After having performed a nitrogen plasma treatment and adding ethanolamine (diluted to 10^{-4} M), a direct bonding of the SOI to the 200-mm diameter, 725 μ m thick sapphire substrate coated with GaN and oxide is performed. After a heat treatment at 150°C (the maximum temperature above which such a bonding

breaks is approximately 200°C), the silicon substrate is lapped to only leave 50 μm thereof, after which this remaining thickness is removed by chemical etching based on HF/HNO₃ (1% by volume of HF(50%) in HNO₃ (70%)) in a machine (for example, of SEZ type). The oxide is also removed.

[0134] The second support substrate is a plate of fused silica having a 200-mm diameter and a 725- μm thickness. It is polished by CMP to obtain a surface compatible with direct bonding. A 30-nm amorphous silicon layer is deposited thereon by LPCVD at 550°C.

[0135] To transfer the layer to be strained, an SAB bonding is first performed at 900°C. In order to do this, the two plates are placed under ultra-high vacuum at 10^{-8} mbar. An activation of each surface with an argon ion beam at 200 eV and 150 mA for 60 s is carried out. The plates are then placed on electrostatic supports ("chucks") preheated to 900°C. After 5 min of thermal stabilization, the two plates are brought into contact. The bonding is then carried out with no change in the levels of strain, as both substrates are at 900°C. The resulting assembly is then transferred, while maintaining the temperature at 900°C, into a chamber enabling transfer by a laser lift-off (LLO) technique to separate the GaN from the sapphire.

[0136] The 100-nm silicon layer is thus transferred onto the silica.

[0137] Before the bonding, as the silicon layer is bonded to the sapphire at a 900°C temperature, it is tensilely strained at +700 MPa. After transfer onto the silica, there is no change in strain because the silica is also at 900°C. After separation of the substrates, both substrates are cooled to room temperature. The silicon layer transferred onto the silica sees its strain increase to +1.24 GPa.

[0138] After removal by chemical etching of the remaining GaN and silicon oxide with HF.

[0139] The 100-nm layer can then be transferred onto a silicon substrate covered with a 20-nm oxide film by lapping and chemical etching. The result is an SSOI having a silicon layer strained to approximately 1.24 GPa.

CLAIMS

1. Method of manufacturing a strained layer comprising the following steps:
 - a) Providing, on the one hand, a first elementary structure (S1) comprising a first support substrate (10) made of a first material covered by a metal or semiconductor or insulating layer (11) made of a material different from the first material, having a thickness smaller than 10 μm , and, on the other hand, a second elementary structure (S2) comprising a second support substrate (20), the first support substrate (10) and the second support substrate (20) being selected so that the coefficient of thermal expansion of the first support substrate (10) is different from the coefficient of thermal expansion of the second support substrate (20) and that the coefficient of thermal expansion of the first support substrate (10) and the coefficient of thermal expansion of the second support substrate (20) induce a desired level of strain in the metal or semiconductor or insulating layer (11) during step c),
 - b) Transferring the metal or semiconductor or insulating layer (11) onto the second elementary structure (S2) by assembling the first elementary structure (S1) and the second elementary structure (S2) by bonding at a bonding temperature T_c such that $T_c > 70^\circ\text{C}$, whereby a bonded structure is obtained in which the metal or semiconductor or insulating layer (11) is strained at a first level of strain, then removing the first support substrate (10) at a temperature T_t such that $T_c - 50^\circ\text{C} < T_t < T_c + 50^\circ\text{C}$, between the bonding and the removal of the first support substrate (10), the temperature of the bonded structure being maintained at a temperature both higher than 70°C and varying by no more than 50°C from the bonding temperature, so that the metal or semiconductor or insulating layer (11),

once transferred, is strained with the first level of strain on the second support substrate (20),

c) Cooling the resulting assembly, whereby a tensilely or compressively strained metal or semiconductor or insulating layer (11) at the desired level of strain is obtained.

2. Method according to claim 1, characterized in that the metal or semiconductor or insulating layer (11) is a semiconductor layer, preferably made of silicon.
3. Method according to any of claims 1 and 2, characterized in that the first support substrate (10) and the second support substrate (20) are selected from among substrates made of germanium, SiC, sapphire, copper, stainless steel, silicon, SiGe, GaN, silica, InP, AsGa, and diamond.
4. Method according to any of the foregoing claims, characterized in that the first elementary structure (S1) comprises one or more additional layers that can be positioned above and/or below the metal or semiconductor or insulating layer (11) and/or in that the second elementary structure (S2) comprises one or more additional layers positioned on the second support substrate (20).
5. Method according to any of the foregoing claims, characterized in that the first elementary structure (S1) comprises the first support substrate (10), the metal or semiconductor or insulating layer (11), and a first layer of amorphous semiconductor material (13) and/or in that the second elementary structure (S2) comprises the second support substrate (20) and a second layer of amorphous semiconductor material (21).
6. Method according to any of claims 1 to 5, characterized in that the first support substrate (10) is made of sapphire and the second support substrate (20) is made of silica.

7. Method according to any of claims 1 and 5, characterized in that the first support substrate (10) is made of copper and the second support substrate (20) is made of silica.
8. Method according to any of claims 1 to 5, characterized in that the first support substrate (10) is made of silicon and the second support substrate (20) is made of copper.
9. Method according to any of the foregoing claims, characterized in that temperatures T_c and T_t are identical.
10. Method according to any of the foregoing claims, characterized in that on assembly of the first elementary structure (S1) with the second elementary structure (S2), there is a state difference in the tangential strain between the first layer of amorphous semiconductor material (13) and the second layer of amorphous semiconductor material (21).
11. Method according to any of the foregoing claims, characterized in that the method comprises, after step c), the following steps:
 - d) Bonding the metal or semiconductor or insulating layer (11) to a third support substrate, preferably identical to the first support substrate (10),
 - e) Removing the second support substrate (20),
 - f) Transferring the metal or semiconductor or insulating layer (11) onto a fourth support substrate, preferably identical to the second support substrate (20), by implementing step b),
 - g) Cooling the assembly obtained at step f).
12. Method according to any of the foregoing claims, characterized in that the metal or semiconductor or insulating layer (11) is a semiconductor layer and in that the method comprises a subsequent step, after step c) or

after step g), during which said layer (11) is transferred onto a semiconductor substrate (30) covered by an oxide layer (31), whereby a structure on insulator is formed.