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(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC** [US/US]; One AMD Place, Mail Stop 68, P.O.Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and

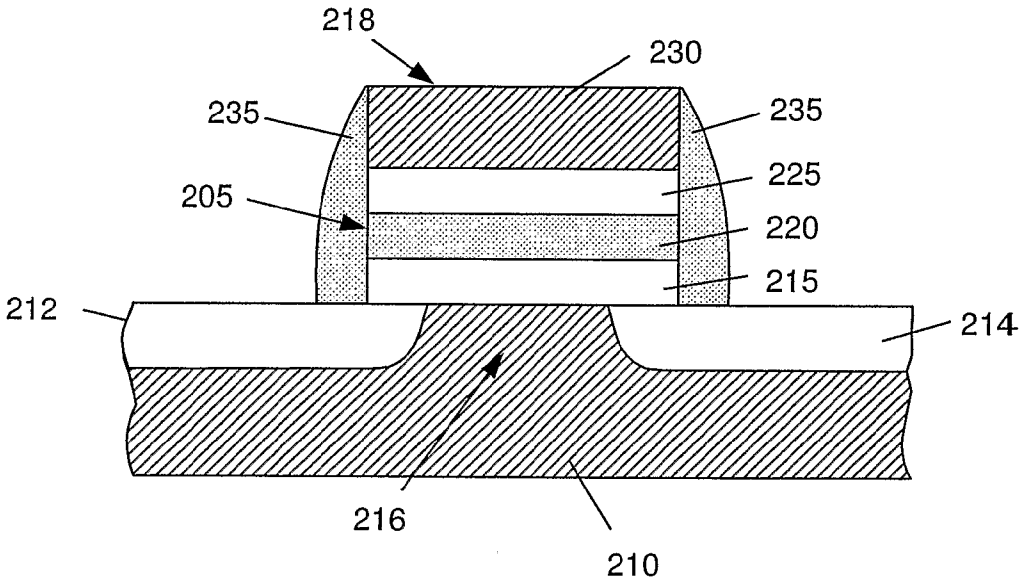
(75) Inventors/Applicants *(for US only)*: **KLUTH, George, Jonathan** [US/US]; 112 Heritage Village Way, Campbell, CA 95008 (US). **CLARK-PHELPS, Robert, B.** [US/US]; 939 Lanewood Drive, San Jose, CA 95125 (US). **JEON, Joong, S.** [US/US]; 10705 Flora Vista Avenue, Cupertino, CA 95014 (US). **ZHONG, Huicai** [CN/US]; 509 Popula Blvd., Wapppingers Falls, NY 12509 (US). **HALLIYAL, Arvind** [IN/US]; 20679 Shelly Drive, Cupertino, CA 95014 (US). **RAMSBEY, Mark, T.** [US/US]; 402 Cumulus Avenue, Sunnyvale, CA 94087 (US). **OGLE, Robert, Bertram, Jr.** [US/US]; 5947 Hosta Lane, San Jose, CA 95124 (US). **CHANG, Kuo-Tung** [US/US]; 12261 Country Squire Lane, Saratoga, CA 95070 (US). **LI, Wenmei** [CN/US]; 880 E. Fremont Avenue, Apt. #425, Sunnyvale, CA 94087 (US).

(74) Agent: **DANIEL, R., Collopy**; One AMD Place, Mail Stop 68, P.O.Box 3453, Sunnyvale, CA 94088-3453 (US).

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[Continued on next page]

(54) Title: MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME



(57) Abstract: According to one embodiment, a memory cell structure comprises a semiconductor substrate (210), a first silicon oxide layer (215) situated over the semiconductor substrate, a charge storing layer (220) situated over the first silicon oxide layer, a second silicon oxide layer (225) situated over the charge storing layer, and a gate layer (230) situated over the second silicon oxide layer. In the exemplary embodiment, the charge storing layer (220) comprises silicon nitride having reduced hydrogen content, e.g., in the range of about 0 to 0.5 atomic percent. As a result, the reduced hydrogen content reduces the charge loss in the charge storing layer (220). The reduced charge loss in the charge storing layer (220) has the benefit of reducing threshold voltage shifts, prograirnming data loss, and programming capability loss in the memory device, thereby improving memory device performance.

WO 2005/027210 A1

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