

SYSTEM AND METHOD OF EFFICIENTLY MODULATING DATA USING
SYMBOLS HAVING MORE THAN ONE PULSE

BACKGROUND

Field

5 [0001] Embodiments of the invention relate to modulation. More specifically, embodiments of the invention relate to an improved encoding density modulation scheme.

Description Of The Related Art

[0002] Various forms of modulation have long been used to
10 encode data with greater efficiency so that more data can be transmitted during a particular time period over a transmission medium. Combinations of various modulation techniques such as, pulse width modulation, amplitude modulation and rise time modulation have been employed to
15 improve the encoding density of modulation schemes. See for example, copending application entitled "Symbol-Based Signaling For An Electromagnetically-Coupled Bus System," Serial Number 09/714,244. However, such schemes often require per-emphasis and channel equalization which
20 increases the cost and complexity of the system. Moreover, in any event it remains desirable to improve coding density to allow for even higher bit rates.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1 is a diagram showing a generalized format
25 of a symbol of one embodiment of the invention.

[0004] Figure 2 is a diagram showing the modulation elements of symbol of one embodiment of the invention that encodes eight databits.

[0005] Figure 3a-3e are diagrams of possible symbols to
5 encode eight bits per symbol.

[0006] Figure 4 is a block diagram of a modulator of one embodiment of the invention.

[0007] Figure 5 is a block diagram of the demodulator of one embodiment of the invention.

10 [0008] Figure 6 is a block diagram of the system incorporating one embodiment of the invention.

DETAILED DESCRIPTION

[0009] Figure 1 is a diagram showing a generalized format of a symbol of one embodiment of the invention. The symbol
15 100 occurs within a symbol period (T_p) 106. The symbol includes a first pulse 102 alternatively referred to as a basic pulse 102 and N additional pulses 104. In Figure 1 N is equal to one, however, N could be any positive integer. Additional pulses are alternatively referred to herein as
20 IDP pulses 104.

[0010] The basic pulse 102 includes i leading slots 112, where i is a positive integer, a base pulse 114 and j lagging slots 116, where j is also a positive integer. The IDP pulse 104 includes a base pulse 118 and m lagging slots
25 where m is a positive integer. Notably, i, j and m are not necessarily equal. In Figure 1, T_{fx} is the width of a leading slot 112, T_{bx} is a width of the lagging slot 116

(alternatively referred to as front end slots and back end slots respectively) of the basic pulse 102 and T_{IDP} is a width of the lagging slot 120 of the IDP pulse 104. The slot width between leading slots and lagging slots and
5 between the pulses may not be equal.

[0011] T_{SB} is the width of the base pulse 114 of the basic pulse 102. T_{IDP} is the width of the base pulse 118 of the IDP pulse. T_{SB} and T_{SIDP} are selected in one embodiment to be the minimum pulse that can be properly propagated along the
10 communication channel without the necessity of channel compensation such as equalization. The basic pulse 102 is separated from the IDP pulse 104 by a gap with T_{g1} .

[0012] If additional IDP pulses are present within the symbol period, they will each be separated from their
15 predecessor by a gap. It is not necessary that all additional pulse have a same format. As used herein, format refers to the base pulse and lagging slots. Thus, a same format has an equal number and equal size of slots and a same width base pulse. Thus, where $m_x \neq m_y$ a different
20 format exists, where x & y refer to distinct additional pulses. A final gap occurs after the last IDP pulse 104, in this case, having a gap width T_{g2} . Amplitude modulation (AM) can be used separately on each pulse. This provides two bits of modulation (one per pulse) if return to zero
25 (RZ) AM is used or four bits of modulation (two per pulse) if non return to zero (NRZ) AM is used.

[0013] Figure 2 is a diagram showing the modulation elements of a symbol of one embodiment of the invention that encodes eight data bits. P1 is the possible starting position of the front edge of the basic pulse. A1 is the possible polarization of the basic pulse. P2 is the possible back edge position of the basic pulse. PP2 is a possible starting position of the base pulse of the IDP pulse. A2 is the possible polarization of the IDP pulse. P3 is the possible position of the back edge of the IDP pulse. In this case, referring back to the nomenclature of Figure 1, i equals 1, j equals 3 and m equals 4.

[0014] Figures 3a-3e are diagrams of possible symbols to encode eight bits per symbol in accordance with modulation elements discussed in connection with Figure 2. As can be seen, the relative position of the base pulse of the IDP pulse varies within the symbol period. This variance of the position of the base pulse of the IDP pulse encodes at least one bit, and in this example, two bits of data. Stated slightly differently, the relationship between the pulses improves modulation efficiency. The position the IDP pulse may assume depends on the duration of the basic pulse. The IDP pulse is thus moveable within the symbol period T_p . Conversely, in one embodiment, the location of the base pulse of the basic pulse is fixed within T_p .

[0015] In this 8-bit modulation example, two bits are associated with the amplitude modulation (one for basic pulse the other for IDP pulse). This assumes RZ AM. One

bit is modulated by the front edge of basic pulse. Five bits are modulated by the combinations of the basic pulse and the IDP pulse. In Figure 3a, two bits are modulated by the back edge of basic pulse and one bit is modulated by back edge of IDP pulse, which yields eight possible states. In Figure 3b, the combination of basic pulse's back edges (three edge positions) and the IDP pulse's back edges (three edge positions) results in total of nine states. Figure 3c yields eight states, similar to Figure 3a. Figure 3d, e provide an additional eight possible states. The total combinations for Figures 3a-e, provide more than 32 states for five bits of modulation. These states are addressed further below in connection with Tables 6-10.

[0016] Tables 1 through 5 show one possible mapping of the data to the symbols shown in Figures 3a-3e respectively.

TABLE 1

D ₀	A1 (1=HIGH, 0=LOW)
D ₁	P1 (0=edge_0, 1=edge_1)
D2=0	PP2
D3=0	PP2
D4	P2
D5	P2
D6	A2 (1=HIGH, 0=LOW)
D7	P3

TABLE 2

D0	A1 (1=HIGH, 0=LOW)
D1	P1 (0=edge_0, 1=edge_1)
D2=1	PP2
D3=0	PP2
D4	P2 & P3
D5	P2 & P3
D6	P2 & P3

D7	A2 (1=HIGH, 0=LOW)
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TABLE 3

D0	A1 (1=HIGH, 0=LOW)
D1	P1
D2=0	PP2
D3=1	PP2
D4	P2
D5	A2 (1=HIGH, 0=LOW)
D6	P2
D7	P3

TABLE 4

10

D0	A1 (1=HIGH, 0=LOW)
D1	P1
D2=1	PP2
D3=1	PP2
D4=0	P2
D5	A2 (1=HIGH, 0=LOW)
D6	P3
D7	P3

TABLE 5

D0	A1 (1=HIGH, 0=LOW)
D1	P1
D2=1	PP2
D3=1	PP2
D4=1	P3
D5	P2
D6	P2
D7	A2 (1=HIGH, 0=LOW)

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[0017] One of ordinary skill will recognize that various other mappings are possible and are within the scope and contemplation of embodiments of the invention.

[0018] Referring again to Figures 3a-e, in one embodiment, the symbol period, TP is 2000 ps. T_{LEAD} (width of the leading slot) is 240 ps, T_s is 320 ps T_{LAG} (width of the lagging slot for both pulses) is 160 ps, and the gap width
5 T_{gap} is 240 ps. In such an embodiment, data rates of 4Gbps can be achieved on a 30" channel with two ball grid array (BGA) packages and two connectors. A wide leading slot is used because the leading edge of the first pulse is most effected by what occurred on the channel previously. Thus,
10 by making the slot wider, it is less likely that channel noise will cause a misinterpretation of the location of the front edge.

[0019] In an alternative embodiment, TP is 1250 ps with T_{LEAD} is 130 ps, T_s is 200 ps, T_{LAG} is 110 and T_{gap} is 140.
15 This permits data rates of 6.4 Gbps on a 5" channel.

[0020] In an alternative embodiment, TP is 1000 ps. T_{LEAD} is 110 ps, T_s is 135 ps, T_{LAG} is 100 ps and T_{gap} is 110 ps. This embodiment permits data rates of 8Gbps on a 5" channel.

[0021] **Figure 4** is a block diagram of a modulator of one
20 embodiment of the invention. A three width bits wb0 through wb2 and the two IDP front edge bits IDPFE0 and IDPFE1 provide the inputs to the state control unit 402. Based on these inputs, the state control unit enables or disables various signal paths through the modulator and therefore
25 frequency controls the pulses created by the electric pulse generation units to form the symbol. The various signal paths are driven through a plurality of delays to effect the

creation of the symbols of the forms previously described. Tables 6-10 show the response of the state control unit 400 based on the inputs. In these tables "0" means pass and "1" means stop.

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TABLE 6

IDPFEO	IDPFE1	Wb0	Wb1	Wb2	SB0	SB1	SB2	SB3	SI0	SI1	SI2	SI3
19.	0 (Enable)	0	0		0	1	1	1				
		0	1		1	0	1	1				
		1	0		1	1	0	1				
		1	1		1	1	1	0				
				0					0	1	1	1
				1					1	0	1	1

TABLE 7

IDPFEO	IDPFE1	Wb0	Wb1	Wb2	SB0	SB1	SB2	SB3	SI0	SI1	SI2	SI3
1.	1 (Enable)	0	0	0	0	1	1	1	0	1	1	1
		0	0	1	0	1	1	1	1	0	1	1
		0	1	0	0	1	1	1	1	1	0	1
		0	1	1	1	0	1	1	0	1	1	1
		1	0	0	1	0	1	1	1	0	1	1
		1	0	1	1	0	1	1	1	1	0	1
		1	1	0	1	1	0	1	0	1	1	1
		1	0	1	1	1	0	1	1	0	1	1

TABLE 8

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IDPFEO	IDPFE1	Wb0	Wb1	Wb2	SB0	SB1	SB2	SB3	SI0	SI1	SI2	SI3
20.	0 (Enable)	0	0						0	1	1	1
		0	1						1	0	1	1
		1	0						1	1	0	1
		1	1						1	1	1	0
				0	0	1	1	1				
				1	1	0	1	1				

TABLE 9

IDPFEO	IDPFE1	Wb0	Wb1	Wb2	SB0	SB1	SB2	SB3	SI0	SI1	SI2	SI3
21.	1 (Enable)	0	0	0	0	1	1	1	0	1	1	1
			0	1	1	0	1	1	0	1	1	1
			1	0	1	1	0	1	0	1	1	1
			1	1	1	1	1	0	0	1	1	1
		1	0	0	0	1	1	1	0	1	1	1
			0	1	0	1	1	1	1	0	1	1
			1	0	0	1	1	1	1	1	0	1
			1	1	0	1	1	1	1	1	1	0

TABLE 10

IDPFEO	IDPFEL	Wb0	SIFE0	SIFE1	SIFE2	SIFE3	SIFE4
0	0		1	1	1	0	1
0	1		1	1	0	1	1
1	0		1	0	1	1	1
1	1	0	0	1	1	1	1
1	1	1	1	1	1	1	0

[0022] Tables 6-9 define the back edge modulation for the basic pulse (SB0-SB3) and the IDP pulse SI0-SI3. Table 10 defines the IDP pulse front edge delay states. In the aggregate, the states provide for modulation consistent with the mappings of Tables 1-5, and are implemented by state control 402 in one embodiment. Matching logic 410 insures that the forwarded clock is time consistent with the symbol generated.

[0023] **Figure 5** is a block diagram of the demodulator of one embodiment of the invention. The data is received in input 518 while the forwarded clock is received at clock recovery circuit 520. The clock is recovered in the clock recovery circuit 520 and passed into the demodulator as shown. The data is similarly forwarded into the demodulator as shown. Comparison of delayed data with the AM threshold and the clock yield the two AM bits and the front edge bit of the basic pulse via a bit mapping unit 526. Comparison of the data with various levels of delay of the clock yields the two IDP front edge bits via bit mapping unit 524.

Delays of the clock compared with the data signal also fed into state mapping units 528 and 530 which then provides their state information to bit mapping unit 532 which in turn yields the width bits wb0 through wb2. The state

control unit 522 insures that the bit mapping unit 532 outputs the right bits base on the state and the group defined by the position of the IDP pulse.

[0024] **Figure 6** is a block diagram of the system incorporating one embodiment of the invention. The processor 600 includes a modulator 400 and demodulator 500. The processor is coupled to a chip set 602 which is coupled to a memory bus 612 and an I/O bus 610. The chip set includes a memory controller 614 which also includes a modulator 400 and a demodulator 500. The memory controller interacts with the memory 604 over memory bus 612. In such an embodiment, the memory interface may may or may not include a modulation 400 and demodulator 500, as a benefit is achieved even where only the communication between the processor 600 and the memory controller 600 occurs at the high speeds provided by the described modulation scheme. An I/O device 606 which also contains a modulator 400 and a demodulator 500 is coupled to I/O bus 610 and may receive symbols modulated as previously described such that a position of an additional pulse within the symbol period encodes at least one bit. The I/O device may include, for example, a disk controller.

[0025] In another embodiment, the memory controller is embedded in the processor. Such an embodiment may or may not have a chip set, but in any event, the memory interface would need to have the corresponding modulator/demodulator to gain a benefit of the described modulation technique

during memory accesses. Also, in such an embodiment (assuming a chip set is present) the chip set need not have the modulator and demodulator for a benefit to be realized.

[0026] In the foregoing specification, the invention has
5 been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes can be made thereto without departing from the broader spirit and scope of embodiments of the invention as set forth in the appended claims. The
10 specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. A method comprising:

transmitting a first pulse during a symbol period, the
5 first pulse providing both front and back edge phase
modulation; and

transmitting a second pulse during the symbol period
following a gap, the second pulse moveable within the symbol
period such that the position of the second pulse within the
10 symbol period modulates at least one bit.

2. The method of claim 1 wherein a position of a base
pulse of the first pulse is fixed within the symbol period.

3. The method of claim 1 further comprising amplitude
modulating both the first pulse and the second pulse.

- 15 4. The method of claim 3 wherein the amplitude modulation
is non-return to zero (NRZ) amplitude modulation.

5. The method of claim 1 wherein the first pulse has at
least one leading slot and at least one lagging slot with
the leading slot wider than the lagging slot.

- 20 6. The method of claim 1 further comprising:

transmitting N additional pulses during the symbol
period each additional pulse following a gap after its
predecessor and each additional pulse moveable within the
symbol period such that the position of the additional pulse
25 within the symbol period modulates at least one bit; and
where N is a positive integer.

7. The method of claim 6 wherein the N additional pulses and the second pulse do not all have a same format.

8. A modulation symbol comprising:

a first pulse having a base pulse width, at least one
5 leading slot and at least one lagging slot;

a second pulse having a second base pulse width with a leading edge and at least one lagging slot; the leading edge positionable within a symbol period to encode at least one bit.

10 9. The modulation symbol of claim 8 wherein the first pulse and the second pulse each encode at least one bit based on an amplitude of the pulse.

10. The modulation symbol of claim 8 further comprising:

N additional pulses each with having a base pulse with
15 a leading edge and at least one lagging slot and the leading edge of each additional pulse positionable within the symbol period to encode at least one bit.

11. The modulation symbol of claim 8 wherein at least one of the first pulse and the second pulse encode at least one
20 bit based on a rise time of the pulse.

12. The modulation of symbol of claim 8 wherein slot size is nonuniform.

13. A system comprising:

a bus;

25 a processor coupled to the bus, the processor including a modulator to encode data as symbols, each symbol including

at least a first pulse and a second pulse such that a position of a base pulse of the second pulse within a symbol period encodes at least one bit;

a chip set coupled to the processor and including a
5 demodulator to receive a symbol encoded by the modulator and decode at least one bit from a position of the base pulse of the second pulse within the symbol period; and

a memory device coupled to the chip set.

14. The system of claim 13 wherein the modulator encodes at
10 least on one bit in each of the first pulse and the second pulse through amplitude modulation.

15. The system of claim 14 wherein the modulator employs non-return to zero (NRZ) amplitude modulation.

16. The system of claim 13 wherein the modulator encodes at
15 least one bit in a leading slot of the first pulse and at least one bit in a lagging slot of the first pulse.

17. The system of claim 16 wherein the modulation encodes at least one bit in a lagging slot of the second pulse.

18. The system of claim 13 wherein the device is less than
20 5" distant from the processor and the modulation has a payload of more than six giga bits per second.

19. The system of claim 13 wherein the device is more than 10" distant from the processor and the modulator has a payload of more than four giga bits per second.

20. The system of claim 13 wherein each symbol includes N additional pulses each having a base pulse position that encodes at least one bit.