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Abstract

Connection for coupling binary control and warning signals into a data processing unit

Each binary signal (B1...Bn) is supplied to a separate input module (MB1...MBn) which can be switched over in an application-specific manner via the processor (MP) in such a manner that these modules, when an active state of the corresponding binary signal (B1...Bn) occurs, generate an interrupt signal (IR1...IRn) interrupting the normal sequence of the processor (MP) or a status signal (ST1...STn) which is detected by the processor during the normal program sequence. The processor preferably contains both a register (RIR) for interrupt signals (IR1...IRn) and a register (RST) for status signals (ST1...STn). When an interrupt signal (IRn) occurs, the normal program sequence of the process is interrupted, the content of the register for interrupt signals is read and a first reset signal (RMI) is generated for those input modules which were switched over for generating interrupt signals. The content of the register for status signals is read during the normal sequence of the program of the processor and a second reset signal (RMS) is generated for those input modules which were switched over for generating status signals. Due to the mode bit control, the invention can be used universally both for interrupt-capable binary signals requiring fast response and for status-capable binary signals which do not have to be processed with time priority.

FIG 1