

A cross-sectional view of a semiconductor device. It shows a substrate (2) with a diagonal hatching pattern. On top of the substrate is a gate insulating layer (3) with a horizontal hatching pattern. A gate electrode (41) is formed on the gate insulating layer (3). The gate electrode (41) is a rectangular block with a diagonal hatching pattern, and it is connected to a gate line (4) that runs horizontally across the top of the device.

A cross-sectional view of a semiconductor device. A central channel region (2) is defined by a substrate with a diagonal hatching pattern. On either side of the channel, there are gate structures. The left gate structure consists of a lower gate (4) and an upper gate (41). The right gate structure consists of a lower gate (3) and an upper gate (41). A central region (43) is indicated by a dashed line with arrows pointing outwards, representing a channel or a region of interest.

FIG. 2B

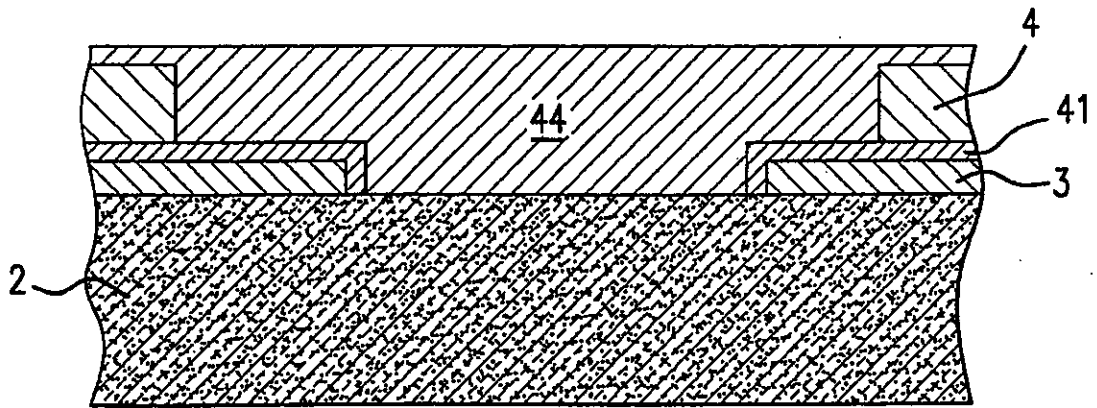


FIG. 2C

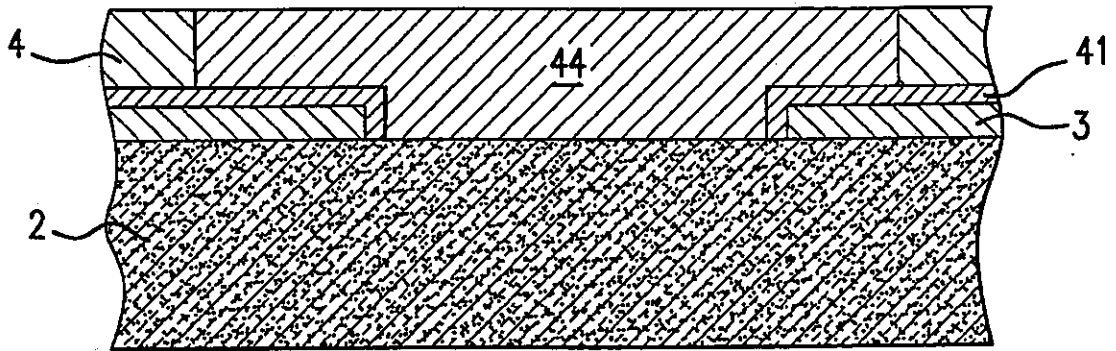


FIG. 2D

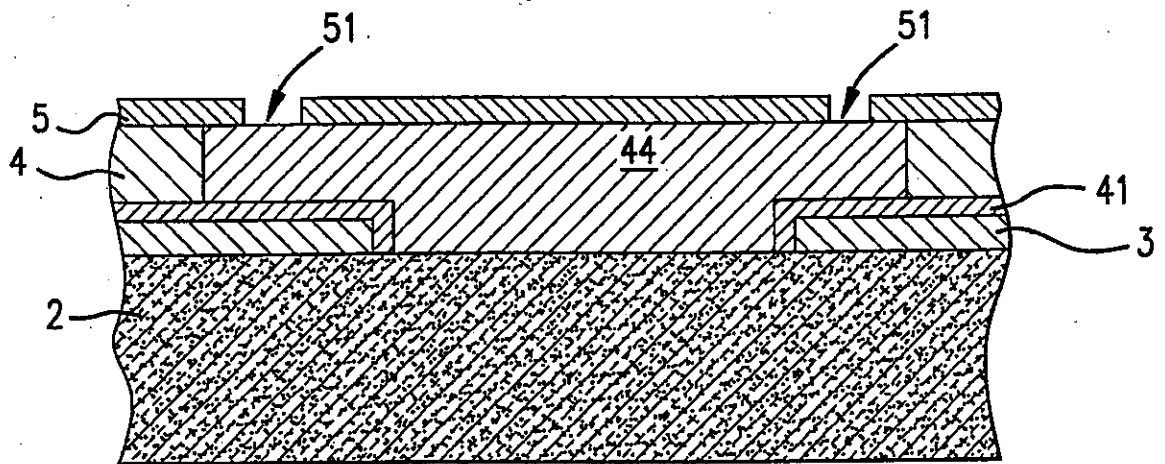


FIG. 2E

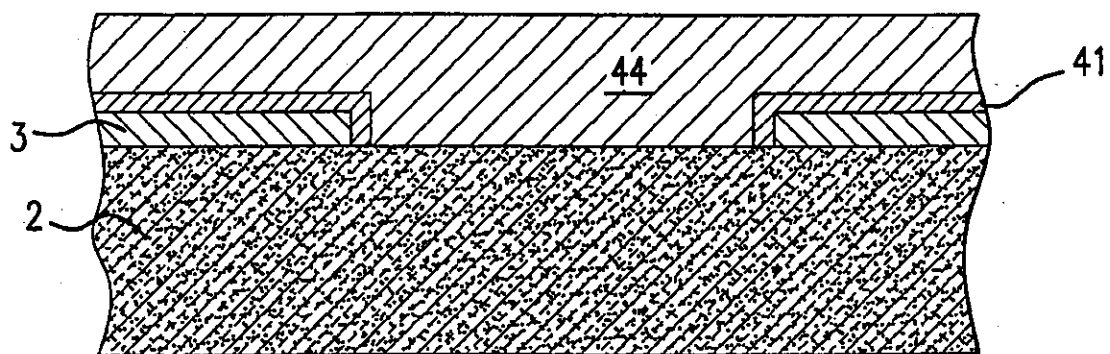


FIG.3A

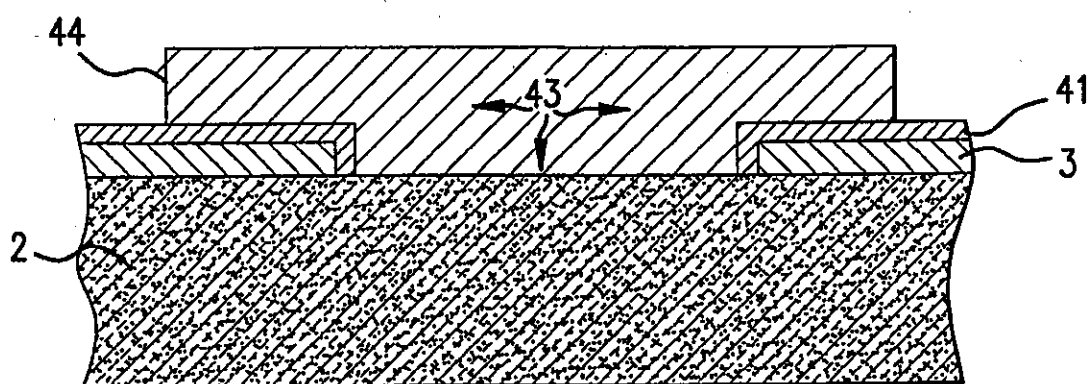


FIG.3B

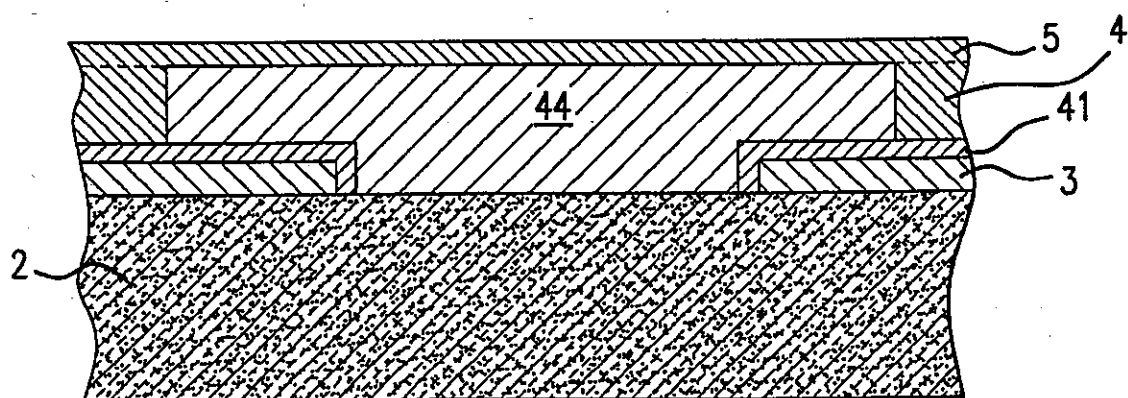


FIG.3C

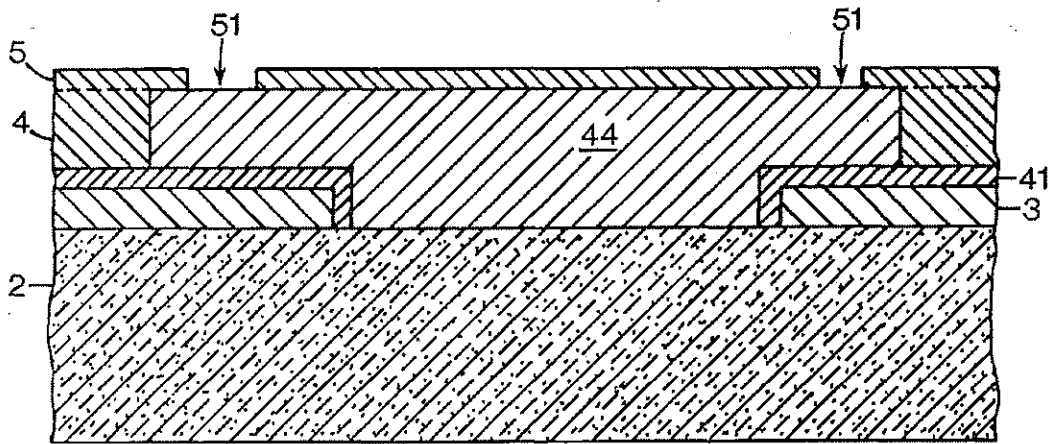


FIG. 3D

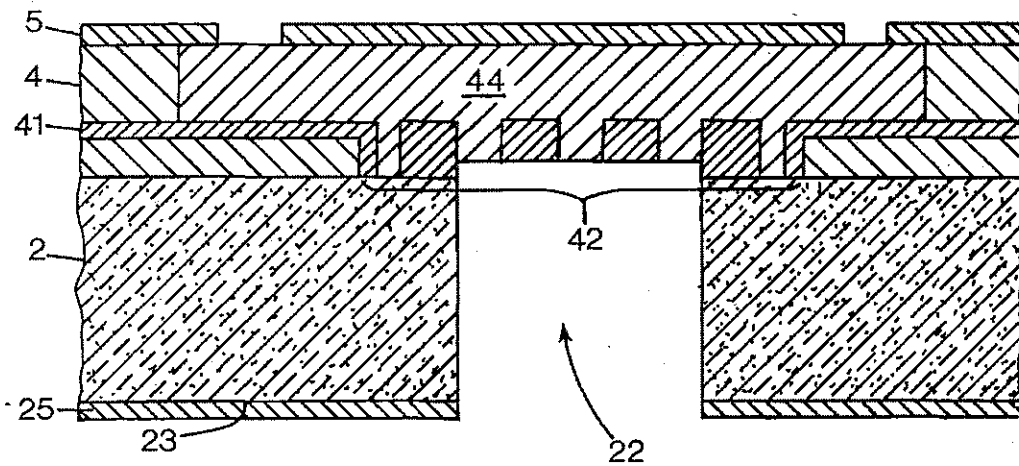


FIG. 4

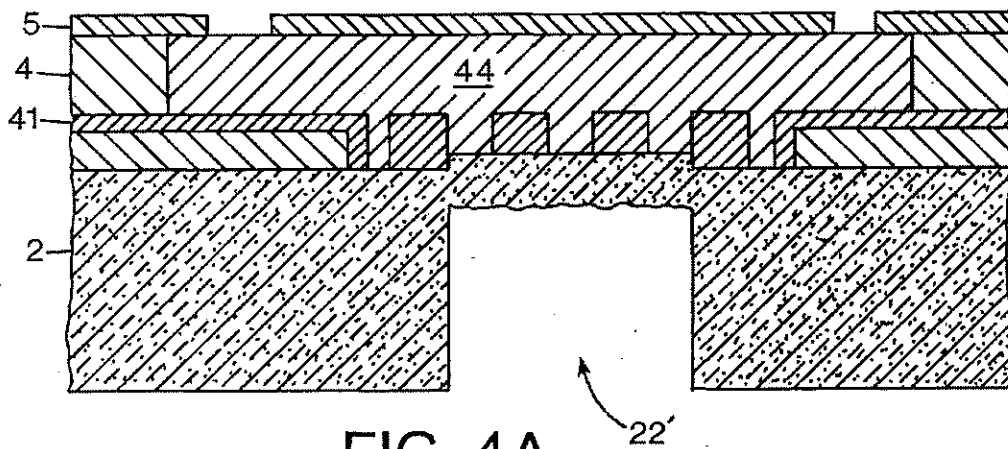


FIG. 4A

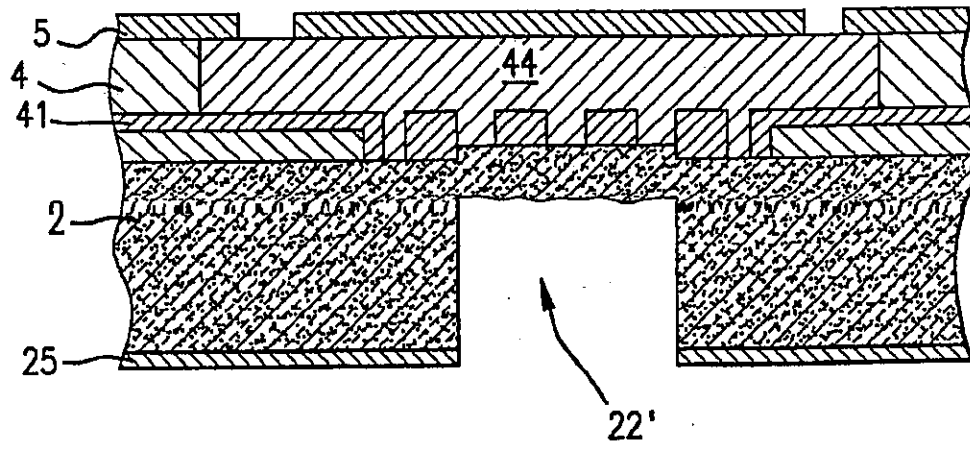
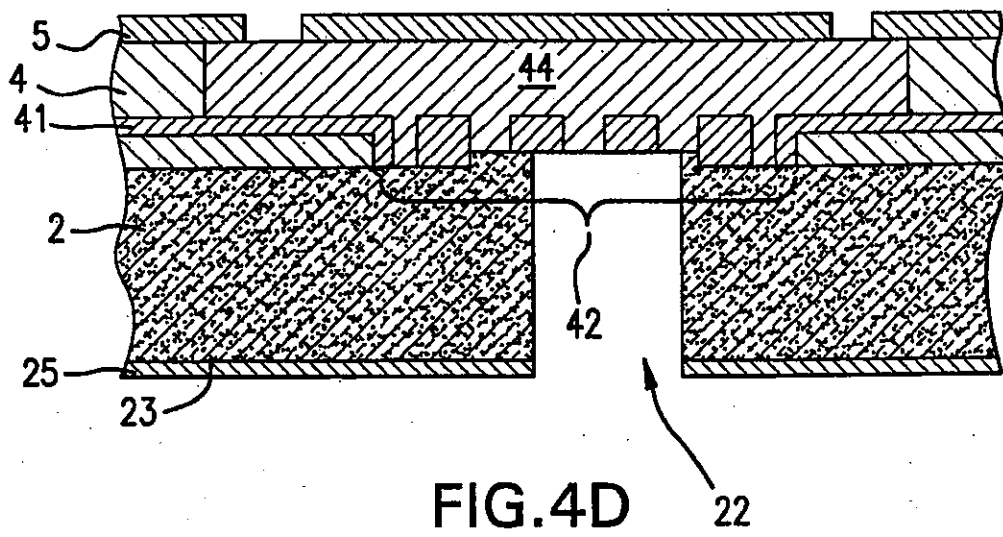
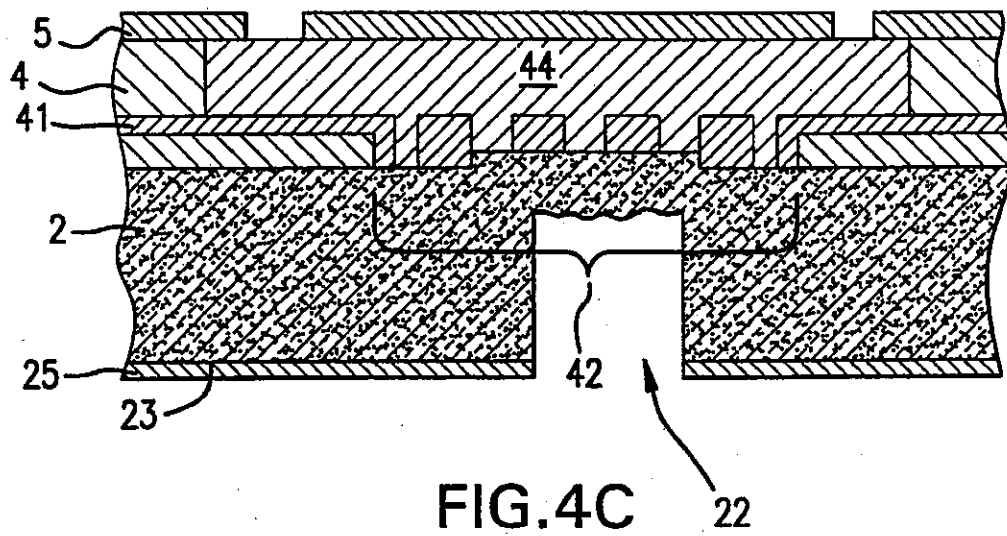


FIG.4B



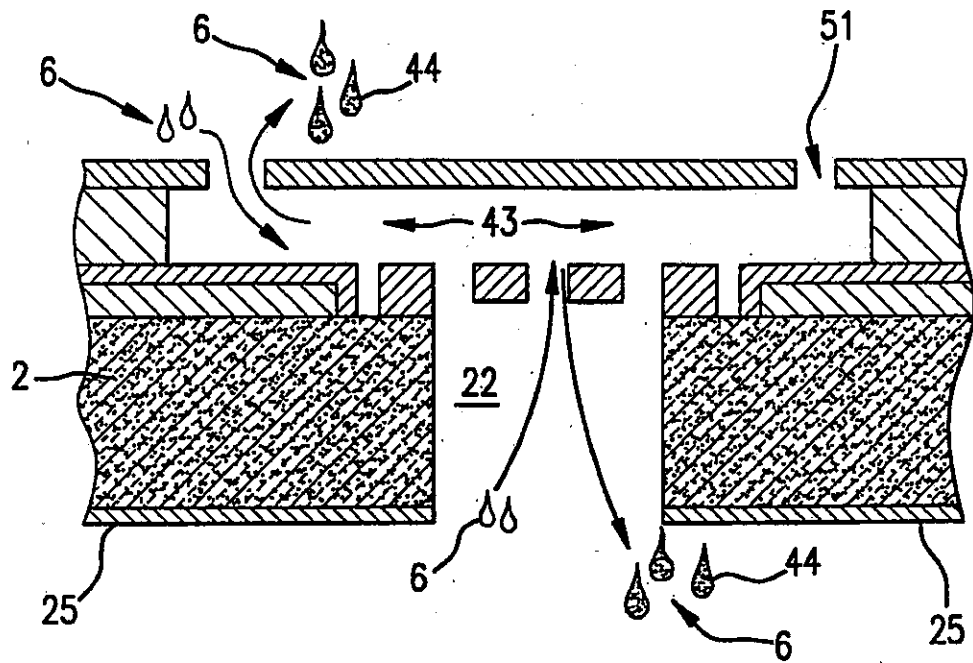


FIG. 5

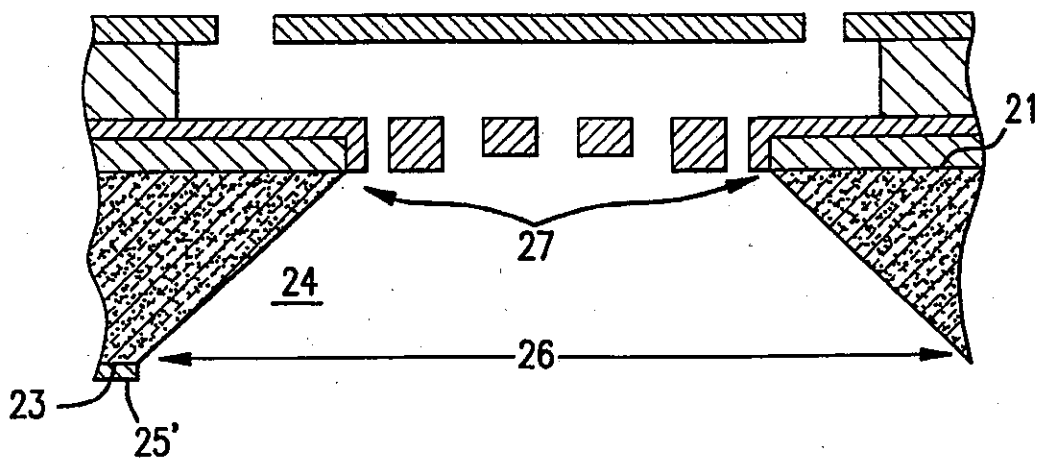


FIG. 6

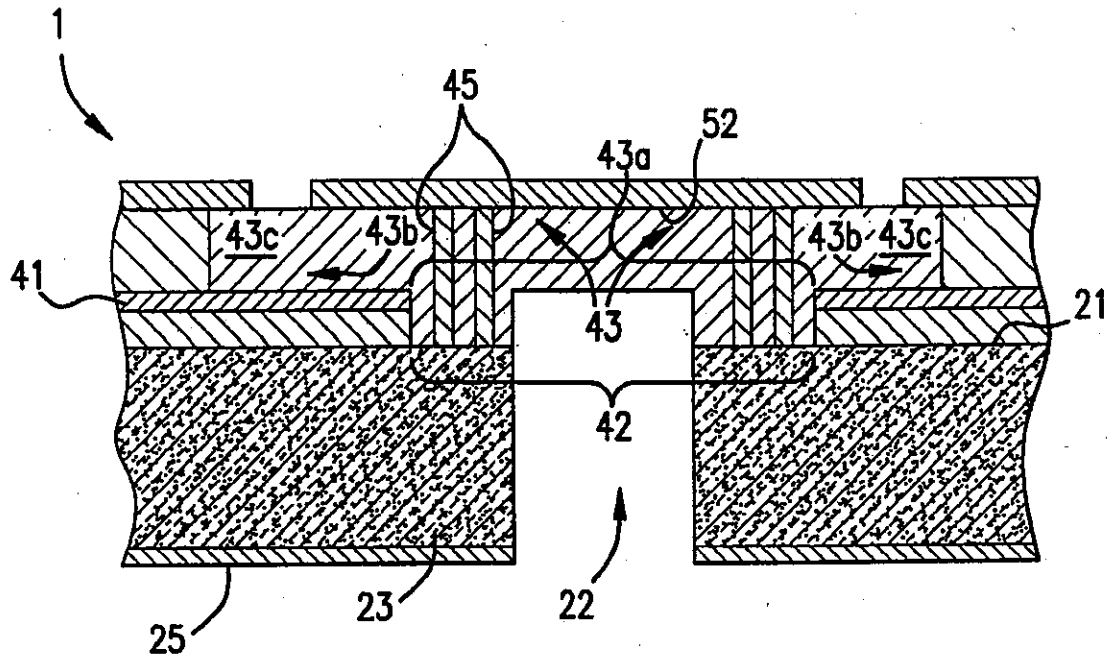


FIG. 7

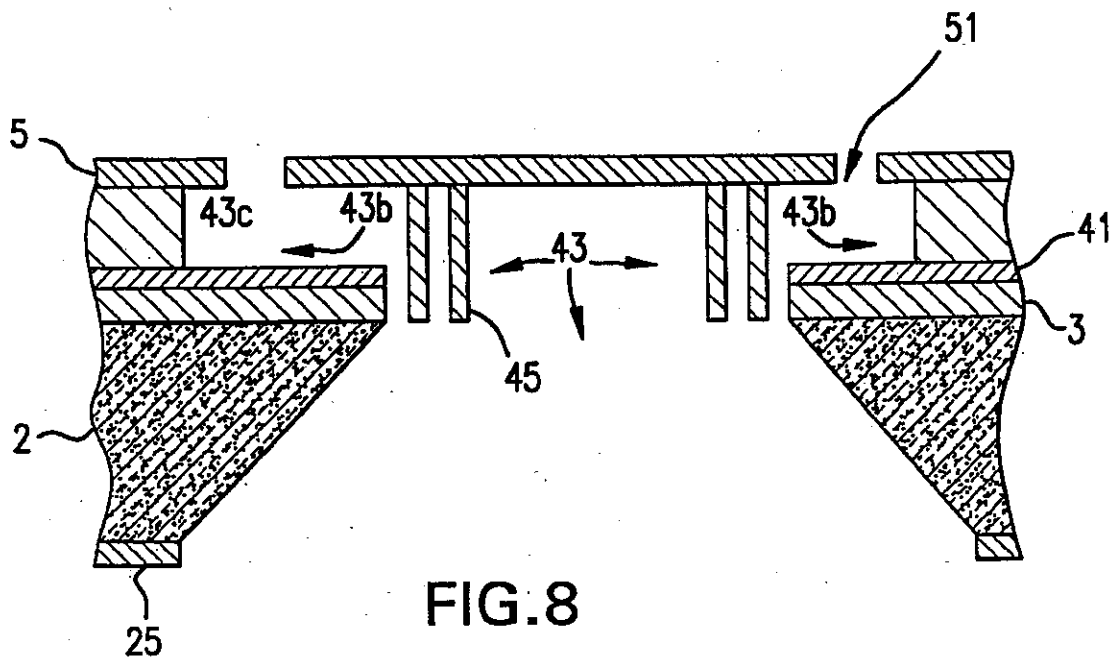


FIG. 8

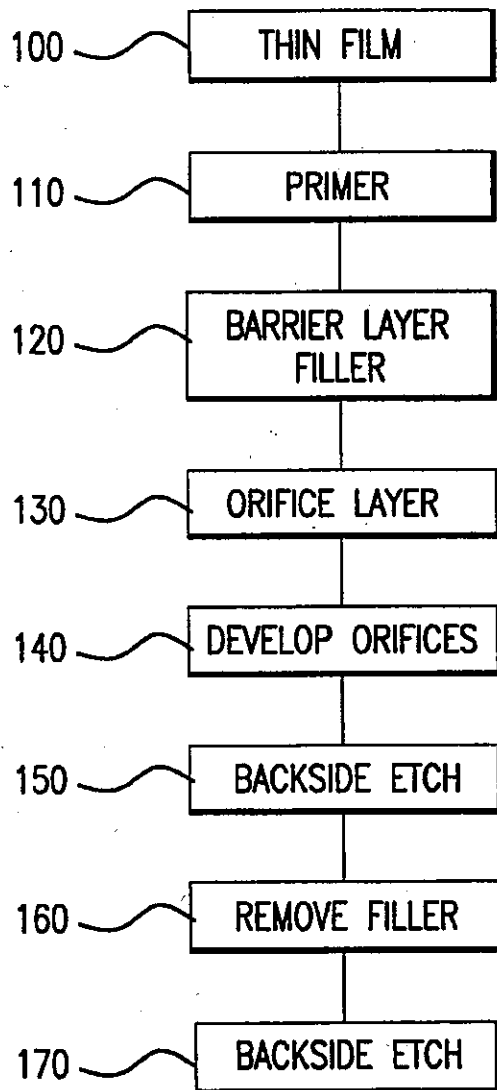


FIG.9

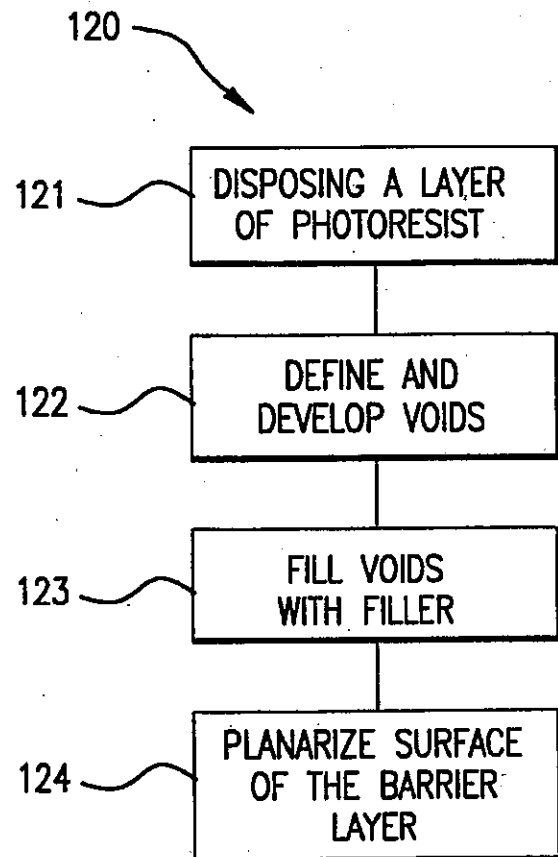


FIG.9A

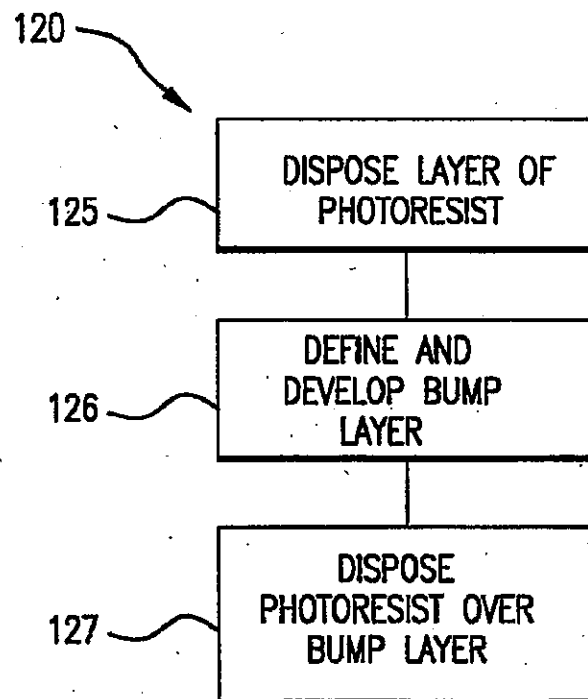


FIG.9B

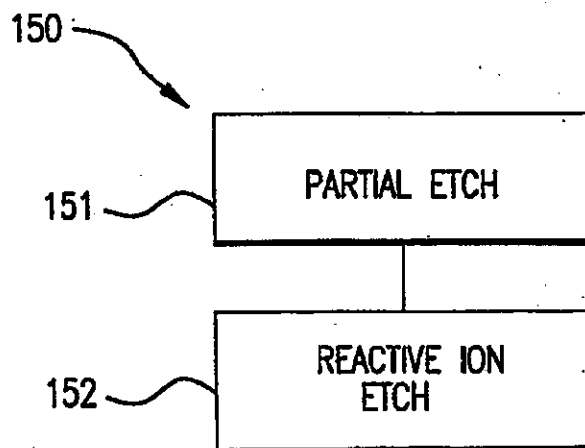


FIG.9C