

Method for synchronizing transmissions at a constant bit rate in ATM networks and circuit arrangements for carrying out the method

Abstract

The invention relates to a method for synchronizing transmissions at a constant bit rate in ATM networks and circuit arrangements for carrying out the method, in which a time stamp T_s is fed to the ATM cells which have been input on the receiver side, the data is output in a delayed fashion, the actual delay time ($T_A - T_s$) is compared with a prescribed desired value t_v , and a correcting variable, which adjusts the clock frequency of a time base (14) counter to the error variable, is generated by a controller (13) on the basis of the error variable $t_R = t_v - (T_A - T_s)$.
(Fig. 1)