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(54) IMPROVEMENTS IN OR RELATING TO SEMI-CONDUCTOR DEVICES

(71) We, FAIRCHILD CAMERA & INSTRUMENT CORPORATION of 464 Ellis Street, Mountain View, California 94040, United States of America, a corporation organised and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to charge coupled semiconductor devices and in particular to a charge coupled device wherein the spaced electrodes overlying an oxide layer on the semiconductor substrate are interconnected by resistive material.

W. S. Boyle and G. E. Smith described the basic concept of charge coupled semiconductor devices in an article published in the April 19, 1970 Bell System Technical Journal, page 587, entitled "Charge Coupled Semiconductor Devices". As described by Boyle and Smith, a charge coupled device consists of a metal-insulation-semiconductor (MIS) structure in which minority carriers are stored in a "spatially defined depletion region", also called a "potential well" at the surface of the semiconductor material. The charge is moved along the surface by moving the potential minimum. A paper on page 593 of the same volume of the Bell System Technical Journal by Amelio et al entitled "Experimental Verification of the Charge Coupled Device Concept" describes experiments carried out to demonstrate the feasibility of the charge coupled device concept.

As discussed by Boyle and Smith, charge coupled devices are potentially useful as shift registers, delay lines, and, in two dimensions, as imaging devices or display devices.

One problem with the construction of charge coupled devices is that the electrodes must be closely spaced. A typical spacing required is 0.1 mils or about 2.5 microns. Variations in spacing result in variations in

potential between electrodes. These variations influence the efficiency of the charge transfer along the surface of the semiconductor material.

The present invention improves the efficiency of transfer of charge along the surface of the semiconductor material and at the same time reduces the processing difficulties associated with the spacing of a plurality of electrodes along the surface of the insulation layer overlying the semiconductor material. The structure of this invention can be produced with a higher yield than that achieved with prior art charge coupled structures.

According to this invention a charge coupled device comprises a semiconductor substrate; an insulating layer formed on the surface of the substrate, and a plurality of electrodes formed on the surface of the insulating layer, said plurality of electrodes being spaced from each other by resistive material. In one embodiment, the electrodes are formed of metal and a resistive material is placed between the electrodes. In another embodiment, the electrodes are formed from heavily doped polycrystalline silicon while the resistive material is substantially intrinsic polycrystalline silicon.

Surprisingly, the structure of this invention increases the allowable spacing between electrodes without any decrease in the efficiency with which charge is transferred from beneath one electrode to an adjacent electrode. The resistive material between electrodes ensures that there are no potential barriers between electrodes inhibiting charge transfer.

Figure 1 shows isometrically the structure of an embodiment of this invention.

Figure 2 shows a cross-section of a portion of the structure of another embodiment of this invention constructed using polycrystalline silicon; and

Figure 3 shows in cross-section an alternative structure constructed according to this invention.

A charge coupled device 10 (Fig. 1) com-

prises a semiconductor substrate 11 on one surface of which is formed an insulating layer 12. For convenience in describing the invention, but without limitation to the general applicability to the concepts described herein, substrate 11 will be described as silicon and insulating layer 12 will be described as silicon dioxide. However, it should be understood that any semiconductor material capable of sustaining a surface charge together with an appropriate dielectric layer or layers 12 can be used with this invention.

Overlying the oxide layer 12 are a plurality of electrodes 13a through 13g separated by a multiplicity of regions of resistive material 14a through 14f.

As discussed in the above cited article by Amelio et al a variety of oxides exhibit surface charge storage. The best results obtained by Amelio et al were obtained with a "dry oxide 1200 angstroms thick grown in oxygen at 1100°C" (Amelio et al, April 1970 BSTJ, page 549). Such oxides are well known in the art and thus the method of forming the oxide on substrate 11 will not be discussed in detail.

Electrodes 13a through 13g are formed on the top surface of oxide 12. Separating these electrodes are portions of thin film resistive material 14a through 14f. Typical electrode spacings in the prior art are approximately 0.1 mils. Using resistive material between electrodes, the applicants obtained charge coupled devices which operated satisfactorily with spacings between electrodes of up to 0.4 mils or 10 microns.

An embodiment of this invention was produced by forming a layer 13 (Fig. 2) of polycrystalline silicon over oxide 12. Layer 13 was then masked to leave exposed selected portions of the polycrystalline silicon corresponding to the electrodes desired to be formed on the surface of the oxide. Then, a selected dopant was diffused into the exposed regions of polycrystalline silicon to form conductive electrodes 13a through 13c. By controlling the particular dopant diffused into the exposed polycrystalline silicon material, the work function difference between the gate electrodes and the underlying substrate is controlled. Resistance regions of substantially intrinsic polycrystalline silicon, such as regions 14a through 14c, separate the doped polycrystalline silicon electrodes.

If desired, a final dielectric layer 15 is placed over layer 13. This dielectric layer, which might, for example, comprise silicon nitride, seals the surface of, and protects, the underlying polycrystalline material 13.

A structure built in accordance with this invention had a spacing between the electrodes increased by a factor of four over the spacing disclosed in the above cited article by Amelio et al. These structures exhibited

extremely fast transfer of charge. The reason for this is not fully understood.

It was noted that in constructing devices without the resistive material between the electrodes, yields were significantly lower than when devices containing resistive material between the electrodes were constructed.

A typical resistance of the material between each electrode is greater than 100 megohms. The resulting extremely high resistance results in devices constructed in accordance with this invention having very low power dissipation. Typical dissipation for an 8-bit three-phase shift register is about three (3) microwatts. This calculation assumes 10 volts difference between all electrodes at all times. In practice, however, delayed impulses are applied to the electrodes and the total power consumption by such a device is less than the above figure by a factor of approximately 2/3.

The device constructed in accordance with this invention had the following dimensions (refer to Fig. 1):

$X_o = 1,000$ angstroms
 $L_M = 0.6$ mils
 $L_G = 0.4$ mils
 $Z_o = 2$ mils

The thickness of the electrodes and the resistive material of the embodiment shown in Fig. 2 is typically 0.5 microns.

In a charge coupled device, the charge stored beneath one electrode is transferred to an adjacent electrode by shifting the potential well from the first electrode to the adjacent electrode. The transfer of minority carriers can be achieved only when there is no potential barrier along the interface between the semiconductor material and the insulation between two adjacent electrodes. While in the prior art this elimination of potential barriers was accomplished by placing the two electrodes close together, the close spacing of electrodes made the masking step difficult. The resistive material of this invention between the electrodes ensures that the potential distribution on the insulation surface between these electrodes is more nearly linear than with prior art structures. Thus there will be no potential barrier along the insulation-semiconductor material interface even with relatively large electrode spacings.

The sheet resistance of the thin film resistor material between the electrodes is large in order to insure small leakage current.

Fig. 3 shows an alternative embodiment of this invention. As in the embodiment of Figures 1 and 2, dielectric 12 is formed on semiconductor material 11. A layer of resistive material 14 is then formed on, and adheres to dielectric 12. Next, a metal layer (not shown in Fig. 3) is formed on the top of resistive material 14. This layer is masked

to protect those portions of metal layer 13 to be retained on resistive material 14 as electrodes. Then the exposed metal is removed, typically by etching. The resulting structure comprises metal electrodes 13a through 13d overlying resistive material 14 on top of dielectric 12.

WHAT WE CLAIM IS:—

1. A charge coupled device comprising:
a semiconductor substrate;
an insulating layer formed on the surface of the substrate; and
a plurality of electrodes formed on the insulating layer, said plurality of electrodes being spaced from each other by resistive material.
2. Structures as in claim 1 wherein said resistive material is polycrystalline silicon.
3. Structure as in claim 2 wherein said electrodes are selectively doped regions of

polycrystalline material separated by intrinsic polycrystalline material.

4. Structure as in claim 3 wherein said substrate is silicon and said insulation layer is silicon dioxide.

5. A charge coupled device comprising:
a semiconductor substrate;
an insulating layer formed on the surface of said substrate;

a layer of resistive material formed on, and adhering to, said insulating layer; and
a plurality of spaced electrodes formed on the top surface of said resistive material.

6. A charge coupled device substantially as herein described with reference to Figures 1 and 2 or 3 of the accompanying drawing.

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