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TITLE OF THE INVENTION

Manufacturing method of semiconductor devices

FIELD OF THE INVENTION

This invention relates to manufacturing method of semiconductor integrated circuits having built-in capacitor in which ferroelectric material is used as capacitance insulation film; especially to fine pattern dry etching process to be applied to Pt electrodes of said capacitor.

BACKGROUND OF THE INVENTION

In the midst of general trends towards finer structuring of semiconductor devices, development activities have been remarkable in the field of microcomputers having capacitors of high dielectric constant materials which is effective to reduce unnecessary radiation, or electro-magnetic interference, and in the field of non-volatile RAM having built-in ferroelectric capacitors which facilitates low-voltage operation and high read/write speed. The ferroelectric materials are made mainly of metal oxide, and contains substantial amount of very reactive oxygen. In forming a capacitor with such dielectric film, material for its electrodes must be least reactive; precious metals such as Pt, palladium, etc. must be used.

FIG. 9 shows typical structure of capacitor in a semiconductor device having built-in dielectric capacitor. Where, 1a denotes top electrode, 2a capacitance insulation film, 3a bottom electrode, 4 underlayer, 7 contact hole, 8 inter

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insulation layer (oxide layer) and 9 wiring.

In the above mentioned structure, bottom electrode 3a is made larger than top electrode 1a; the reason is to provide contacting individually at two points, viz. top electrode 1a and bottom electrode 3a, with the upper wiring 9.

Etching process to form the capacitor consists of that on Pt top electrode layer and dielectric film, and that on Pt bottom electrode layer 3; wherein, etching on Pt top electrode layer and dielectic film must be conducted at a speed different from that on Pt bottom electrode.

The Pt etching has been conducted by means of wet etch with aqua regia, ion milling with Ar gas, or by other means. However, the nature of both wet etching and ion milling is isotropic etching, which means the grade of precision is not high enough for the fine pattern processing. Especially, ion milling bears with it a drawback that there is not much difference in etching speed between Pt and underlayer material.

In order to overcome the above mentioned drawback, active research and development efforts have been made in Pt fine pattern processing by means of dry etching; where, as etching gas, use of Cl_2 and HBr are reported (Extended Abstracts, Autumn Meeting 1991, The Japan Society of Applied Physics, 9p-ZF-17, p516; Extended Abstracts, Spring Meeting 1993, The Japan Society of Applied Physics, 30a-ZE-3, p577, and others). Now in the following, explanation will be made on dependence of Pt etching

speed to high frequency (RF) electric power when Cl_2 gas is used as etching gas.

FIG. 10 shows dependence of Pt etching speed, and of Pt/resist etching speed ratio to RF power, with Cl_2 gas as etching gas. Where, horizontal axis denotes RF power, left vertical axis Pt etching speed, and right vertical axis Pt/resist etching speed ratio.

Facility used for the etching is a magnetron reactive ion etching (RIE) mode dry etcher.

Etching conditions are: Cl_2 gas flow 20 SCCM, gas pressure 1 Pa. Wafer temperature during etching is below 20℃ because its back surface is cooled with He.

FIG. 10 exhibits a trend that Pt etching speed is increased from 10 nm/min. to 100 nm/min. when RF power is raised from 200W to 600W.

Pt/resist etching speed ratio, when RF power is raised from 200W to 600W, also shows upward trend from 0.2 to 0.3; however, the etching speed ratio remains very low. The above quoted papers also report similar results in the dependence of Pt etching speed to RF power when Cl_2 gas is used.

In addition, the above quoted papers describe about a case where HBr gas was used as etching gas; in which case, according to the papers, Pt etching speed was reported to be 120 nm/min.

In such conventional cases where single substance gas such as Cl_2 or HBr is used as etching gas, Pt etching speed is very

low; which means it takes very long time to etch Pt of a required thickness (several hundreds nm), therefore, a drawback of deteriorated throughput of production facilities.

Furthermore, the prolonged etching time is liable to cause a problem of etched resist layer during etching time. If resist layer is made thicker, it affects grade of definition, making formation of fine pattern very difficult.

A possibility for increasing Pt/resist etching speed ratio is to add a gas containing carbon component and conducts etching by means of plasma polymerization while piling up carbon layer. This procedure, however, causes piling up of carbon layer within reaction chamber, which becomes source of particle generation. This necessitates frequent maintenance servicing of facilities, making operating efficiency poor.

SUMMARY OF THE INVENTION

. Objective of this invention is to offer a new manufacturing method of semiconductor devices, wherein Pt etching speed is increased, hence, throughput of production facilities can be improved.

In order to implement the objective this invention features in such semiconductor device manufacturing method, wherein insulation layer, bottom electroe Pt layer, dielectric film and top electrode Pt layer are provided on top of a substrate having already-completed circuit elements and wiring, and then, capacitor is formed by selectively dry etching bottom electrode

Pt layer after selectively dry etching top electrode Pt layer and dielectric film;

it comprises process to dry etch Pt layer consisting bottom electrode or top electrode, wherein, either Pt layer is dry etched while a compound of Pt and S is being composed, or first Pt and S compound is made and then the Pt compound is dry etched;

it uses a gas containing S component as etching gas for Pt etching, or an etching gas containing S component as additive gas; and

it implants S into Pt layer, before Pt dry etching process, by means of ion implantation to compose S and Pt compound, and then dry etch the Pt compound thus composed.

Therefore, according to this invention, Pt and S compound is composed during etching. Because boiling point of this compound is far lower than that of Pt, etching speed for Pt layer can be increased to the improved throughput of manufacturing facilities. Pt etching time can be shortened, and resist etching prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1(A)~(D) illustrates formation of capacitor in an embodiment of this invention.

FIG. 2 is characteristics chart that shows dependence of Pt etching speed and Pt/resist etching speed ratio to RF power in Embodiment 1 of this invention, with S_2Cl_2 gas as etching gas.

FIG. 3 is characteristics chart that shows dependence of Pt etching speed to mixing ratio of etching gas between Cl_2 gas and

S_2Cl_2 gas in Embodiment 2 of this invention.

FIG. 4 is characteristics chart that shows dependence of Pt etching speed and Pt/resist etching speed ratio to RF power in Embodiment 3 of this invention; where, etching gas was HBr gas, additive gas was H_2S gas.

FIG. 5 is characteristics chart that shows dependence of Pt etching speed to mixing ratio between HBr gas and H_2S gas, in Embodiment 3 of this invention.

FIG. 6(A)-(D) illustrate formation of capacitor in Embodiment 4 of this invention.

FIG. 7 is characteristics chart that shows dependence of Pt etching speed to RF power in Embodiment 4; where, S was implanted into Pt by means of ion implantation to compose S and Pt compound, and then Pt is etched with Cl_2 gas.

FIG. 8 is Pt/S alloy phase diagram.

FIG. 9 shows cross-section of typical capacitor manufactured by conventional semiconductor device manufacturing method.

FIG. 10 is characteristics chart that shows dependence of Pt etching speed and Pt/resist etching speed ratio to RF power in the above manufacturing method, where, single substance Cl_2 gas was used as etching gas.

DESCRIPTION OF PREFERRED EMBODIMENTS

In the following, explanation will be given on an embodiment of this invention referring to FIGs; where, same part as the conventional structure as shown in FIG. 9 is given the same

numeral.

In FIG. 1(A)-(D), 1 denotes Pt layer for top electrode, 1a top electrode; 2 dielectric film, 2a capacitance insulation film, 3 Pt layer for bottom electrode, 4 insulation underlayer, 5 and 6 resists. For the sake of simplifiaction, regions of circuit elements on substrate do not appear in the drawings.

On underlayer 4 provided over silicon semiconductor substrate, pile up 200nm thick Pt layer 3 for bottom electrode; on Pt layer 3 for bottom electrode pile up 180nm thick dielectric film 2; on dielectric film 2 pile up 200nm thick Pt layer 1 for top electrode.

Now, explanation will be made on process to form capacitor out of multi-layered structure thus fabricated.

First, place resist 5 on Pt layer 1 for top electrode, for the purpose of making top electrode 1a and capacitance insulation layer 2a, as shown in FIG. 1(A). Next, as shown in FIG. 1(B), etch down Pt layer 1 for top electrode and dielectric film 2 to form top electrode 1a and capacitance insulation layer 2a; and stop etching when surface of Pt layer 3 for bottom electrode is exposed. Then, place resist 6 to entirely cover top electrode 1a and capacitance insulation layer 2a, as shown in FIG. 1(C). Finally, etch down Pt layer 3 for bottom electrode to form bottom electrode 3a, as shown in FIG. 1(D).

As Embodiment 1 to manufacture capacitor of above mentioned structure, S_2Cl_2 gas is used as Pt etching gas.

FIG. 2 shows Pt etching speed and Pt/resist etching speed ratio under a changing RF power in this Embodiment.

Comparison between FIG. 2, characteristics of in this Embodiment, and FIG. 10, those in conventional manufacturing method, clarifies that Pt etching speed in this Embodiment is twice as high, and Pt/resist etching speed ratio rises from 0.4 to 0.5 along with the increased RF power from 200W to 600W. Furthermore, Pt/resist etching speed ratio hsa been almost doubled.

FIG. 3 shows, as Embodiment 2, dependence of Pt etching speed to mixing ratio of etching gas when Cl_2 gas and S_2Cl_2 gas are mixed and used as etching gas. Horizontal axis denotes gas mixing ratio, vertical axis Pt etching speed.

Facility used is a magnetron RIE mode dry etcher.

Etching conditions are: mixing ratio of $S_2Cl_2/(S_2Cl_2+Cl_2)$ etching gas is varied, RF power 600W, gas pressure 1 Pa. Wafer temperature during etching is maintained below 20℃ by means of wafer back surface cooling.

FIG. 3 clarifies that Pt etching speed follows the upward trend from 100 nm/min. to 200 nm/min. when mixing ratio of etching gas is changed from 100% Cl_2 gas to 100% S_2Cl_2 gas.

According to this Embodiment case, Pt etching speed can be increased by the use of an etching gas containing S component, and throughput of production facilities can be raised, and Pt/resist etching speed ratio can be made higher.

In this Embodiment case, use of sulfur chloride gas such as S_2Cl_2 gas or use of Cl_2 and S_2Cl_2 mixed gas were exampled as etching gas. However, as the gas containing S component, sulfur fluoride gas such as SF_6 gas or S_2F_2 gas may be used to obtain same results.

As Embodiment 3, a case when H_2S gas is added to etching gas in Pt etching process will be explained referring to FIGs.

FIG. 4 shows dependence Pt etching speed and Pt/resist etching speed ratio to RF power when HBr gas is used as etching gas, and H_2S gas as additive gas. Horizontal axis denotes RF power, left vertical axis Pt etching speed, right vertical axis Pt/resist etching speed ratio.

Facilities used is a magnetron RIE mode dry etcher.

Etching conditions are: HBr gas flow 20 SCCM, H_2S gas flow 10 SCCM, gas pressure 1 Pa. Wafer temperature during etching is maintained below 20℃ by means of wafer back surface cooling.

FIG. 4 clarifies that Pt etching speed follows the upward trend from 20 nm/min. to 200 nm/min. when RF power is increased from 200W to 600W; as compared with conventional case shown in FIG. 10, Pt etching speed is almost doubled. Pt/resist etching speed ratio follows the upward trend from 0.4 to 0.5 as RF power increases from 200W to 600W. As compared with the case when Cl_2 gas was used as Pt etching gas, the etching speed ratio with resist is almost doubled.

FIG. 5 shows dependence of Pt etching speed to mixing ratio

of gas when HBr gas is used as etching gas, H_2S gas as additive gas. Horizontal axis denotes gas mixing ratio, vertical axis Pt etching speed.

Facility used is a magnetron RIE mode dry etcher. Etching conditions are: $H_2S/(H_2S+HBr)$ mixing ratio is varied, RF power 600W, gas pressure 1 Pa. Wafer temperature during etching is maintained below 20℃ by means of wafer back surface cooling.

FIG. 5 clarifies that Pt etching speed reaches the fastest, 200 nm/min., when gas mixture ratio is around 30%.

According to this Embodiment case, Pt etching speed can be increased by the use of a gas containing S component as additive gas, and throughput of production facilities can be raised, and Pt/resist etching speed ratio can be made high..

In this Embodiment case, use of H_2S gas as additive gas was exampled. However, as the gas containing S component, SO_2 gas may be used to obtain same results.

Next, as Embodiment 4 of this invention, explanation will be made on a case where S is implanted into Pt by means of ion implantation to compose S and Pt compound; and then Pt is dry etched.

FIG. 6(A)~(D) illustrates formation of capacitor in this Embodiment case; where, 1 is Pt layer for top electrode, 1a top electrode, 2 dielectric film, 3 Pt layer for bottom electrode, 4 underlayer made of insulation layer, 5 resist.

On underlayer 4 provided over silicon semiconductor

substrate, pile up 200nm thick Pt layer 3 for bottom electrode; on Pt layer 3 for bottom electrode pile up 180nm thick dielectric film 2; on dielectric film 2 pile up 200nm thick Pt layer 1 for top electrode.

Now, explanation will be made on process to form capacitor out of multi-layered structure thus fabricated.

First, place resist 5 on Pt layer 1 for top electrode, as shown in FIG. 6(A). Next, as shown in FIG. 6(B), implant S ion into Pt layer 1 for top electrode by means of ion implantation to compose a compound of Pt and S in the region to be etched off, as shown in FIG. 6(C). In this stage, S is not implanted into dielectric film 2. Then, as FIG. 6(D) illustrates, etch off the Pt and S compound.

FIG. 7 shows dependence of Pt etching speed to RF power, wherein, S is implanted into Pt by means of ion implantation to compose S and Pt compound, and then Cl_2 gas is used as etching gas. Horizontal axis denotes RF power, vertical axis Pt etching speed.

Facilities used is a magnetron RIE mode dry etcher. Ion implantation conditions are: acceleration voltage 600KeV, dope quantity 5×10^{15}atm/cm^2. Etching conditions are: Cl_2 gas flow 20 SCCM, gas pressure 1 Pa. Wafer temperature during etching is maintained below 20℃ by means of wafer back surface cooling.

FIG. 7 clarifies that Pt etching speed follows upward trend from 15 nm/min. to 150 nm/min. when RF power is raised from 200W

to 600V.

As compared with FIG. 10, conventional case, Pt etching speed is about 1.5 times as high.

According to this Embodiment case, etching speed of Pt layer 1 for top electrode can be increased by first implanting S into Pt layer 1 for top electrode by means of ion implantation to compose S and Pt compound, and then dry etching the compound. By so doing, throughput of production facilities can be improved.

Now, regarding a case, wherein a gas containing S component is used as etching gas and a gas containing S component is used as additive gas, and another case, wherein Pt is dry etched while Pt and S compound is being composed, or Pt and S compound is first composed and then Pt is dry etched, explanation will be made on the mechanism how Pt etching speed is increased.

FIG. 8 is Pt/S alloy phase diagram, in which one will see that by mixing very small quantity of S into Pt, it starts evaporating at 1175℃.

It is known that boiling point of Pt is as high as 3804℃. However, as mentioned above, boiling point of Pt is lowered by mixing a very small quantity of S into Pt.

S_2Cl_2 gas and S_2F_2 gas, both are S-containing gas, have large S/X ratio (X=Cl, F) and easily pile up S when dissociated in plasma.

Therefore, when S-containing gas is used as etching gas and S-containing gas is used as additive gas, the S component

dissociated in plasma reacts with Pt to compose a low boiling point compound.. Because of this, Pt etching speed is increased as compared with the case when Cl_2 gas is used as etching gas.

So, in the process where Pt layer 1 for top electrode and dielectric film 2 are to be etched, conduct etching under relatively slow Pt etching conditions, and stop it as soon as Pt layer 3 for bottom electrode is exposed. In the next process where Pt layer 3 for bottom electrode is to be etched, conduct etching under fast Pt etching conditions. In this way, required capacitor structure may be formed.

As the above mentioned Embodiments clarified, the process according to this invention uses a S-containing gas as Pt etching gas, or a gas containing S component as additive gas to change Pt for electrode into low boiling point S/Pt compound; and conducts etching after compound is composed;
therefore, Pt etching speed can be increased. Etching speed ratio with respect to resist can also be increased.

This invention, therefore, implements new manufacturing method of semiconductor devices which provides high processing accuracy and high throughput of production facilities.

WE CLAIM:

1. Semiconductor device manufacturing method, wherein capacitance element is formed by:

first providing, on top of a substrate having already-completed circuit element and wiring, etc., insulation layer, bottom electrode Pt layer, dielectric film and top electrode Pt layer, and then, selectively dry etching said top electrode Pt layer and dielectric film, thereafter, selectively dry etching bottom electrode Pt layer; and in conducting dry etching on said Pt consisting bottom electrode or top electrode,

proceeding dry etching work while composing a Pt and S compound, or, first making a Pt and S compound and then dry etch the compound thus composed.

2. Semiconductor device manufacturing method, wherein capacitance element is formed by:

first providing, on top of a substrate having already-completed circuit elements and wiring, etc., insulation layer, bottom electrode Pt layer, dielectric film and top electrode Pt layer, and then selectively dry etching said top electrode Pt layer and dielectric film, thereafter, selectively dry etching bottom electrode Pt layer; and in conducting dry etching on said Pt consisting bottom electrode or top electrode,

using a gas containing S component as etching gas.

3. Semiconductor device manufacturing method according to Claim 2, wherein the gas containing S component is one member selected from the group consisting of sulfur fluoride gas and sulfur chloride gas.

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4. Semiconductor device manufacturing method, wherein capacitance element is formed by:

first providing, on top of a substrate having already-completed circuit elements and wiring, etc., insulation layer, bottom electrode Pt layer, dielectric film and top electrode Pt layer, and then selectively dry etching said top electrode Pt layer and dielectric film, thereafter, selectively dry etching bottom electrode Pt layer; and in conducting dry etching on said Pt consisting bottom electrode or top electrode,

using a gas containing S component as additive gas to Pt etching gas.

5. Semiconductor device manufacturing method according to Claim 4, wherein the additive gas is at least one member selected from the group consisting of sulfur fluoride, sulfur chloride, H_2S and SO_2.

6. Semiconductor device manufacturing method, wherein capacitance element is formed by:

first providing, on top of a substrate having already-completed circuit element and wiring, etc., insulation layer, bottom electrode Pt layer, dielectric film and top electrode Pt layer, and then selectively dry etching said top electrode Pt layer and dielectric film, thereafter selectively dry etching bottom electrode Pt layer; and before conducting dry etching on said Pt consisting bottom electrode or top electrode,

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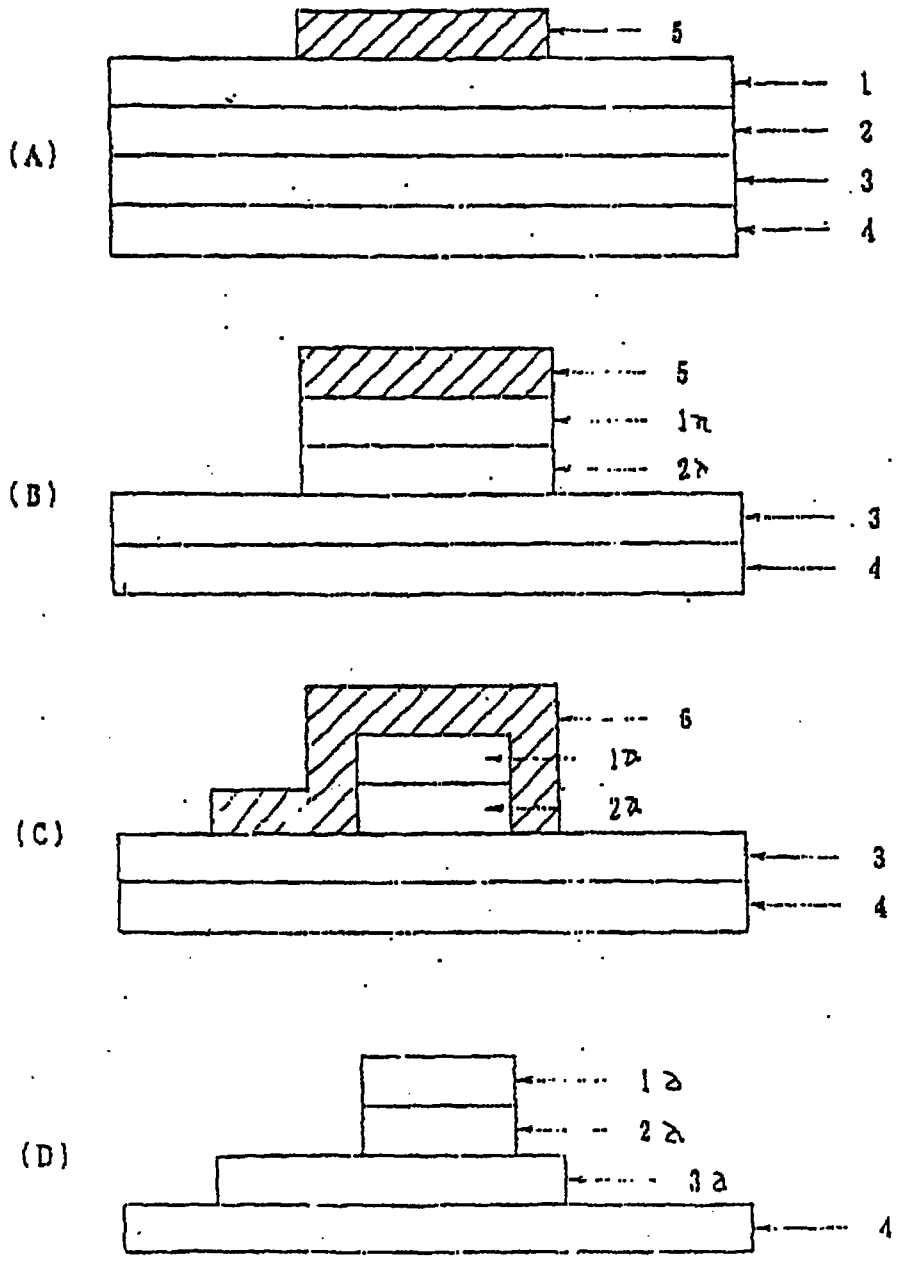
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implanting S into Pt by means of ion implantation to compose S and Pt compound, and then dry etch the Pt compound thus composed.

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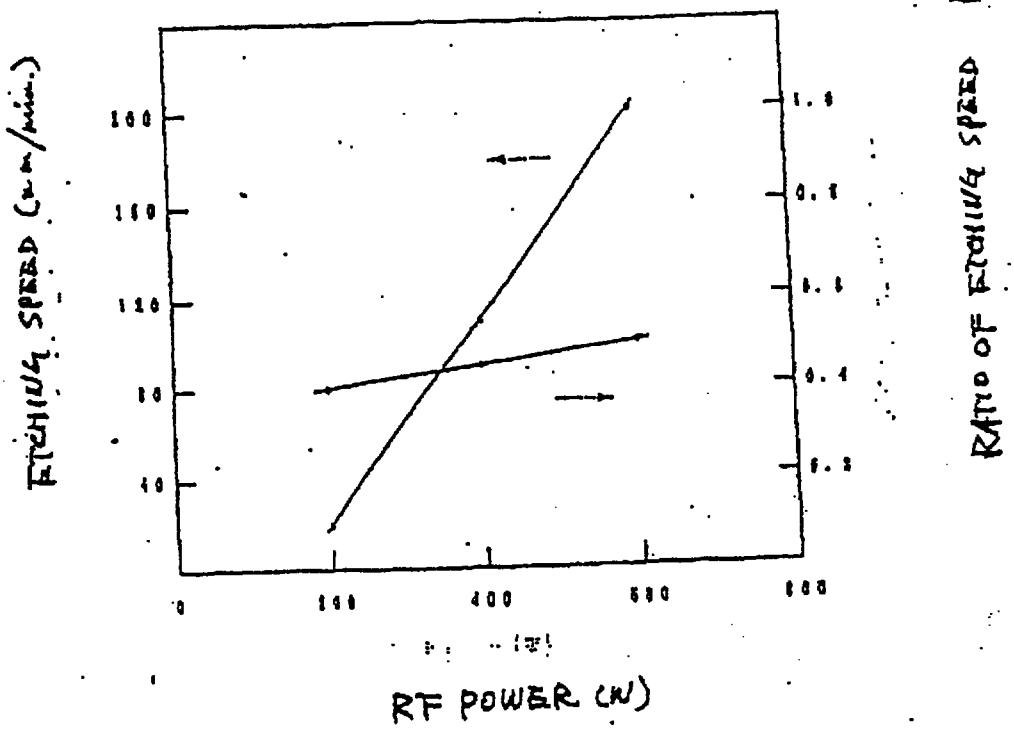
FIG. 1



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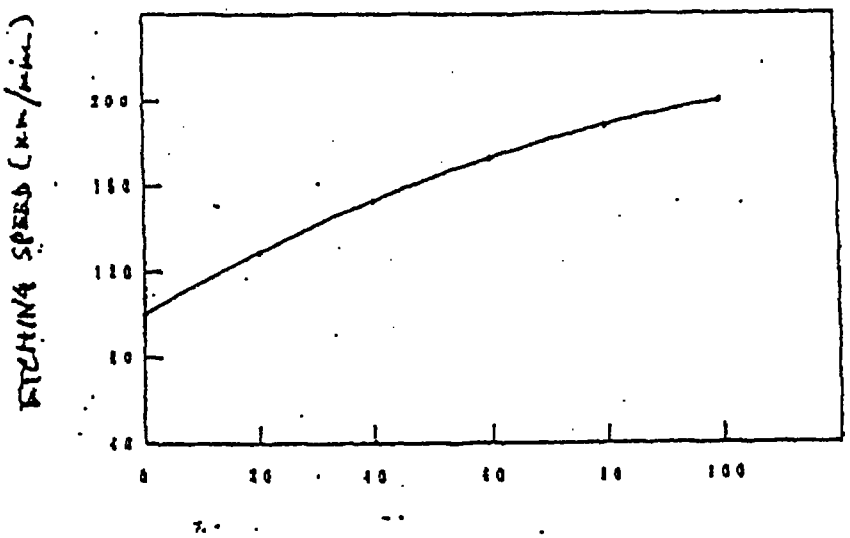
FIG.2



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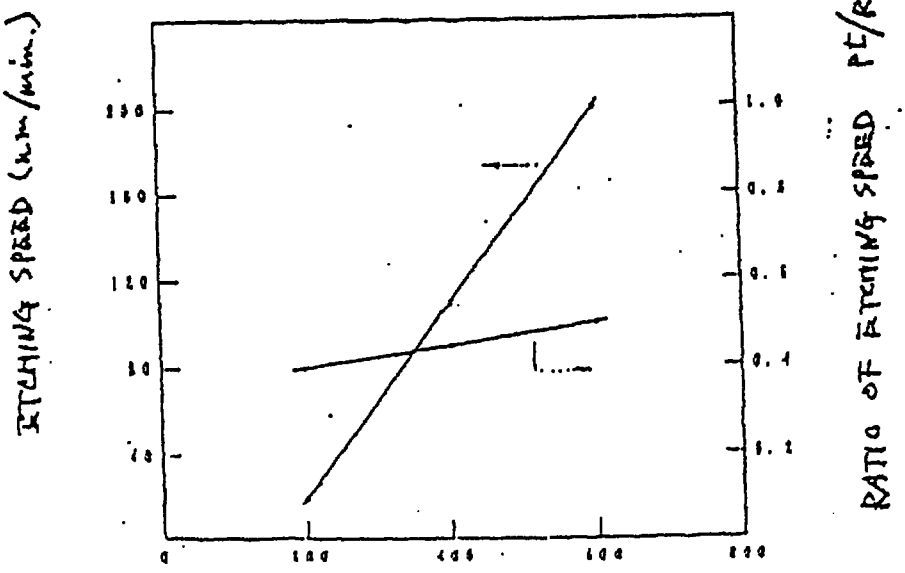
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FIG. 3



MIXING RATIO ETCHING GAS $S_2Cl_2/(S_2Cl_2+Cl_2)$ (%)

FIG. 4

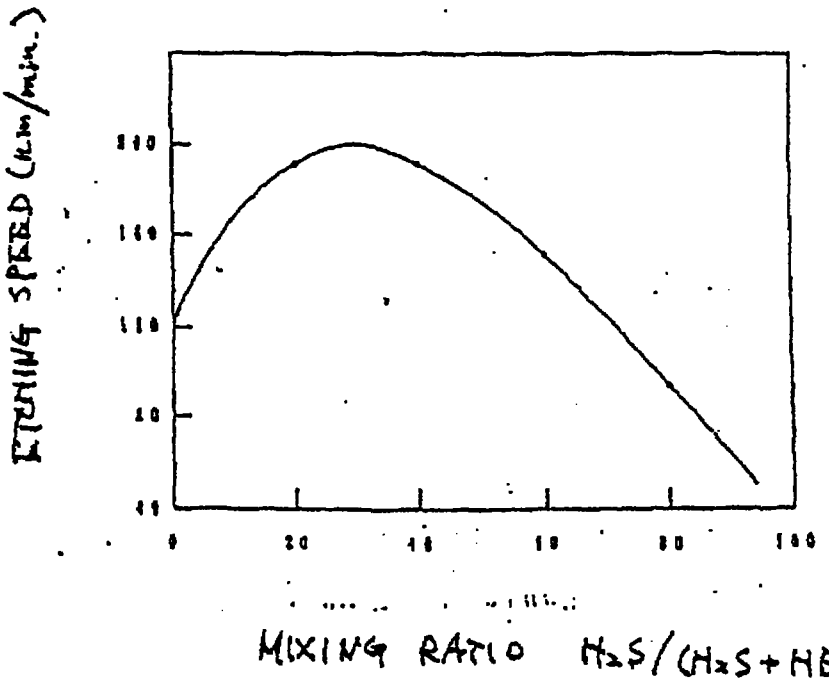


RF POWER (W)

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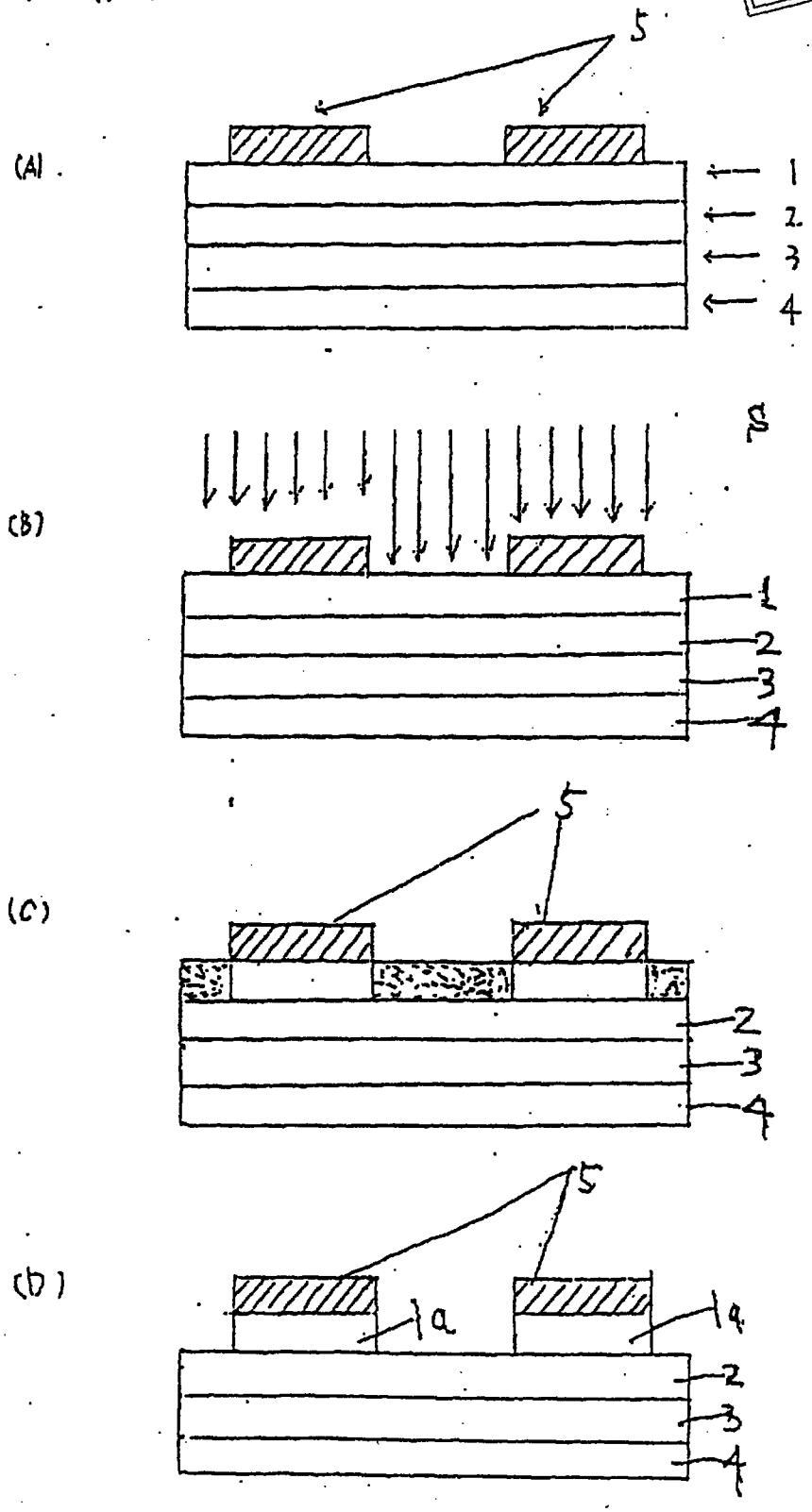
FIG.5



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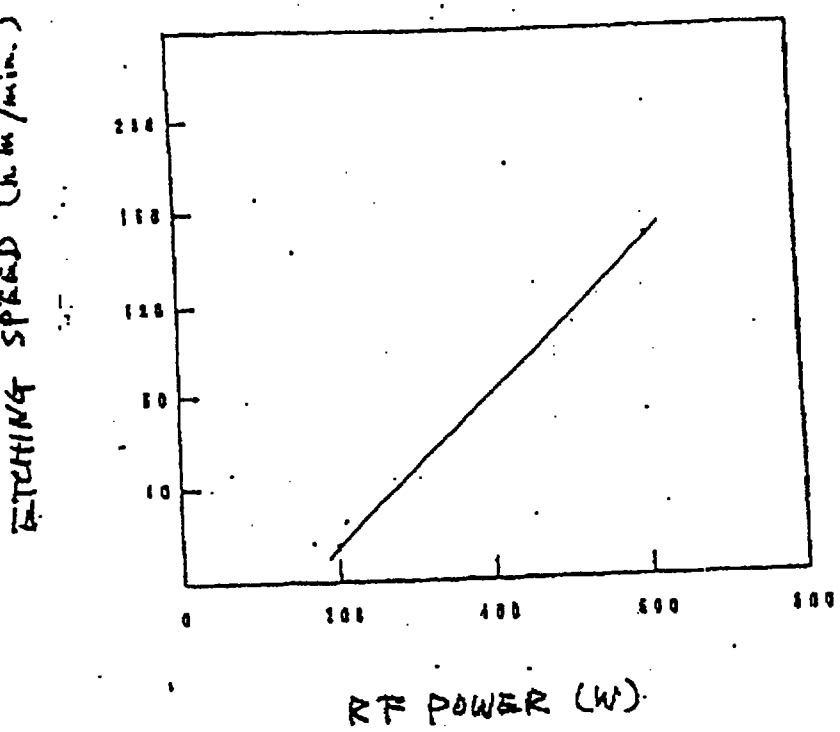
FIG. 6



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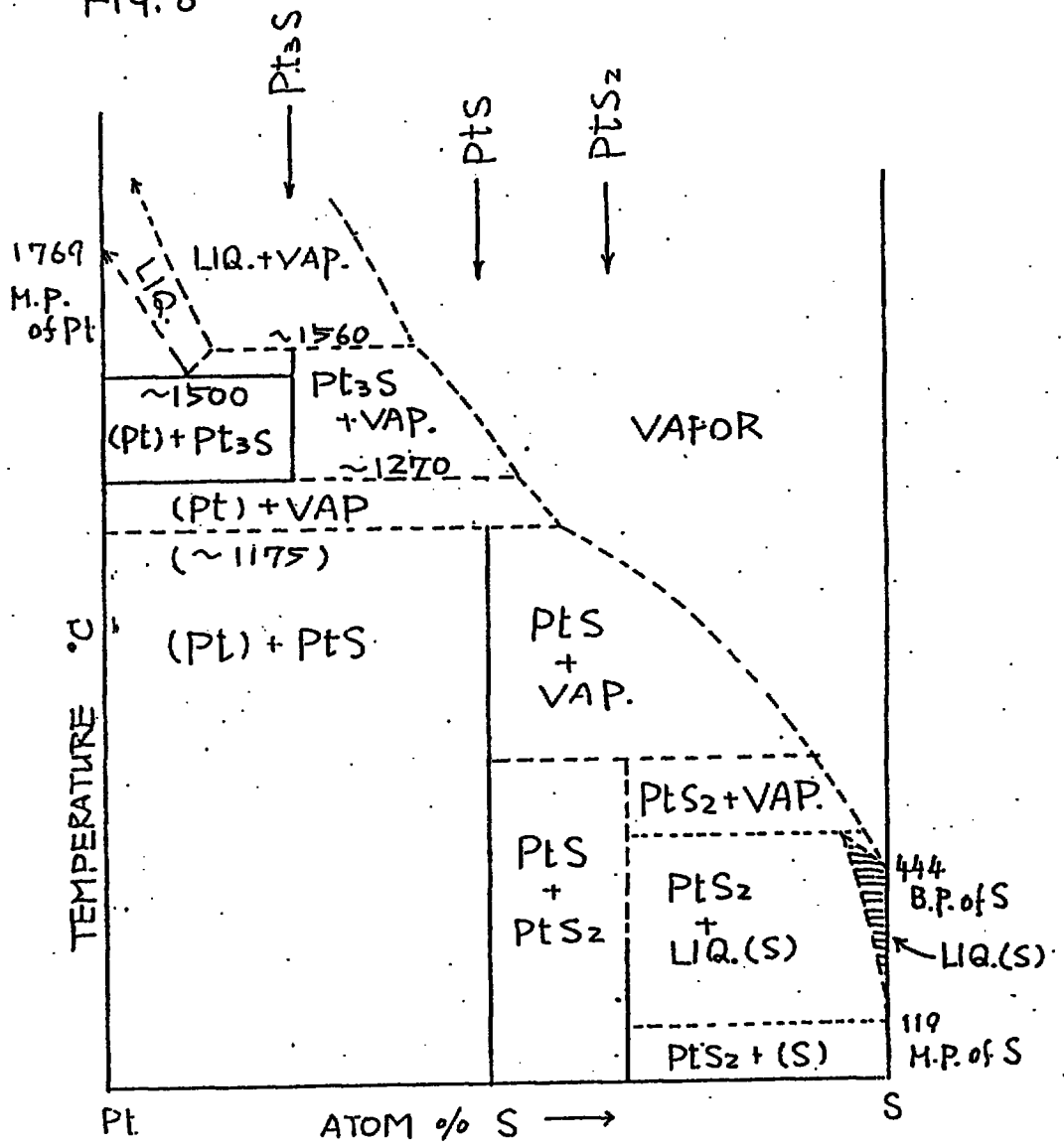
FIG. 7



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FIG. 8



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FIG. 9

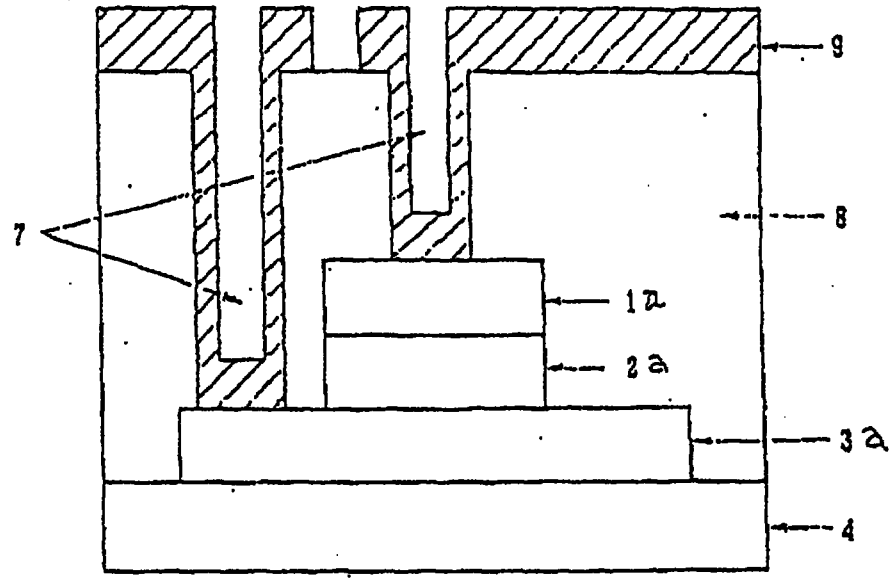
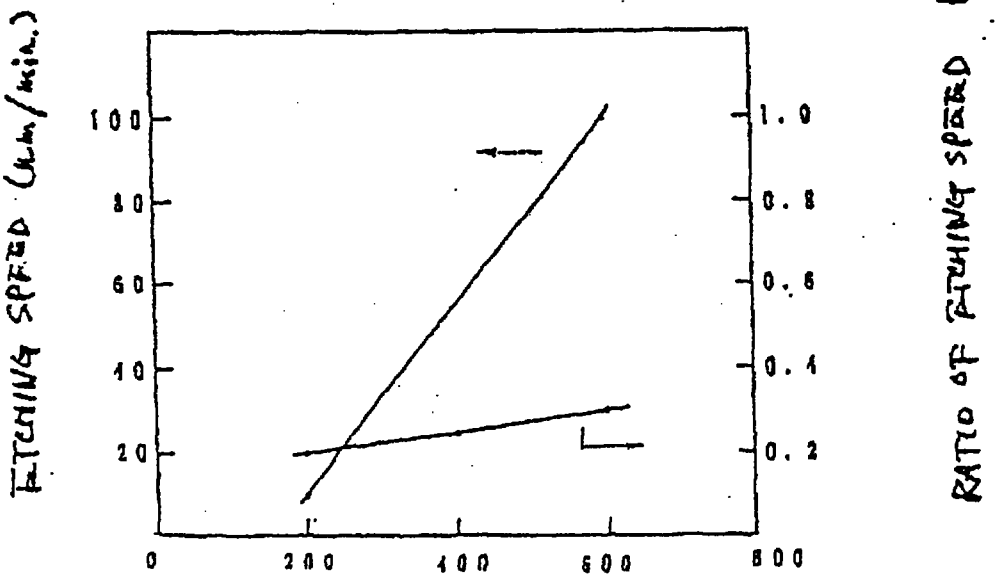


FIG. 10



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ABSTRACT OF THE DISCLOSURE

TITLE OF THE INVENTION

Manufacturing method of semiconductor devices

On top of a substrate having already-completed circuit elements and wiring, etc., insulation under layer 4, Pt layer 3 for bottom electrode, dielectric film 2 and Pt layer 1 for top electrode are shaped.

And then, form top electrode 1a, capacitance insulation film 2a and bottom electrode 3a by etching Pt layer 1 for top electrode or Pt layer 3 for bottom electrode, using an etching gas containing S component while composing Pt and S compound; or first compose Pt and S compound, and then etch the compound.

(Figure 1)

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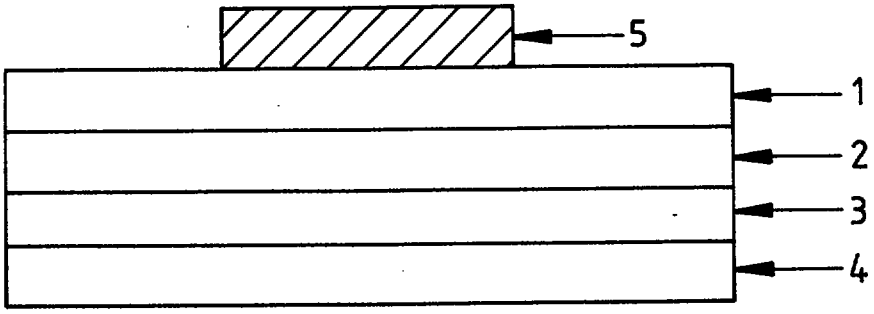


FIG 1(A)

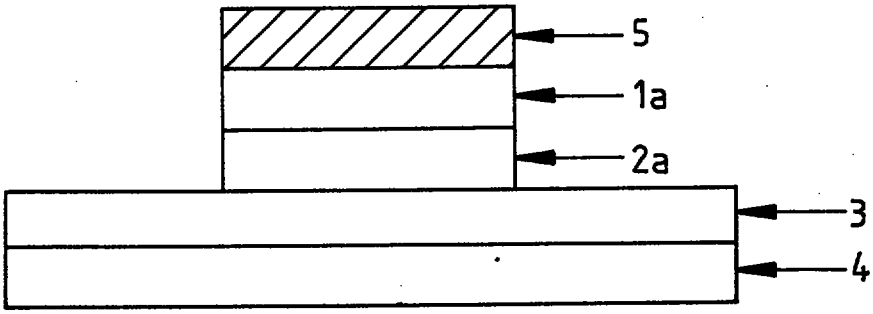


FIG 1(B)

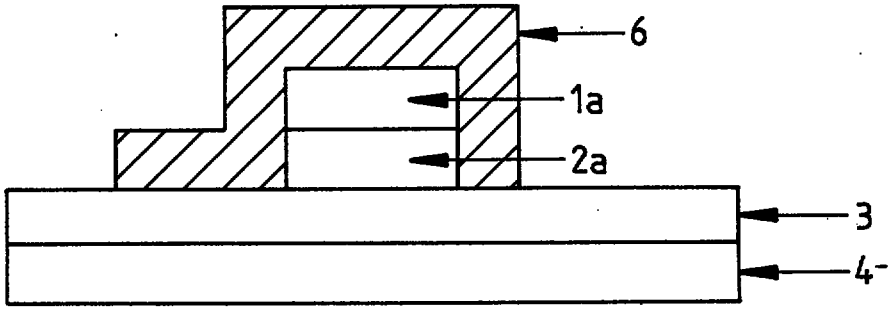


FIG 1(C)

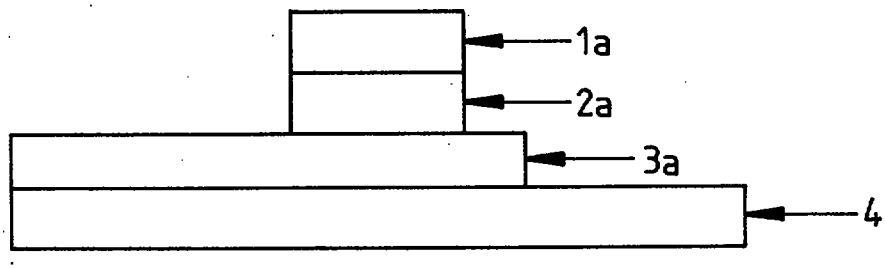


FIG 1(D)

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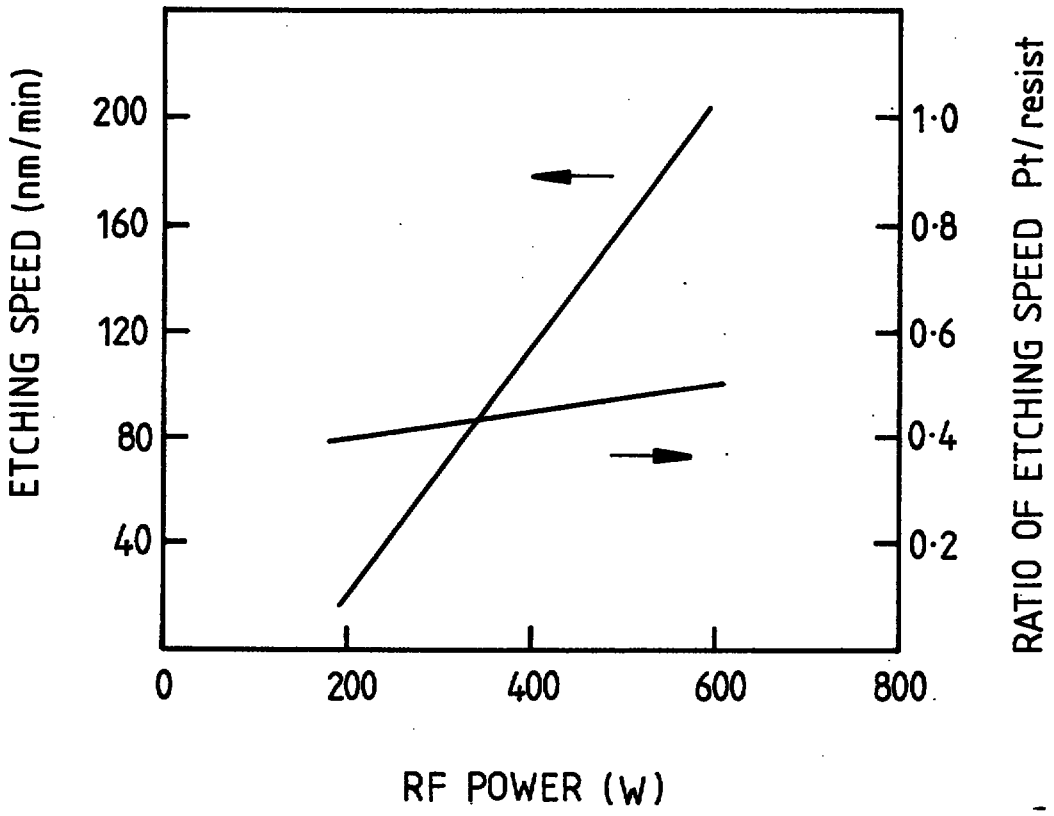


FIG 2

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FIG 3

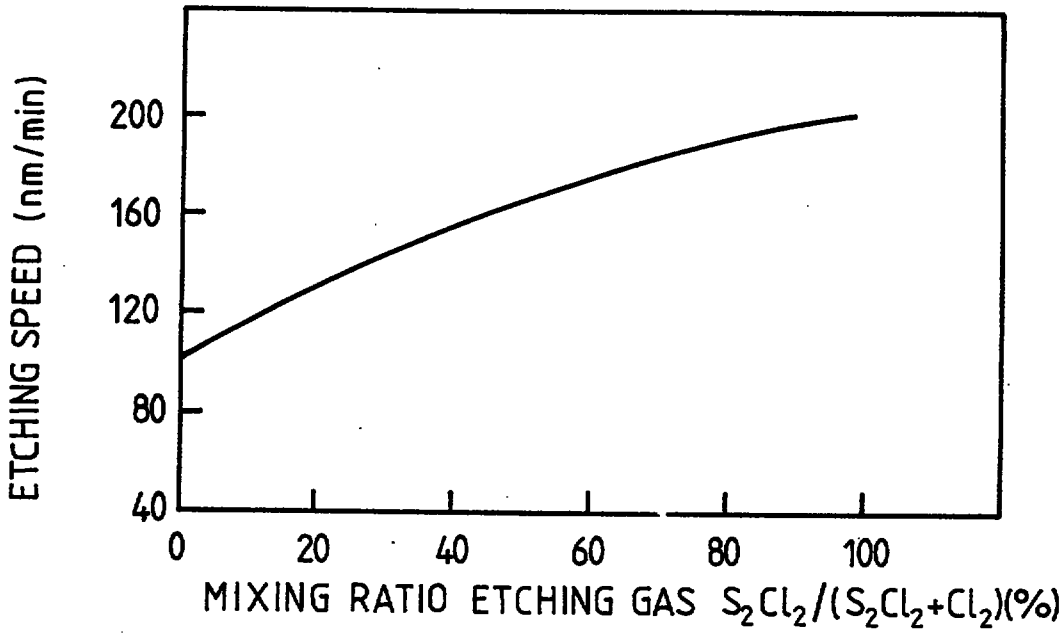
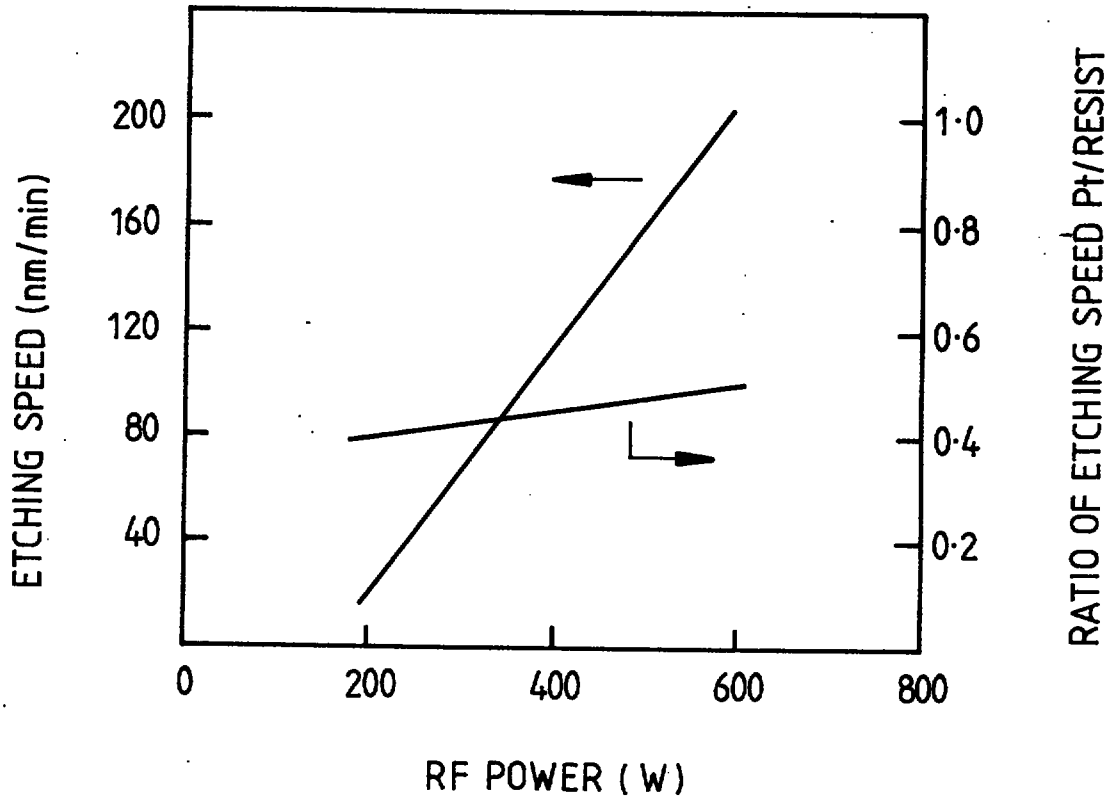
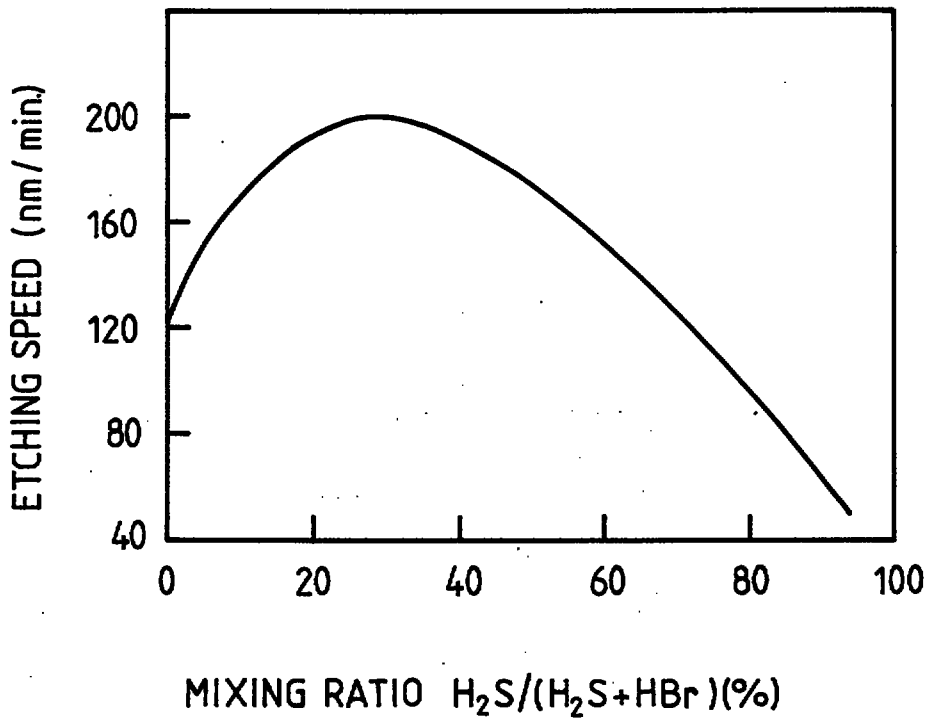


FIG 4



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FIG 5



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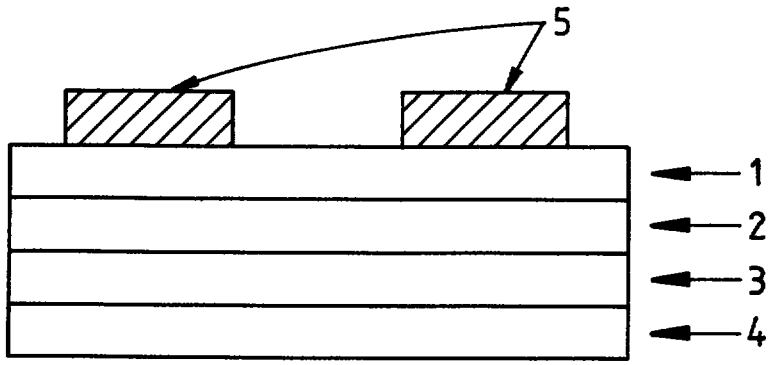


FIG 6(A)

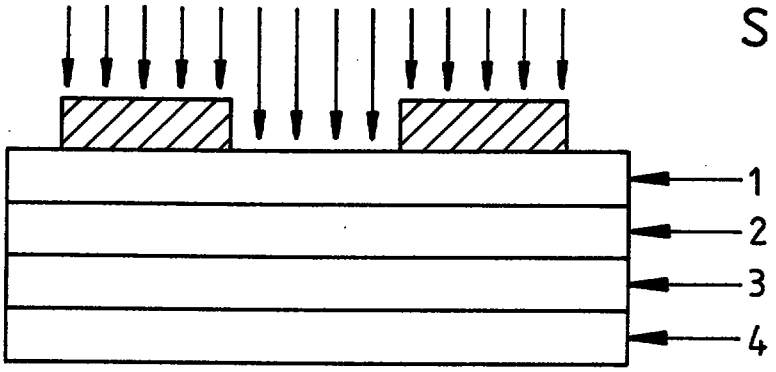


FIG 6(B)

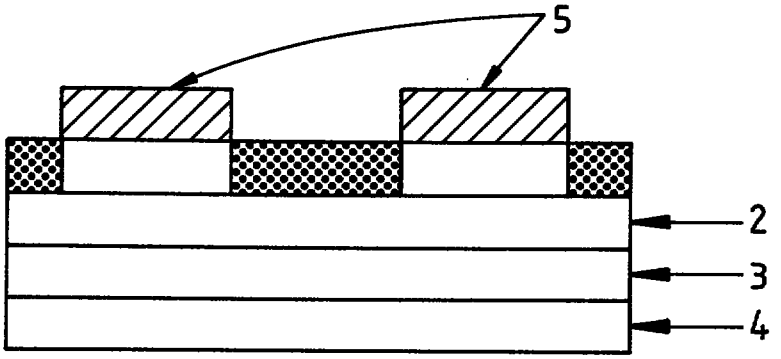


FIG 6(C)

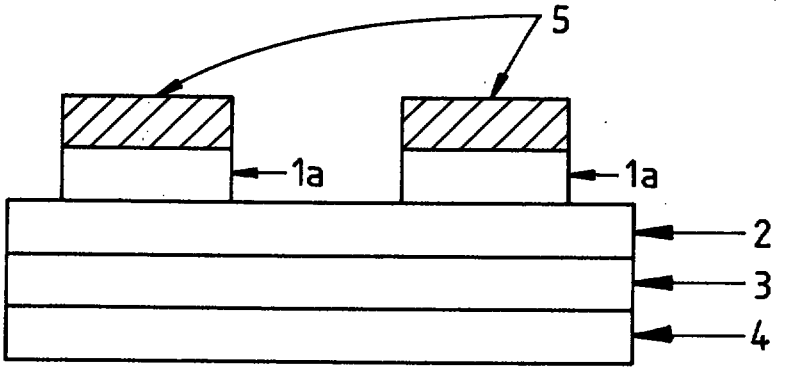
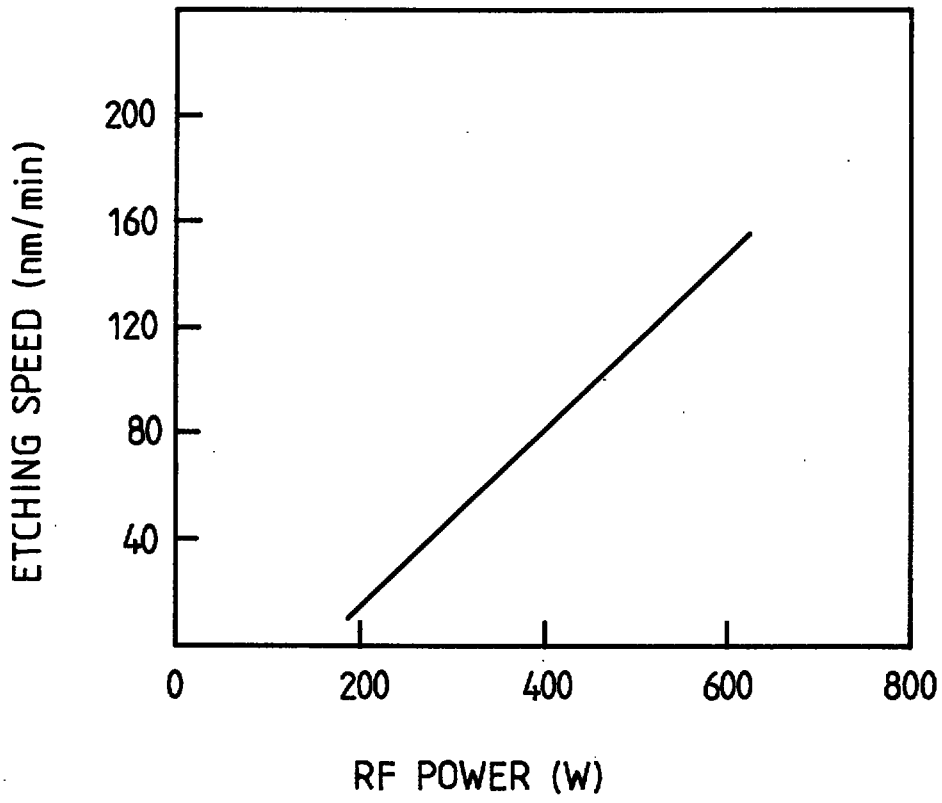


FIG 6(D)

REPLACEMENT SHEET
25 MAY 1996
Date .....

FIG 7



REPLACEMENT SHEET
Date : 25 MAY 1996

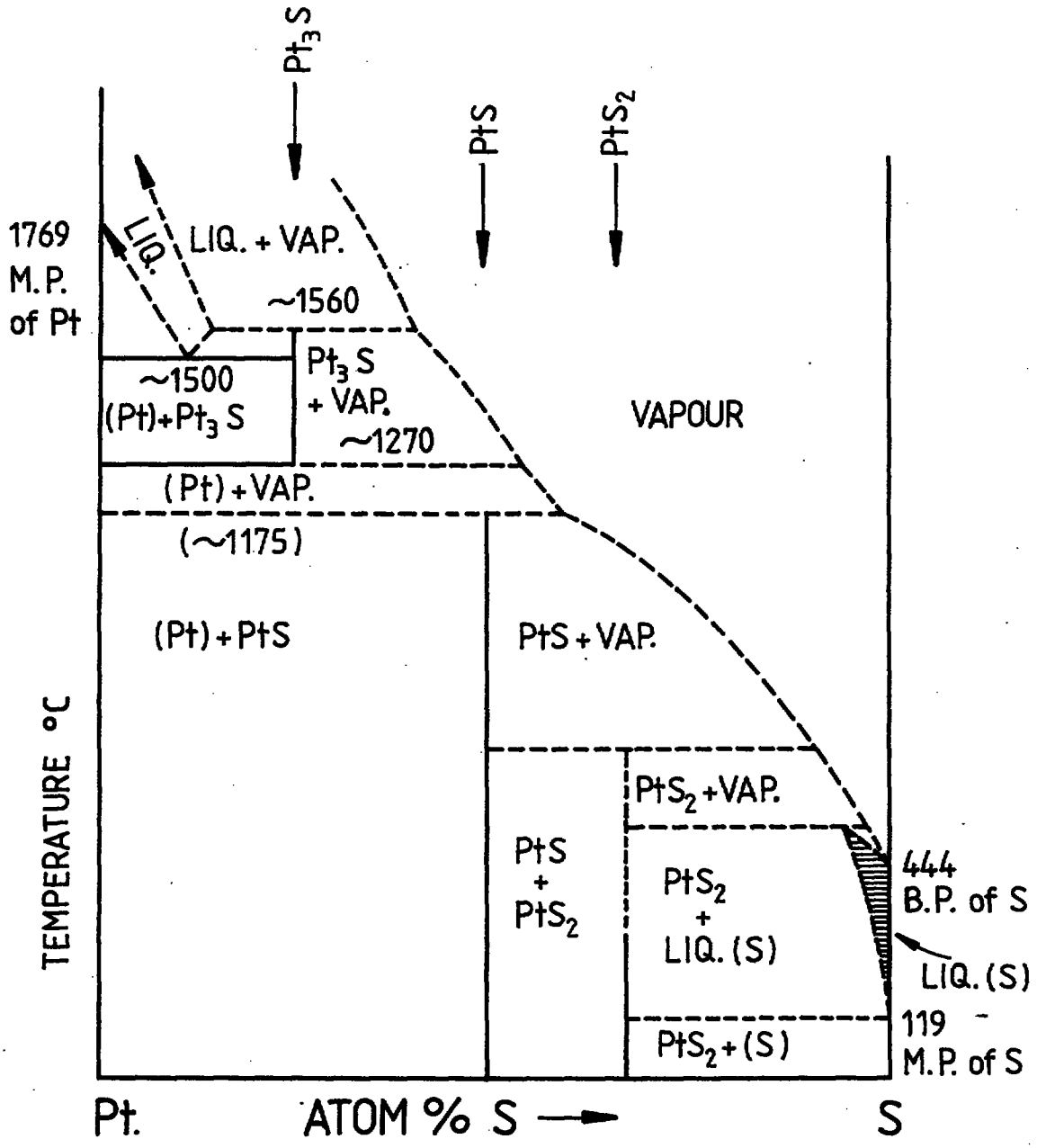


FIG 8

REPLACEMENT SHEET
Date : 25 MAY 1996

Substitute sheet - 25 May 1996

FIG 9

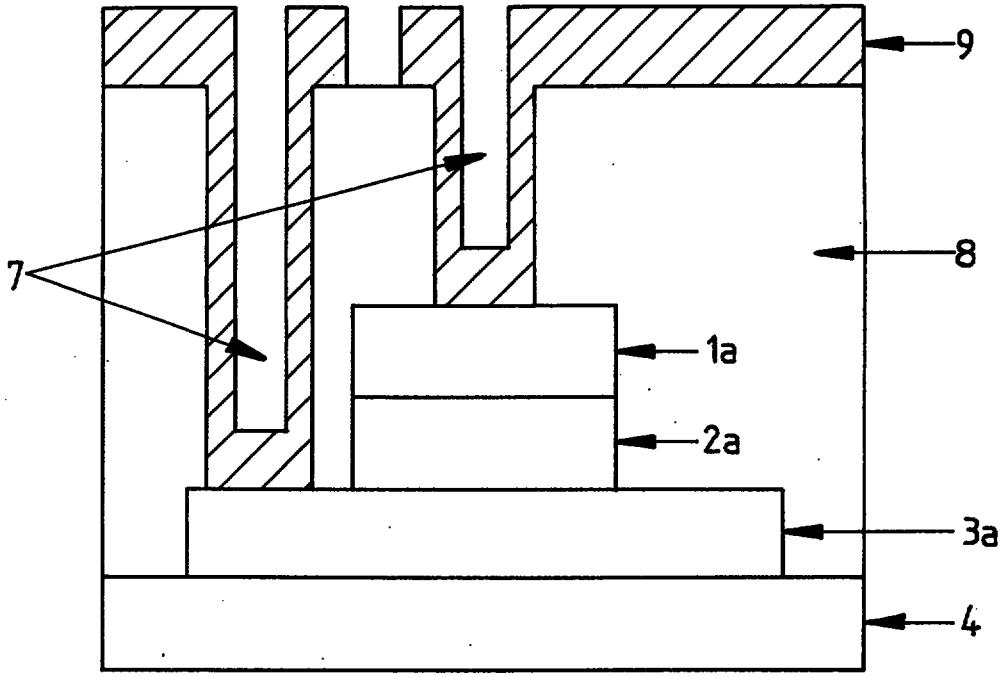
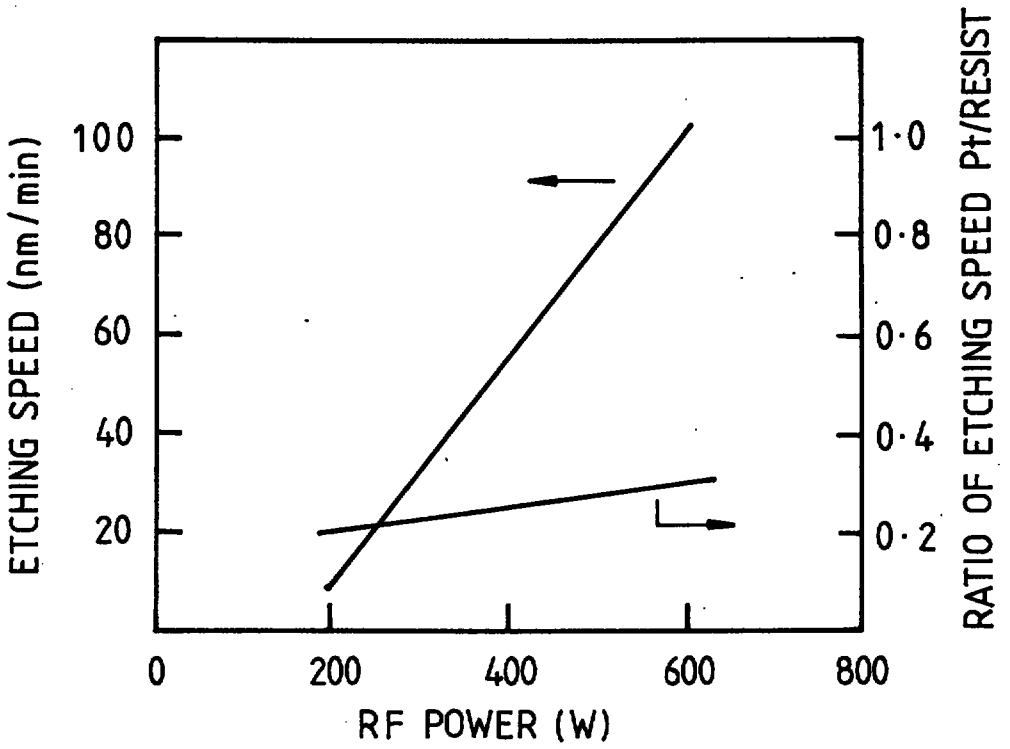


FIG 10



* C L M S *

REPLACEMENT SHEET
Date : 14 AUG 1997

Substitute sheet
14 August 1997

4. Semiconductor device manufacturing method, wherein capacitance element is formed by:

first providing, on top of a substrate having already-completed circuit elements and wiring, etc., insulation layer, bottom electrode Pt layer, dielectric film and top electrode Pt layer, and then selectively dry etching said top electrode Pt layer and dielectric film, thereafter, selectively dry etching bottom electrode Pt layer; and in conducting dry etching on said Pt consisting bottom electrode or top electrode,

using a gas containing S component as additive gas to Pt etching gas.

5. Semiconductor device manufacturing method according to Claim 4, wherein the additive gas is at least one member selected from the group consisting of sulfur fluoride, sulfur chloride, H_2S and SO_2.

~~6. Semiconductor device manufacturing method, wherein capacitance~~ element is formed by:

first providing, on top of a substrate having already-completed circuit element and wiring, etc., insulation layer, bottom electrode Pt layer, dielectric film and top electrode Pt layer, and then selectively dry etching said top electrode Pt layer and dielectric film, thereafter selectively dry etching bottom electrode Pt layer; and before conducting dry etching on said Pt consisting bottom electrode or top ~~electrode,~~

REPLACEMENT SHEET
Date : 14 AUG 1997

Substitute sheet
14 August 1997

~~implanting S into Pt by means of ion implantation to~~ compose S and Pt compound, and ~~then~~ dry etch the Pt compound ~~thus composed.~~