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## (54) MULTIPHASE SIGNAL GENERATOR

(71) We, SOCIETE JATEC, a Lebanese Corporation, of Immeuble Steiger, Cornich du Fleuve, Beyrouth, Lebanon, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention concerns a multiphase signal generator, that is, a generator whose function is to feed several output terminals by supplying them with output signals which succeed one another in a predetermined order. More exactly, these output signals may assume two predetermined values. One of these values may, for example, enable the bringing into action of a device controlled by one of these output terminals, the other of these values setting that device in the rest state. It may then be said, to simplify the description, that the output signal exists when it has the first of these values, and does not exist when it has the second.

Such a multiphase signal generator may be used more particularly in a traffic control unit for controlling the various traffic lights of a highway crossroads. The various lights which control the traffic in a same direction from a group, and there are several groups. Each of the outputs of the multiphase signal generator then controls the switching on and switching off of the light(s) of a determined colour taken in one or possibly several of these groups of traffic lights.

Multiphase signal generators used up till now had the disadvantage of not enabling the duration of the various phases of their operating cycle to be controlled independently and conveniently. Certain of these generators, of the electronic type, comprised, for example, a clock pulse oscillator feeding a frequency divider which itself feeds a decoder supplying output signals. A clock pulse oscillator feeding a ring type step by step switch which may itself control power circuits at the output has also been used with like aims in view.

The aim of the present invention is, more

particularly, to overcome the above mentioned disadvantage.

According to the present invention there is provided a multiphase signal generator comprising:

a controllable clock for supplying clock pulses, the frequency of which is controllable by a frequency control signal,

a counting arrangement arranged to receive said clock pulses and having  $k$  phase output terminals from which it is arranged to supply sequentially and respectively  $k$  phase signals, each beginning after a predetermined number of clock pulses and ending after a greater predetermined number of clock pulses,

an output decoder having  $k$  input terminals arranged respectively to receive the  $k$  phase signals, and  $q$  output terminals which form the output terminals of the multiphase signal generator, and from each of which the output decoder is arranged to supply an output signal during certain of said phase signals according to the particular output terminal,

a selection decoder having  $k$  input terminals arranged respectively to receive the  $k$  phase signals and  $p$  selection terminals from each of which the selection decoder is arranged to provide a selection signal during certain of said phase signals according to the particular selection terminal, these selection signals being arranged to be provided sequentially without two selection signals being provided at any one time from two selection terminals,

a control circuit comprising  $p$  adjustable elements respectively connected to the  $p$  selection terminals and arranged sequentially and respectively to receive the  $p$  selection signals and to supply frequency control signals to the said clock in response to the selection signals and of a value in each case in dependence upon the adjustment value of the particular adjustable element.

The multiphased signal generator may readily be produced in an entirely electronic configuration, so as to operate in a cyclic way. Each cycle may comprise any number of phases each having a duration which may

be controlled independently, that is, without influence on the other phases. The generator makes it possible to control power output circuits which are in any number, independently of the number of phases. Each of these power output circuits may be brought into action during one only or several phases of the cycle, these phases being consecutive or otherwise. The generator may be compared, if it operates in a cyclic manner, to a motor which could operate at a continually adjustable speed, each revolution being divided into several sections corresponding to the previously mentioned phases, and the speed of the motor possibly being controlled, for each of these sections, between certain limits. That motor could drive a shaft which could bear any number of cams. These cams could each control a switch and each have a profile which is distinct and easy to modify. Moreover, the generator according to the invention is deprived of inertia if it is produced in an electronic configuration. Its operation is completely controlled by clock pulses supplied by clock pulse oscillator. The independent adjusting of the duration of the various phases is obtained according to the invention by the use of several distinct adjusting means corresponding to distinct phases of operation. These adjusting means control the frequency of the clock pulse oscillator and are successively brought into action by the actual operation of the generator, when the latter reaches the corresponding phases. More exactly, the adjusting means are brought into action by selection signals developed from the clock pulses. These selection signals determine, at each instant, which of various adjusting means is in action. It will be seen that a functional loop is thus produced, the clock pulse oscillator controlling the operation of a digit assembly and that digit assembly itself controlling the frequency of the clock pulse oscillator.

With reference to Figures 1 to 7 of the accompanying drawings, embodiments of the present invention will be described herebelow by way of example.

Figure 1 is a block diagram of a generator according to the invention,

Figure 2 is an electronic diagram of a part of the generator in Figure 1,

Figures 3 and 4 are operation diagrams of the generator in Figures 1 and 2,

Figure 5 is an electronic diagram of a part of the generator in Figure 1,

Figure 6 is a block diagram of a generator according to the invention, including, besides the elements of the generator in Figure 1, complementary elements enabling a better adaptation to a highway traffic control unit, and

Figure 7 is an electronic diagram of a part of the generator in Figure 6.

Corresponding elements in these various figures bear, in all these latter, the same reference letters or numerals, an electrical conductor possibly being designated by the same reference letters, or numerals, as the signal it transmits, and as the diagram showing the variations in that signal.

The multiphase signal generator according to the invention which will be described by way of an example may be used for controlling highway traffic signals at a road junction, connected with a power output circuit. These traffic signals may be divided into three groups, and for each of these groups, it is required that the lighting of the green, yellow and red lamps be controlled according to a set colour diagram, which may be different for each group.

Figure 1 shows a clock pulse oscillator OH, whose period T is easily adjusted, for example, by setting a resistor. That clock pulse oscillator supplies clock pulses to a frequency divider DF. It may be formed by flip-flops connected up in series. For the application indicated above, where speeds are very low in relation to the possibilities of the electronic components, an asynchronous binary fitting of conventional type gives good results. It is known that six flip-flops are sufficient for carrying out a division by 64 and, in a general way, that a number  $a$  of flip-flops enables a division of frequency by a number  $n \leq 2^a$ . The outputs of the flip-flops of the frequency divider DF feed a counting decoder DC. That decoder consists of logic gates of the AND type whose inputs are connected to the flip-flops of the frequency divider DF. These gates may be, for example, of a conventional diode type. The frequency divider DF and the counting decoder DC form a counting assembly making it possible to count the clock pulses up to a number  $n$ , equal to, or less than, if the number of flip-flops of the frequency divider DF is  $a$ ,  $2^a$ . The duration of an operation cycle of the generator according to the invention is then determined by the number  $n$  and the values of the period of the clock pulse oscillator OH. The frequency divider DF is arranged in a conventional way so that when  $n$  clock pulses have been received, the flip-flops return to their original state, that is, each time the counting assembly has counted  $n$  clock pulses, it returns automatically to zero. This is obviously necessary to enable cyclic operation. It is however quite evident that other types of counting assembly could be used, provided that if cyclic operation is required, the counting assembly return to zero at the end of a certain number of clock pulses  $n$ . The choice of the number  $n$  depends on the intended applications, and more particularly on the relations between the various values which the durations of the various phases should be able to assume.

More exactly, this number should be chosen so that the ratio of the maximum required value of the period of the clock pulse oscillator OH to the minimum required value of that same period be sufficiently low for the convenient production of an oscillator with a period adjustable from this minimum to this maximum. It may be observed, in this respect, that an increase of the number  $n$  increases the price of the generator as a whole only in very slight proportions, for a single complementary flip-flop enables that number to be doubled.

The interposing of insulating or adapting elements may be necessary between the outputs of the frequency divider DF and the counting decoder DC, according to the components used for producing these two elements. Such elements are not shown. In a general way, it must be understood that each time insulating, adapting or sign reversing elements must be interposed between elements shown here by blocks, these elements are not shown, to simplify the drawing and the description. The inserting of such elements is indeed possible to the man skilled in the art.

The outputs of the AND gates of the counting decoder DC, equal in number to a number  $m$ , are connected to an equal number of inputs of a ring type step by step switch CA. Each of these outputs sends out, during each cycle, a counting pulse to the corresponding input of that switch. The latter comprises a certain number of stages, equal to  $m$ , each provided with an output. Each counting pulse received by the ring type step by step switch CA brings one of these stages into action, that is, when the ring type step by step switch receives a counting pulse on an input corresponding to a stage, that stage comes into action and supplies at its output, a phase signal beginning with that counting pulse. That phase signal ends with the following counting pulse, which, moreover, brings the following stage into action, this resulting in the sending out of another phase signal to the following output of the switch, and so on, in a cyclic manner.

The existence of a phase signal at an output means that a continuous potential, for example 1 volt, is applied to that output, and the non-existence of such a phase signal means that another potential for example 12 volts, is applied to that same output. Of course, the values of the electric potentials used may be very diverse, according to the components used.

The producing of such a ring type step by step switch is within the competence of the man skilled in the art. That switch may be, for example, produced for the above mentioned application, and in compliance with Figure 5, by means of controlled semiconductor rectifiers such as thyristors, which

make it possible to obtain sufficient power at the output. It comprises a number  $m$  of inputs such as 501, 502 and 503 and an equal number of outputs such as 511, 512 and 513. Each of these inputs is connected through a rectifier such as 521 and a resistor such as 531 to the gate of a thyristor such as 541, 542 or 543. The cathode of that thyristor is connected up to a common negative feed terminal 591 which is, moreover connected up to the gate of that thyristor through a resistor such as 551. The anode of that thyristor is connected up to a common positive feed terminal 592 through a charge resistor such as 561, as well as to an output such as 511. The anodes of the thyristors such as 541, 542 and 543 are connected up in a ring by means of capacitors such as 571, 572 and 573 so that the anode of each of these thyristors, for example the thyristor 541, is connected up on the one hand, to the anode of the preceding thyristor, for example the thyristor 542 and on the other hand, to the anode of the following thyristor, for example the thyristor 543. Each of the thyristors such as 541, 542 and 543 constitutes a stage of the ring type step by step switch CA.

The operation of that switch may be described, assuming that at the outset, all the thyristors are extinguished. When an input such as 503 receives a counting pulse, the corresponding thyristor such as 543 is fired. When the following counting pulse is applied to the following input such as 501, the following thyristor such as 541 is fired in its turn, this causing a lowering of the potential of its anode. This lowering is transmitted through a capacitor such as 571 to the anode of the thyristor such as 543, previously fired, and causes the extinguishing of the latter. A negative phase signal then appears at the corresponding output such as 511, and on that output only, until a counting pulse applied to a subsequent input such as 502 causes the firing of a thyristor such as 542, the applying of a phase signal on an output such as 512, the extinguishing of the thyristor such as 541, and the ending of the phase signal at the output such as 511.

The outputs of the ring type step by step switch CA feed the inputs of two decoders, an output decoder DS and a selection decoder DR. These two decoders comprise logic gates of the OR type the number of these gates being  $p$  for the selection decoder and  $q$  for the output decoder. The numbers  $p$  and  $q$  are at the most equal to the previously mentioned number  $m$ . Each of the inputs of each of these gates is connected to an output of the ring type step by step switch CA. The outputs of the OR type gates of the output decoder DS equal in number to  $q$  may constitute the previously mentioned output terminals of the generator.

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73 (13)

These output terminals may however also be provided with power switches, the existence of a signal at the output of one of the OR gates of the output decoder DS then resulting in the closing of such a power switch by that gate. These controlled power switches may, for example, be of the type known by the name of TRIAC. These switches taken as a whole constitute the output circuit CS shown in the figure. Each of these switches is connected up in series to an alternating current voltage source and a coloured lamp of one of the traffic lights. The previously mentioned output signals may then be considered as being constituted by the alternate voltages applied to these lamps.

The assembly comprising the frequency divider DF, the counting decoder DC, the ring type step by step switch CA, the output decoder DS and the selection decoder DR constitutes the previously mentioned unit assembly, which is designated in Figure 1 by the reference EN.

The outputs of the OR gates equal in numbers to  $p$ , of the selection decoder DR, constitute the previously mentioned selection terminals. They are each connected to an input of a control circuit CC comprising a number  $p$  of adjustable resistors. The first terminal of each of these adjustable resistors is connected up to a corresponding selection terminal. The second terminals of these resistors are all connected up to the control terminal of the clock pulse oscillator OH and enable the previously mentioned frequency control signal to be supplied, that signal being a current signal depending on the value of the adjustable resistor to which a selection signal is supplied. The control circuit CC could however be constituted by elements other than resistors; for example, by capacitors or by adjustable induction coils, or by a combination of such adjustable elements, that is, more generally by adjustable impedances. It could also be constituted by potential sources or adjustable current sources, or even, in the case where the generator according to the invention is not electronic but fluidic, by sources of pressure, which are, for example adjustable. It is necessary only for the adjustable elements of the control circuit CC to be equal in numbers to the number  $p$  and to be able each to assume various adjustment values. Each element must be arranged so that its adjustment value controls the value of the frequency control signal, that is, the period of the clock pulse oscillator OH, during a selection period corresponding to that element. That selection period is defined by the existence of a selection signal on the selection terminal corresponding to that element.

It may be observed that when the adjustment of one of the adjustable elements of the control circuit CC is effected manually

or automatically, the frequency of the clock pulse oscillator OH is modified during the selection period corresponding to that adjustable element, and only during that period. Now, the duration of each selection period is determined by the time between the two counting pulses which determines the beginning and the end of that selection period, by the clock pulse oscillator period during that selection period, that number of clock pulses being predetermined by the arranging of the counting decoder DC and of the selection decoder DR. Therefore, the duration of each selection period is thus controlled independently of the duration of the other selection periods. By a suitable choice of the arranging of the selection periods in relation to the various output signals, it may be observed that it is thus possible to affect the duration of these output signals with great versatility. Adjusting knobs CC1 and CCp, enabling the manual adjusting of the adjustable elements of the circuit CC have been shown in the figure.

The generator according to the invention has, moreover, the advantage of being economical, for the number of adjusting elements may easily be made much lower than the number of distinct phases which may be defined taking the output signals as a basis.

Figure 2 shows the electronic diagram of the clock pulse oscillator OH and of the control circuit CC. The clock pulse oscillator OH essentially consists of a unijunction transistor UJT, whose two bases are connected, the one to a suitable positive potential source through a resistor R1 and the other to earth through a resistor R2. The emitter of that transistor is connected up to earth through a capacitor CH, as well as, on the other hand, to the control circuit CC. Thus is constituted a relaxation oscillator of a conventional type, whose period is controlled by the current charging the capacitor CH from the control circuit CC. The clock pulses are sampled at the terminals of the resistor R2. The adjustable elements of the control circuit CC are adjustable resistor RG1, RG2 . . . RGp. Rectifiers D1, D2 . . . Dp are connected up in series to these adjustable resistors. The previously mentioned control terminal is shown at BC, whereas the previously mentioned selection terminals are shown at BS1, BS2 . . . BS<sub>p</sub>.

Such an oscillator may just as well be produced by means of a diode having four layers which suddenly becomes conductive when the voltage applied between its terminals reaches a predetermined upper threshold and remains conductive as long as that voltage does not go down below a predetermined lower threshold.

During each of the previously mentioned selection periods, the selection decoder DR

applies a positive potential to one and only one, of the selection terminals BS1, BS2, . . . Bsp. The charge current of the capacitor CH is then determined by the ratio of that positive potential to the value of the adjustable resistor RG1, RG2, . . . or RGp which corresponds to the selection terminal in consideration.

The potentials applied to the various selection terminals during the various selection periods are all the same in the example described. But it is quite evident that in other embodiments, it would be possible to assign different values to these potentials.

The insulation diodes such as D1, D2, . . . Dp make it possible to insulate the various selection terminals from one another.

If the ratio between the maximum and minimum values of the recurrence period of the clock pulses is too great for the adjusting of that period to be effected by means of simple adjustable resistors it is possible to effect selection switching not only on adjustable resistors, but also on adjustable capacitors which would moreover fulfill the function of the capacitor CH. The circuit thereof would obviously be rather complicated.

With reference to Figures 3 and 4, the operation of the generator according to the invention will now be described in the case where it is applied to the controlling of three groups of three-coloured traffic lights. Each of these groups of lights corresponds to the traffic in one direction. In this example, the following values have been adopted for the various previously mentioned numbers:

$$\begin{aligned} n &= 64 \\ m &= 15 \\ p &= 8 \\ q &= 9 \end{aligned}$$

Figures 3 and 4 show a diagram IH indicating the clock pulses sent out by the clock pulse oscillator OH. Six diagrams B1 to B6 show output signals of the flip-flops composing the frequency divider DF, the diagrams IC1 to IC15 show the counting pulses reaching the output of the counting decoder DC and applied to the inputs of the ring types step by step switch CA. The diagrams SP1 to SP15 show the phase signals

reaching the outputs of the ring type step by step switch CA. The diagrams SS1 to SS8 show the selection signals supplied by the selection decoder DR and applied to the control circuit CC. The diagrams V1, V2, V3, J1, J2, J3, R1, R2, R3, represent respectively, the output signals applied by the output decoder DS, across the output circuit CS, to the green lamps of the three groups of traffic lights, to the amber lamps of these three groups and lastly, to the red lamps of these same groups, respectively, it being understood that the arrangements enabling amber flashing lights to be obtained are not distinguished here from those enabling continuous amber lights to be obtained. The diagram F1, F2 and F3 show the colours of the lights of the first, second and third groups respectively, it being understood that the colour green is shown by square shading, the colour amber is shown by inclined shading and the colour red is shown by horizontal shading. In these figures, the successive phases of the operating cycle of the multiphase signal generator are designated by the references S1, S2, . . . S15.

The operation of the multiphase signal generator according to the invention will now be described by means of these various diagrams:

The  $m$  counting pulses supplied by the counting decoder DC (diagrams IC) correspond to the clock pulses (diagram IH) of order 0, 2, 4, 7, 9, 21, 23, 25, 28, 30, 42, 44, 46, 49 and 51 and limit the phases S1, S2, etc. up to S15 during which the period of the oscillator OH assumes the values T1, T2, . . . T15.

The selection decoder DR makes it possible to control the duration of: the phases S2, S4, S7, S9, S12 and S14 by the adjustable element RG1 of the control circuit CC during the existence of the selection signal SS1;

The phases S1, S6 and S11 by the element RG2 during the existence of the selection signal SS2;

And the phases S3, S5, S8, S10, S13 and S15 by the elements RG3, RG4, RG5, RG6, RG7 and RG8 during the existence of the selection signals SS3, SS6, SS4, SS7, SS5 and SS8 respectively. Output signals exist at the output terminals as follows:—

- |    |                   |                |              |
|----|-------------------|----------------|--------------|
| 1/ | During the phases | S5 and S6      | (diagram V1) |
| 2/ | " "               | S10 and S11    | (diagram V2) |
| 3/ | " "               | S1 and S15     | (diagram V3) |
| 4/ | " "               | S1, S2 and S14 | (diagram J3) |
| 5/ | " "               | S4, S6 and S7  | (diagram J1) |
| 6/ | " "               | S9 S11 and S12 | (diagram J2) |

7/ During the phases S1, S2, S3, S4, S8, S9, S10, S11, S12, S13, S14, and S15  
(diagram R1)

8/ " " " S1, S2, S3, S5, S6, S7, S8, S9, S13, S14 and S15  
(diagram R2)

5 9/ " " " S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13 and S14  
(diagram R3)

The phases S5, S10 and S15 of the system correspond to the green only periods of the three channels. It must be possible to regulate their durations in general between 5 and 50 seconds each, all other values being, moreover, possible according to conditions of use. This means that it must be possible to vary T5, T10 and T15 between 0.4 and 5 seconds approximately, and to adjust them separately or independently.

The phases S3, S8 and S13 of the system correspond to the three "all red" periods. It must be possible to regulate their durations in general between 1 and 10 seconds each. This means that it must be possible for T3, T8, T13 to vary between 0.3 and 4 seconds approximately, and that they must be adjustable separately and independently.

The phases S2, S4, S7, S9, S12 and S14 correspond to the non-splashing amber periods, these periods occurring, the ones immediately after the green periods, the others during the end of the "RED" periods. Their durations are all the same, and it must be possible to regulate them in general between 1 and 5 seconds. This means that:  $T2=T4=T7=T9=T12=T14=Tj$ , and that it must be possible to regulate  $Tj$  between 0.5 and 3 seconds approximately.

Lastly, the phases S1, S6 and S11 correspond to the amber flashing periods which occur during the end of the green periods. Their durations are all the same and it must be possible to regulate them, in general, between 1 and 5 seconds. This means that  $T1=T6=T11=Tjc$ , and that it must be possible to regulate  $Tjc$  between 0.5 and 3 seconds approximately.

It is often useful, when no vehicle is driving in one of the directions leading to a cross-roads, to shorten the period during which traffic is authorised in that direction. It is a known method to use, for that purpose, detection elements such as electrical conductor loops sunk into the roadway, which supply a detection signal each time a vehicle drives on the roads surveyed by these detection elements. By means of Figure 6, an embodiment of the invention enabling the use of such detection signals will be described, it being understood that all the elements already described with reference to Figure 1 are again used but will not be again described for they are arranged and operate in an unchanged manner. Moreover, in Figure 6, lamps such as 601 and 602, fed

between the terminals of the output circuit CS and a common conductor PH, have been shown. The traffic may be controlled by the switching on and off of these lamps.

In the embodiment in Figure 6, the frequency divider DF receives, through a gate 604 of the OR type, not only the pulses supplied by the clock pulse oscillator OH, but also pulses, of the same type, which may be supplied by a fast oscillator OHR having a very much higher fixed recurrence frequency, a hundred c/s for example. The operator of that fast oscillator is controlled by the generator. The result of this is that when the fast oscillator OHR is brought into operation, the duration of the various phases is made extremely short, that is, the cycle goes very fast, until the generator reaches a phase where it brings about cessation of that fast oscillator.

Of course, the same result could be obtained by modifying control circuit CC and the clock pulse oscillator OH so as to be able to control, from that oscillator, a frequency of a hundred c/s which is the equivalent of an incorporation of the fast oscillator OHR in the clock pulse oscillator OH.

The fast oscillator OHR is controlled by a bistable circuit FT so that this oscillator may function or not function according to whether that circuit is in its energised state, or in its rest state, respectively. This circuit may be energised by a on pulse supplied by a time delay circuit T itself controlled by a reset circuit RAZ.

As long as the circuit RAZ supplies a reset signal, the circuit T may not supply any starting up pulse. From the instant when the circuit RAZ ceases to supply a reset signal, the circuit T allows a predetermined lapse of time to pass. That lapse is manually adjustable between a half second and twenty seconds, for example and it may be supposed that it is equal to ten seconds to facilitate the description. The adjusting of that lapse of time may be effected by means of an adjusting knob 620. At the end of that lapse of time, that circuit T supplies on pulse.

The circuit RAZ is controlled by a gate 606, of the OR type, so that a reset signal is supplied when a signal exists at any of the inputs of that gate. Three inputs of that gate 606 are connected up to the outputs of three gates 608, 610 and 612, of the AND type, which receive, at their first inputs, such as

the inputs 609 and 611, the detection signals supplied by three detection elements L1, L2 and L3 and on their second inputs, the signals V1, V2 and V3 respectively, supplied by the output decoder DS and which correspond to the "GREEN" periods on the roads surveyed by the detection elements L1, L2, L3 respectively.

The result of this is that if there is a vehicle on the road surveyed by the element L1, for example, during the "GREEN" period corresponding to that road, the detection element L1 sends out a signal which, through the gate 606, the circuit RAZ, the circuit T and the circuit FT prevents the fast oscillator OHR from operating. During the "GREEN" period, the circuit T supplies a starting up pulse which starts up the operation of the fast oscillator OHR only if no vehicle has been detected during ten seconds. This starting up causes the acceleration of the operating cycle of the generator and the end of the "GREEN" period comes almost immediately. The operation of the fast oscillator OHR must then be stopped. For that purpose, the bistable circuit FT is reset in its rest state by the output signal of a gate 614, of the NOR type, which receives the signals V1, V2 and V3 and which supplies an output signal when none of these signals is applied. With the aim of ensuring the resetting to zero of the time delay starting up circuit T at the beginning of each "GREEN" period, the gate 606 receives the signals J1, J2 and J3 supplied by the output decoder DS. Quite evidently, this aim could quite as well be achieved by using other signals, providing they are applied in all the intervals between "GREEN" periods. Such other signals could be supplied for example by the counting decoder DC.

With reference to Figure 7, an embodiment of the circuits RAZ, T, FT and OHR previously mentioned will now be described, these circuits being supplied between a negative terminal 702 and a positive terminal 704.

The circuit RAZ comprises a thyristor 706 whose cathode is connected up to the terminal 702 and whose gate is connected up, through resistors 708 and 710, on the one hand to the terminal 702 and on the other hand to the input terminal 712 connected up to the output of the gate 606, so that when that gate supplies a positive output signal, the thyristor 706 is fired. It then short-circuits a capacitor 714, which is connected up between its anode and the terminal 702, and which forms a part of the time delay circuit T. The latter is thus reset to zero.

The circuit T comprises, moreover, a unijunction transistor 716 whose emitter is connected up on the one hand to the anode of the thyristor 706 and on the other hand through an adjustable resistor 718 in series

with a fixed resistor 719, to a conductor 720 transmitting the positive feed potential. The two bases of the transistor 716 are connected up through resistors 722 and 724, the one to the conductor 720, the other to the terminal 702, the latter base being, moreover connected up through a connection capacitor 726 to the bistable flip-flop circuit FT. When the capacitor 714 is not short-circuited by the thyristor 706, it is charged, with a speed depending on the resistor 718, until the transistor 716 suddenly becomes conductive, this causing the discharging of that capacitor into the resistor 724 and the sending of a positive starting up pulse to the circuit FT. The latter comprises a thyristor 728 whose gate is connected up to the terminal 702 through a resistor 730 and on the other hand to the capacitor 726. The cathode of that thyristor is connected up to the terminal 702 and its anode, through a resistor 732 to the conductor 720. The potential of this anode decreases when the thyristor 728 is fixed by a starting up pulse applied to its gate, this corresponding to the passing of the circuit FT to its energised state. This circuit may be reset to its rest state by extinguishing the thyristor 728, by bringing back the potential of the conductor 720 to that of the terminal 702 to which it is connected by a resistor 734. For that purpose, the conductor 720 is connected up to the positive terminal 704 through a transistor 736 whose base is connected up to the output of the gate 614 and whose emitter is connected up to the conductor 720. The applying of a negative potential to that base ensures the extinguishing of the thyristor 728.

Moreover switching off of the transistor 736 also prevents the operation of the circuit T and as will be seen further on, of the fast oscillator OHR, this changing nothing of what has previously been explained, since the oscillator has not, in any case, operate, in the absence of an energising signal.

On firing of the thyristor 728 a signal is applied, through a resistor 738, to the base of a transistor 740. This transistor has its emitter connected to the terminal 702 and its collector connected, through resistor 742, to the conductor 720 and is therefore switched-on while the transistor 736 is operating and the thyristor 728 is switched-off. However, on firing of the thyristor 728, the transistor 740 is switched-off and a positive energising signal appears at the collector of transistor 740, by means of which a charge current may be supplied, through a resistor 744, to a capacitor 746 forming a part of the fast oscillator OHR, is obtained on that collector. That fast oscillator comprises, moreover a unijunction transistor 748 one of whose bases is connected up to the conductor 720 through a resistor 750 and whose other base is connected up to the

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95

100

105

110

115

120

125

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terminal 702 through a resistor 752. The emitter of the transistor 748 is connected up to the resistor 744, so as to constitute a relaxation oscillator of the same type as the one which constitutes the clock pulse oscillator OH, but with a greater recurrence frequency. The clock pulses appearing at the terminals of the resistor 752, are applied to the output terminal 754 connected up to an input of the gate 604.

According to the embodiment in figure 6 described above, it appears obviously that the operation of the system, while remaining cyclic, ceases to be periodic, for the time which passes during a complete cycle depends on the traffic.

The multiphase signal generator which has just been described may be used not only for producing a traffic unit, as in the example chosen, but also for producing advertising lighting where special effects may be obtained due to the existence of periods whose duration may be adjusted, or of automatic telephone reply systems, or even of the driving of machines having several functions operating in a cyclic way, it being understood that yet other applications are evidently possible.

It must be understood that the invention is in no way limited to the embodiment described and illustrated, which has been given only by way of example. Without going beyond the scope of the invention, some arrangements may be changed or some means may be replaced by equivalent means.

More particularly, it is possible to energise the ring type step by step switch CA directly from the clock pulse oscillator OH, without passing through a frequency divider such as DF and a counting decoder such as DC, on condition that the frequency of the oscillator OH may vary between limits sufficiently far apart. In the example of application described, its period should vary from half a second to a hundred seconds.

Moreover, the control circuit CC, the clock oscillator OH and the unit assembly EN may if derived not constitute physically distinct units and be integrated in a time delay circuit assembly.

It is, however, clear that the operation of the clock pulse oscillator OH remains unchanged, that is, that this time delay circuit assembly constitutes a clock system whose operation is the definition of a sequence of clock instants, connected to a part of a unit assembly whose function is to effect switching operations at clock instants of predetermined order.

#### WHAT WE CLAIM IS:—

1. A multiphase signal generator comprising a controllable clock for supplying clock pulses, the frequency of which is controllable by a frequency control signal,  
a counting arrangement arranged to re-

ceive said clock pulses and having  $k$  phase output terminals from which it is arranged to supply sequentially and respectively  $k$  phase signals, each beginning after a predetermined number of clock pulses and ending after a greater predetermined number of clock pulses,

an output decoder having  $k$  input terminals arranged respectively to receive the  $k$  phase signals and  $q$  output terminals which form the output terminals of the multiphase signal generator, and from each of which the output decoder is arranged to supply an output signal during certain of said phase signals according to the particular output terminal,

a selection decoder having  $k$  input terminals arranged respectively to receive the  $k$  phase signals and  $p$  selection terminals from each of which the selection decoder is arranged to provide a selection signal during certain of said phase signals according to the particular selection terminal, these selection signals being arranged to be provided sequentially without two selection signals being provided at any one time from two selection terminals,

a control circuit comprising  $p$  adjustable elements respectively connected to the  $p$  selection terminals and arranged sequentially and respectively to receive the  $p$  selection signals and to supply frequency control signals to the said clock in response to the said clock in response to the selection signals and of a value in each case in dependence upon the adjustment value of the particular adjustable element.

2. A generator according to claim 1, in which the selection decoder comprises  $p$  OR gate, the outputs of which are respectively connected to the  $p$  selection terminals, and the inputs of which are connected to the  $k$  input terminals of the selection decoder, each of these  $k$  input terminals being connected to only one input of one gate.

3. A generator according to claim 1, in which the counting arrangement comprises: a counter arranged to receive and count the clock pulses and to supply counting pulses when it has counted predetermined number of clock pulses,

a ring type step by step switch arranged to receive the counting pulses and to supply sequentially to each of the  $k$  phase terminals a phase signal beginning with one counting pulse and ending with the following counting pulse.

4. A generator according to claim 3, in which the counter comprises

a frequency divider arranged to receive the clock pulses and constituted by flip flops and

a counting decoder consisting of logic gates of the AND type, the inputs of these gates being connected to the flip-flops and the output of each of these gates being con-

terminal 702 through a resistor 752. The emitter of the transistor 748 is connected up to the resistor 744, so as to constitute a relaxation oscillator of the same type as the one which constitutes the clock pulse oscillator OH, but with a greater recurrence frequency. The clock pulses appearing at the terminals of the resistor 752, are applied to the output terminal 754 connected up to an input of the gate 604.

According to the embodiment in figure 6 described above, it appears obviously that the operation of the system, while remaining cyclic, ceases to be periodic, for the time which passes during a complete cycle depends on the traffic.

The multiphase signal generator which has just been described may be used not only for producing a traffic unit, as in the example chosen, but also for producing advertising lighting where special effects may be obtained due to the existence of periods whose duration may be adjusted, or of automatic telephone reply systems, or even of the driving of machines having several functions operating in a cyclic way, it being understood that yet other applications are evidently possible.

It must be understood that the invention is in no way limited to the embodiment described and illustrated, which has been given only by way of example. Without going beyond the scope of the invention, some arrangements may be changed or some means may be replaced by equivalent means.

More particularly, it is possible to energise the ring type step by step switch CA directly from the clock pulse oscillator OH, without passing through a frequency divider such as DF and a counting decoder such as DC, on condition that the frequency of the oscillator OH may vary between limits sufficiently far apart. In the example of application described, its period should vary from half a second to a hundred seconds.

Moreover, the control circuit CC, the clock oscillator OH and the unit assembly EN may if derived not constitute physically distinct units and be integrated in a time delay circuit assembly.

It is, however, clear that the operation of the clock pulse oscillator OH remains unchanged, that is, that this time delay circuit assembly constitutes a clock system whose operation is the definition of a sequence of clock instants, connected to a part of a unit assembly whose function is to effect switching operations at clock instants of predetermined order.

#### WHAT WE CLAIM IS:—

1. A multiphase signal generator comprising a controllable clock for supplying clock pulses, the frequency of which is controllable by a frequency control signal,
- a counting arrangement arranged to re-

ceive said clock pulses and having  $k$  phase output terminals from which it is arranged to supply sequentially and respectively  $k$  phase signals, each beginning after a predetermined number of clock pulses and ending after a greater predetermined number of clock pulses,

an output decoder having  $k$  input terminals arranged respectively to receive the  $k$  phase signals and  $q$  output terminals which form the output terminals of the multiphase signal generator, and from each of which the output decoder is arranged to supply an output signal during certain of said phase signals according to the particular output terminal,

a selection decoder having  $k$  input terminals arranged respectively to receive the  $k$  phase signals and  $p$  selection terminals from each of which the selection decoder is arranged to provide a selection signal during certain of said phase signals according to the particular selection terminal, these selection signals being arranged to be provided sequentially without two selection signals being provided at any one time from two selection terminals,

a control circuit comprising  $p$  adjustable elements respectively connected to the  $p$  selection terminals and arranged sequentially and respectively to receive the  $p$  selection signals and to supply frequency control signals to the said clock in response to the said clock in response to the selection signals and of a value in each case in dependence upon the adjustment value of the particular adjustable element.

2. A generator according to claim 1, in which the selection decoder comprises  $p$  OR gate, the outputs of which are respectively connected to the  $p$  selection terminals, and the inputs of which are connected to the  $k$  input terminals of the selection decoder, each of these  $k$  input terminals being connected to only one input of one gate.

3. A generator according to claim 1, in which the counting arrangement comprises: a counter arranged to receive and count the clock pulses and to supply counting pulses when it has counted predetermined number of clock pulses,

a ring type step by step switch arranged to receive the counting pulses and to supply sequentially to each of the  $k$  phase terminals a phase signal beginning with one counting pulse and ending with the following counting pulse.

4. A generator according to claim 3, in which the counter comprises

a frequency divider arranged to receive the clock pulses and constituted by flip flops and

a counting decoder consisting of logic gates of the AND type, the inputs of these gates being connected to the flip-flops and the output of each of these gates being con-





connected to a distinct input of the ring type step-by-step switch to supply to that switch one of the counting pulses.

- 5 5. A generator according to claim 4, in which each of the output terminals is provided with a controlled power switch arranged to be rendered conductive by the presence of an output signal on that output terminal, the switch then being suitable for  
10 allowing an alternating current to pass.

6. A generator according to claim 5, including

- 15 a logic circuit arranged to receive on the one hand a detection signal and on the other hand at least one output signal from the output decoder, and to provide an energisation signal when the circuit receives the output signal without receiving the detection signal, and

- 20 a fast oscillator for supplying to the counting arrangement clock pulses at a recurrence frequency greater than that of the said controllable clock, the fast oscillator being controlled by the logic circuit so as to operate  
25 only when the latter supplies said energisation signal.

7. A generator according to claim 6, wherein the logic circuit includes means for the energisation signal to be supplies only after

a predetermined lapse of time has passed 30 from the instant when the logic circuit receives the output signal without receiving the detection signal.

8. A generator according to claim 6, wherein the logic circuit is responsive to at least 35 two output signals from the output decoder and to a corresponding number of detection signals and the logic circuit is arranged to supply an energisation signal when it receives any one of the output signals without receiving at the same time the corresponding 40 detection signal.

9. A multiphase signal generator substantially as hereinbefore described with reference 45 to Figures 1 to 5 or 6 and 7 of the accompanying drawings.

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