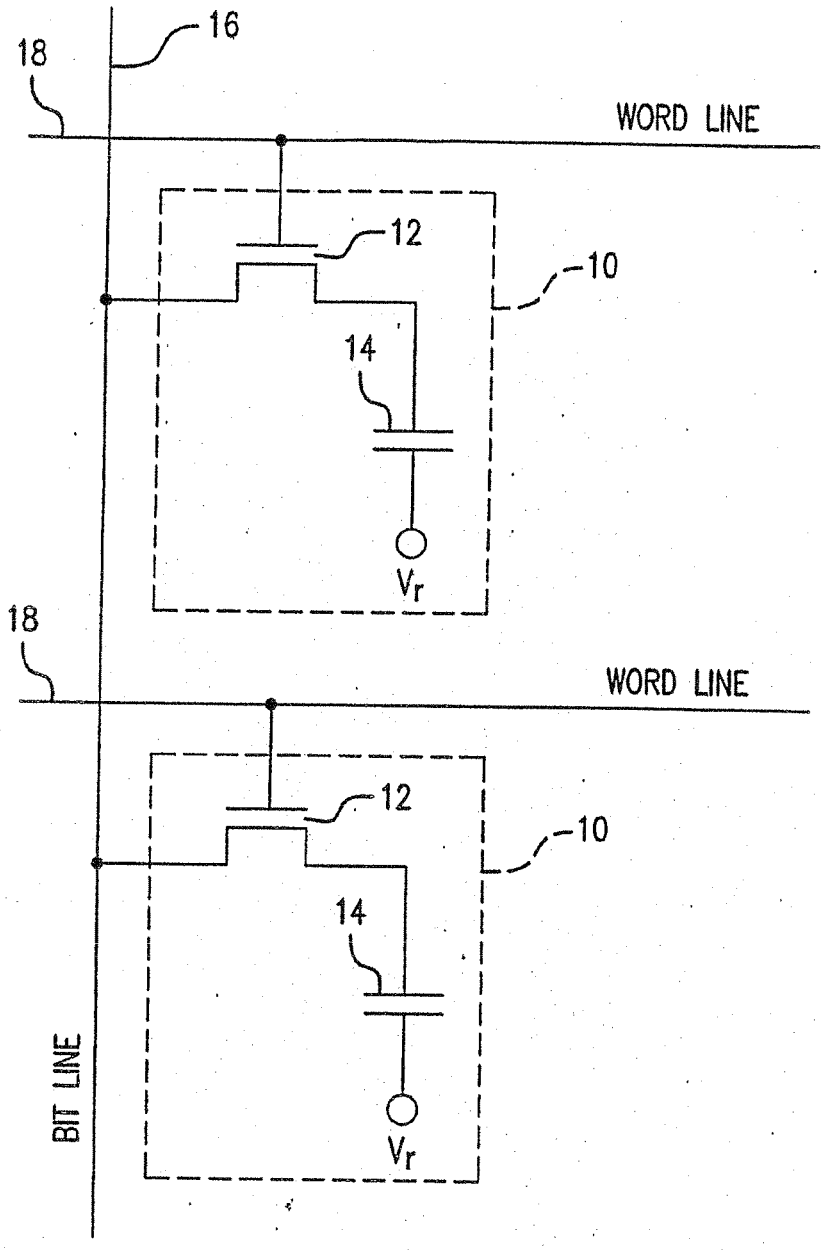


FIG.1A
PRIOR ART

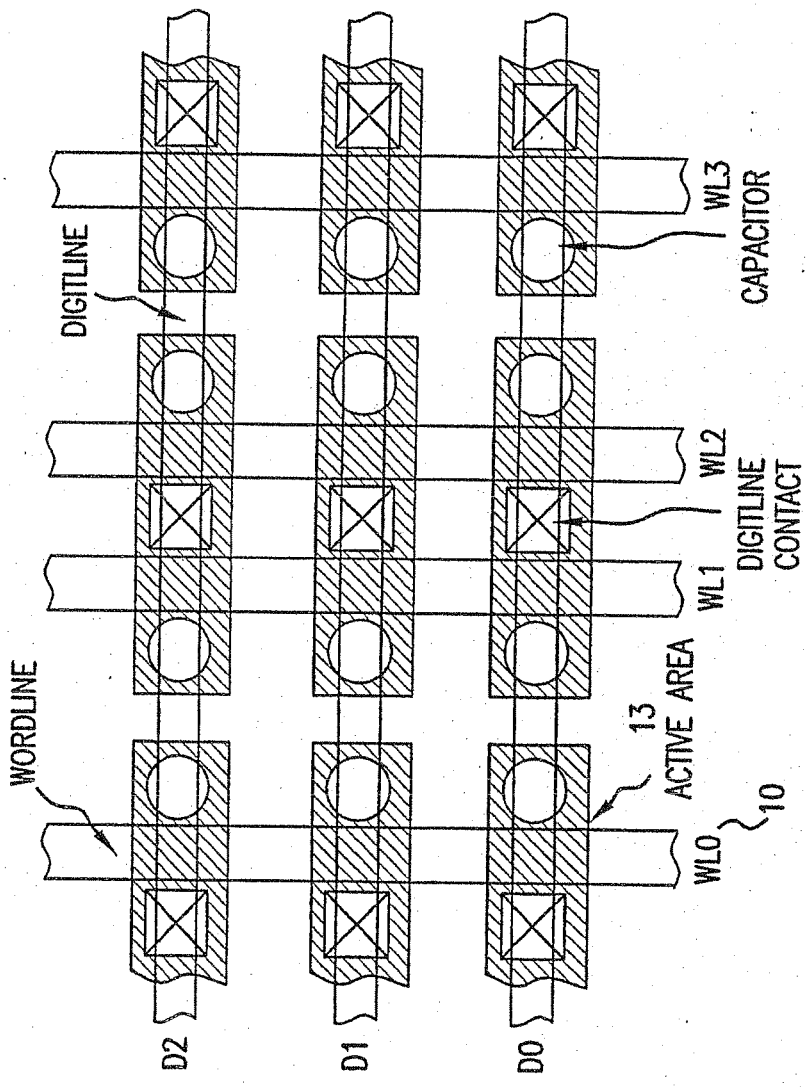


FIG. 1B
PRIOR ART

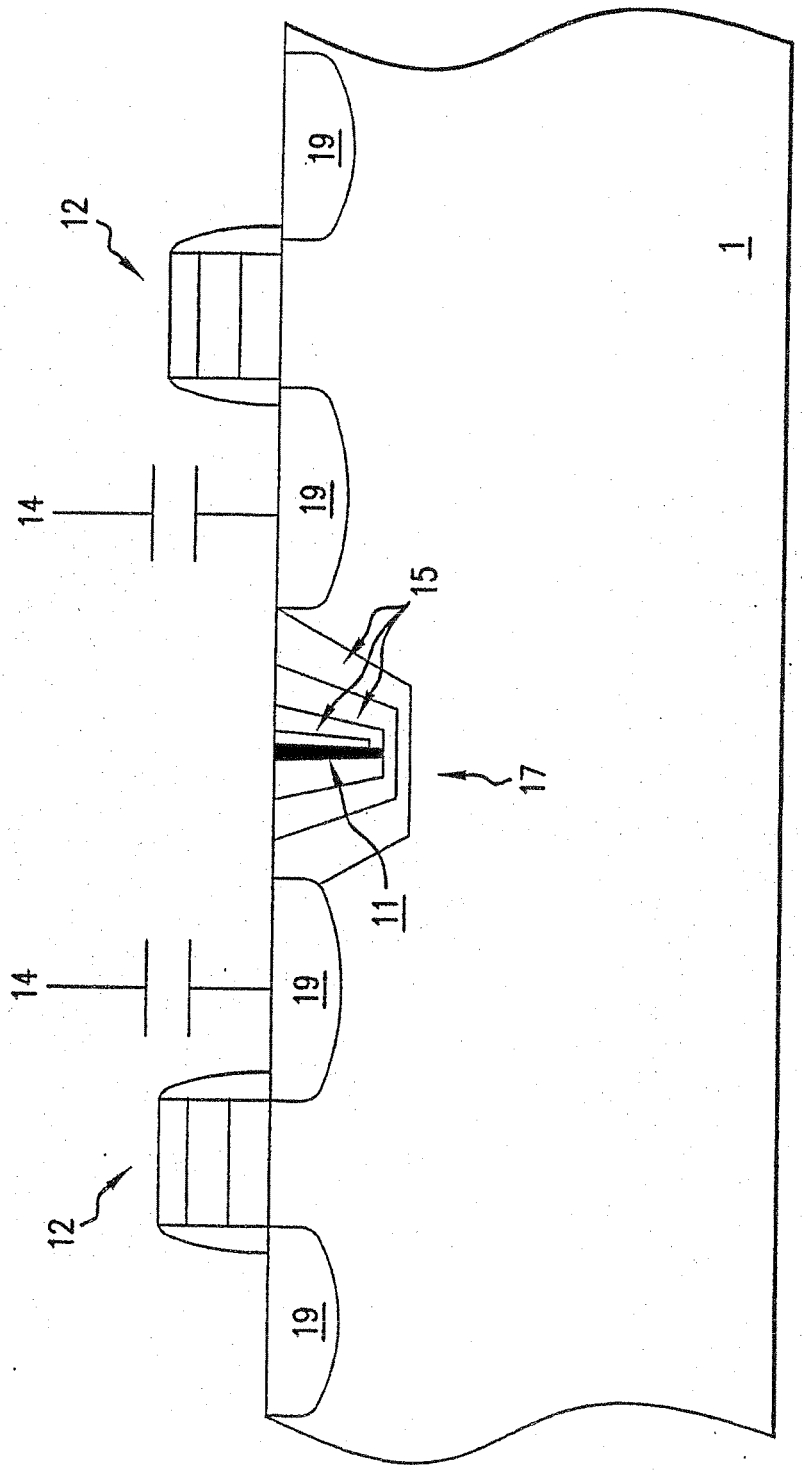


FIG.1C

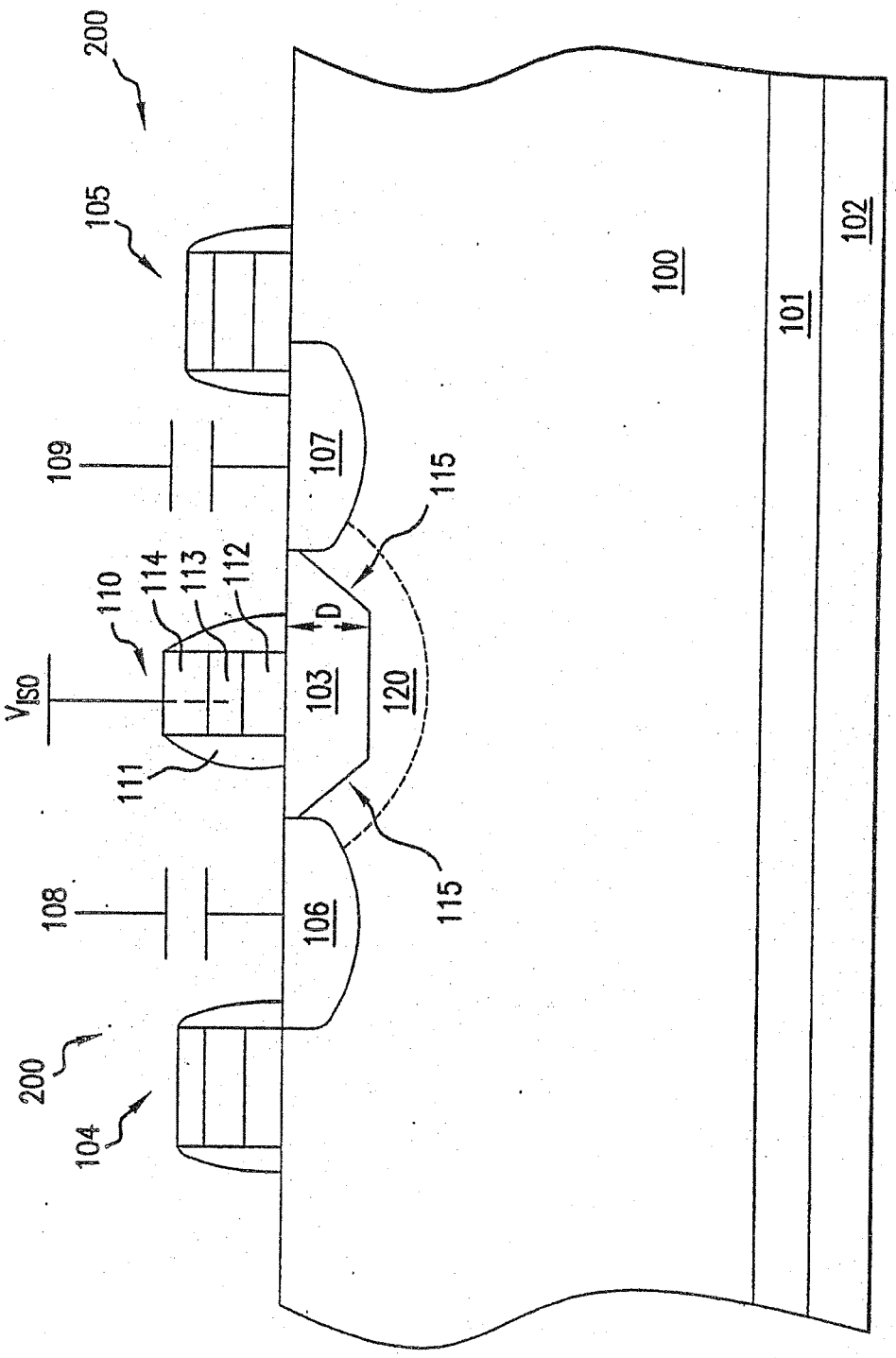

200
105
109
107
115
110
114
113
112
V_{ISO}
103
D
120
111
108
106
115
200
104
100
101
102

FIG.2A

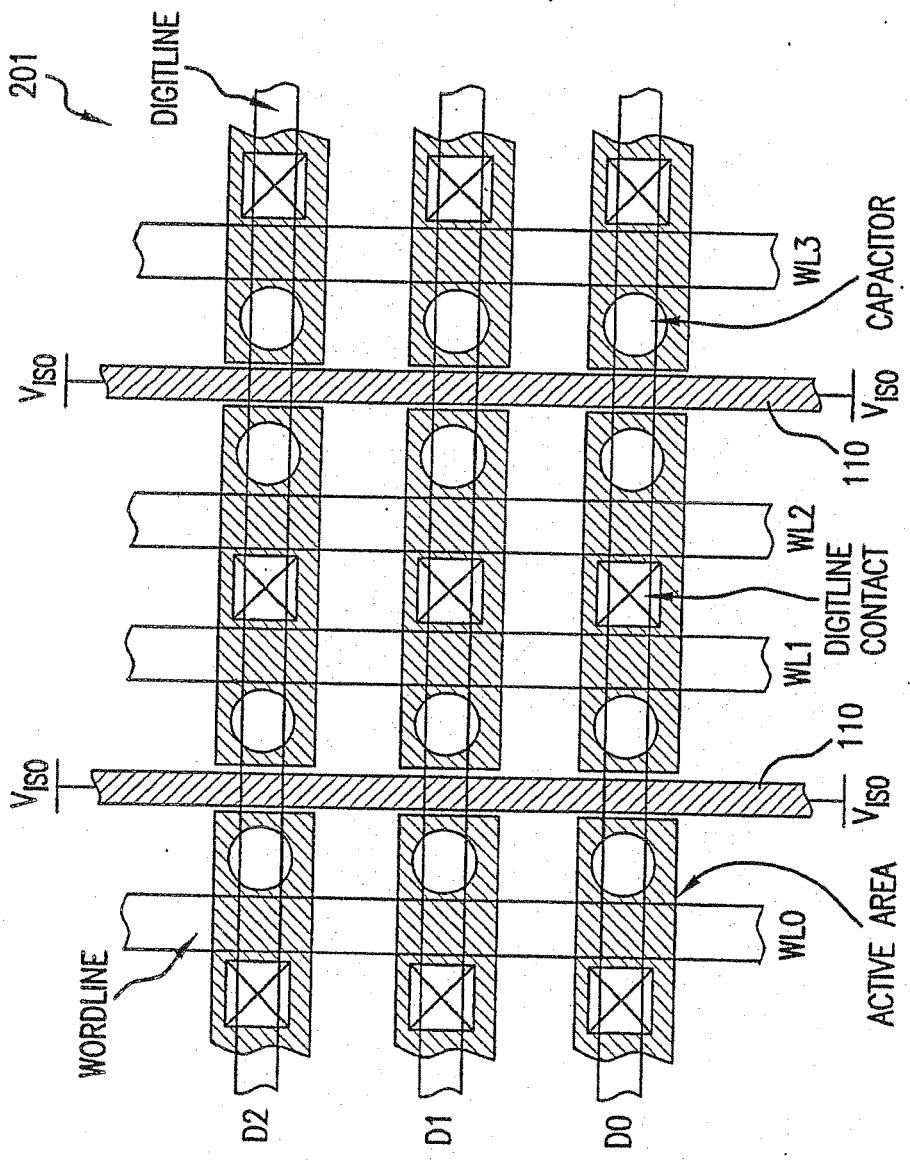

201
DIGITLINE
WL3
CAPACITOR
V_{ISO}
V_{ISO}
110
WL2
DIGITLINE CONTACT
WL1
110
V_{ISO}
V_{ISO}
WORDLINE
WL0
ACTIVE AREA
D2
D1
D0

FIG.2B

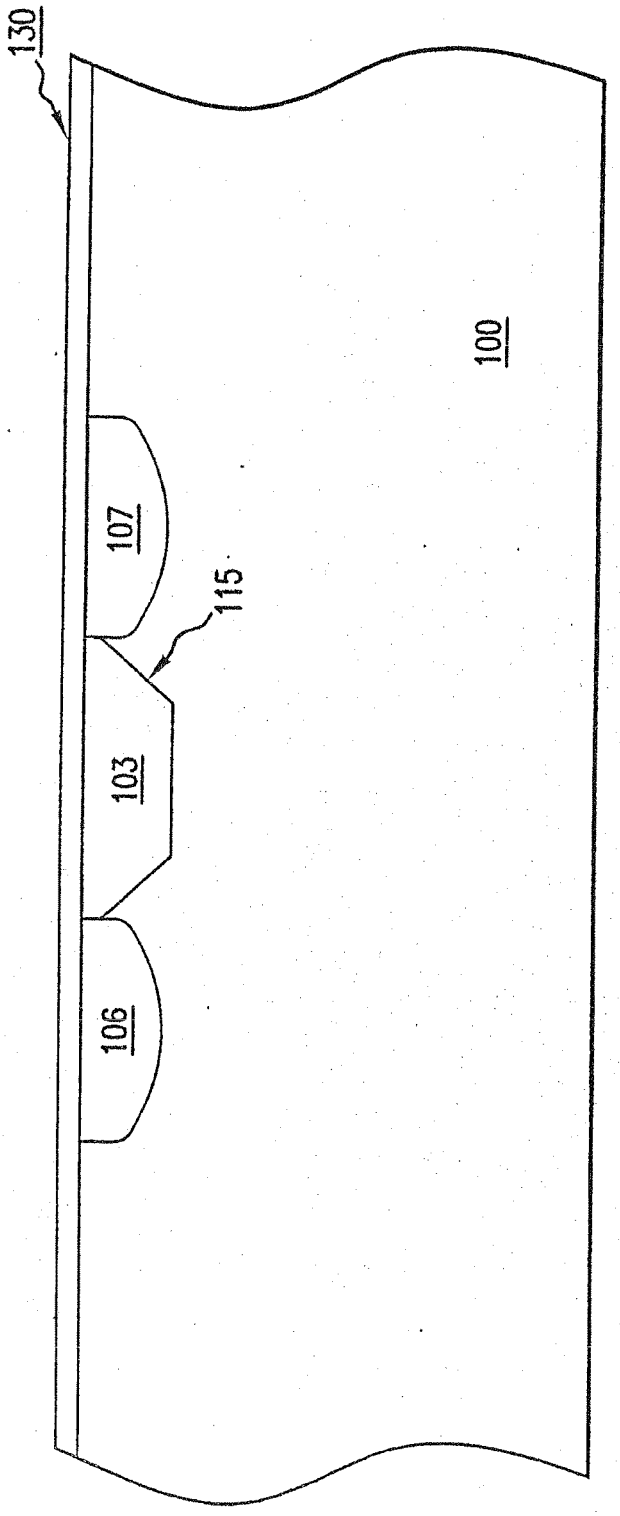


FIG.3

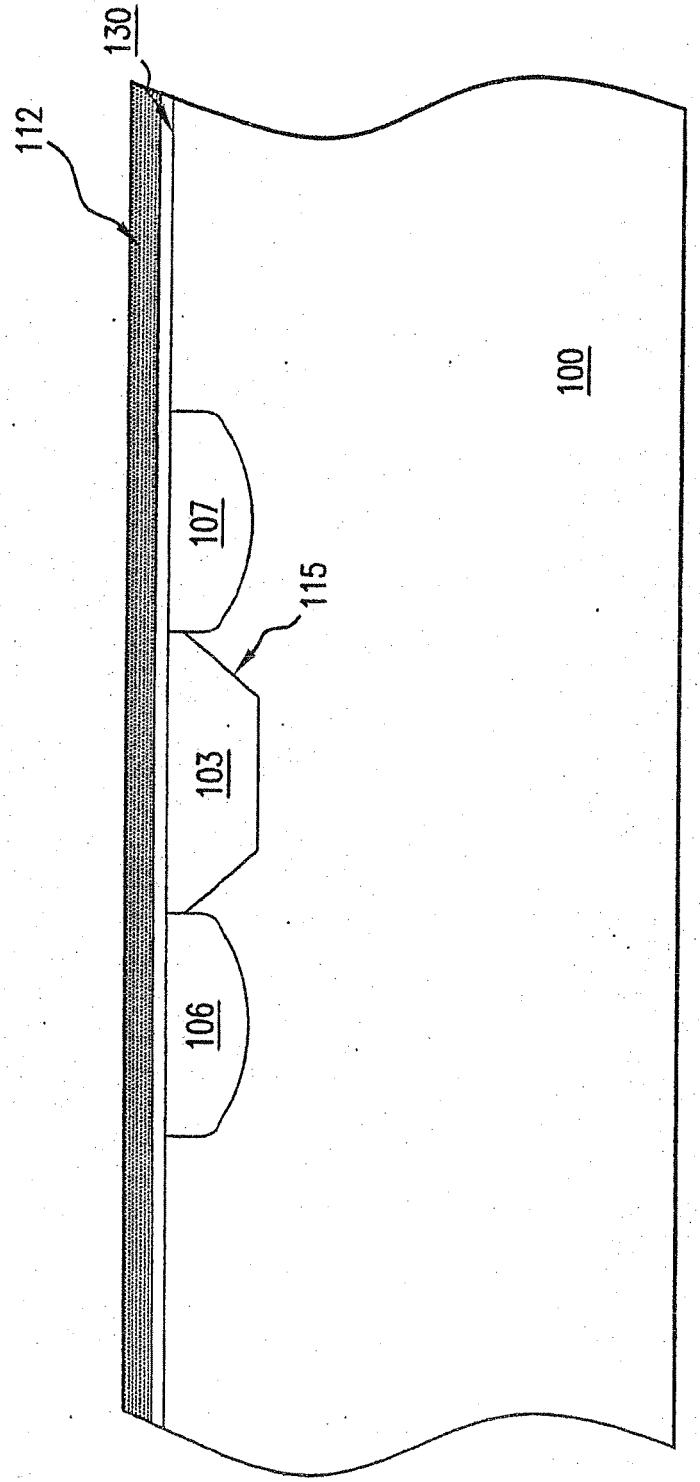


FIG.4

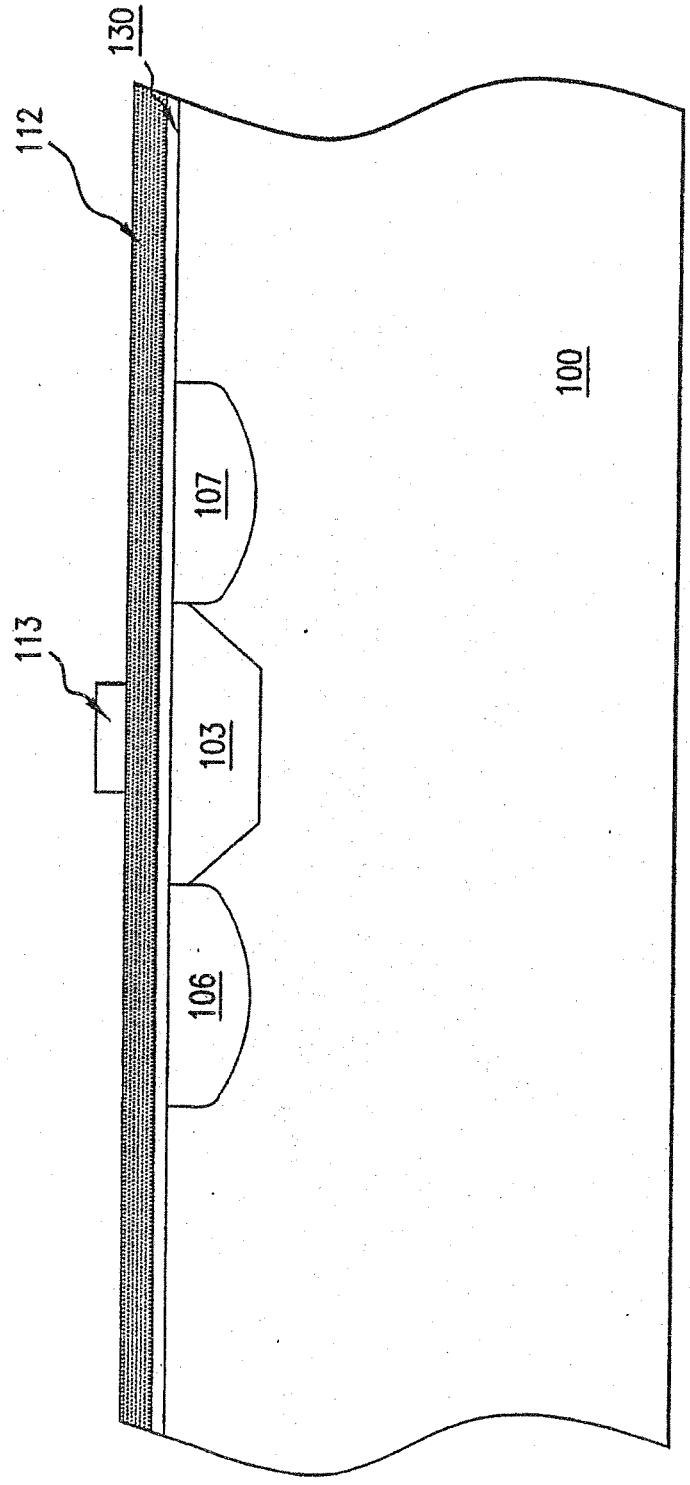


FIG.5

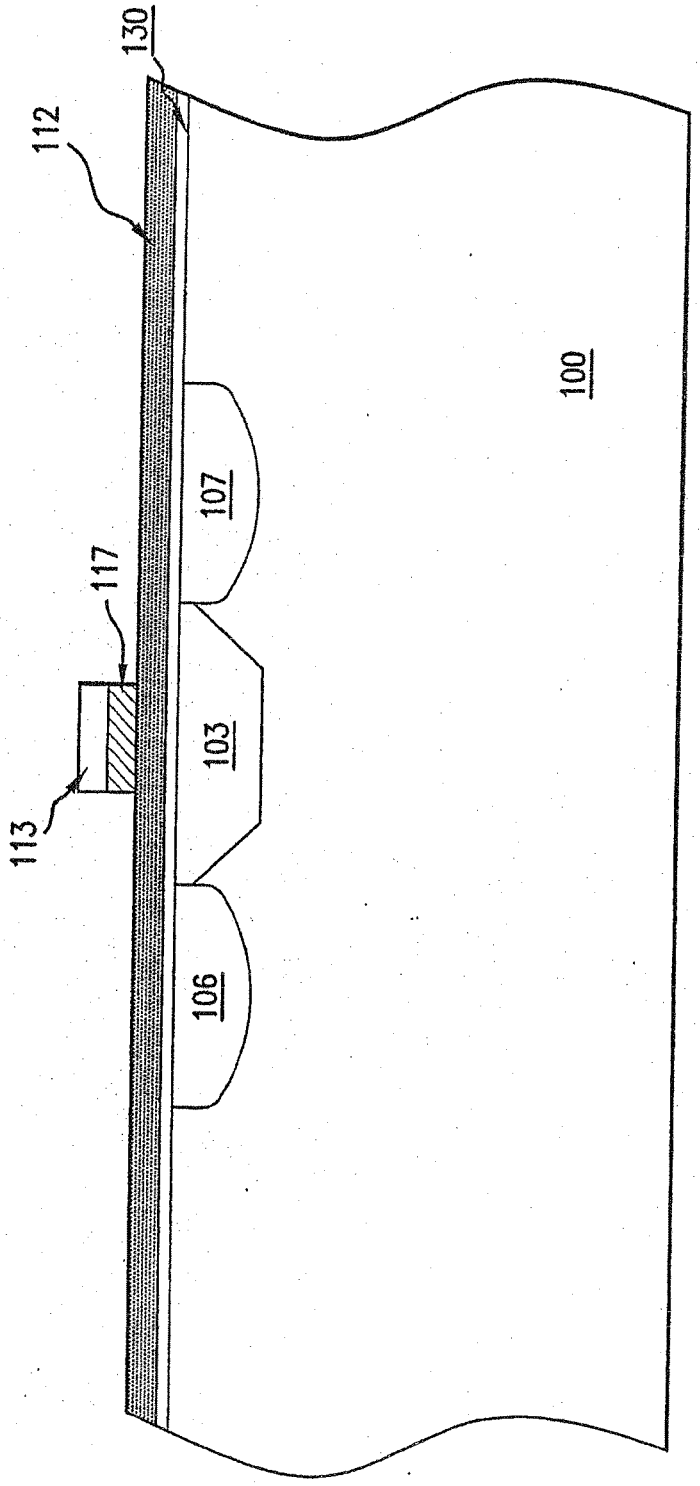


FIG.5A

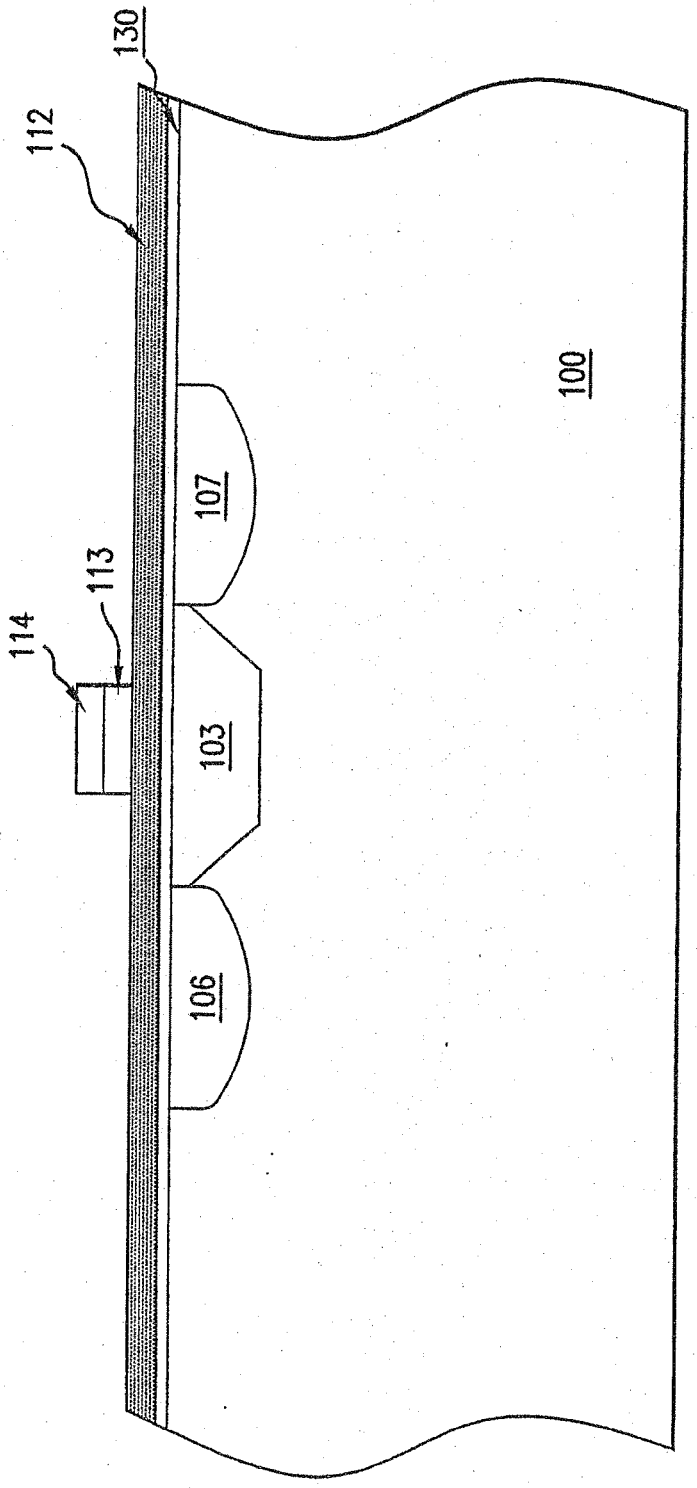


FIG.6

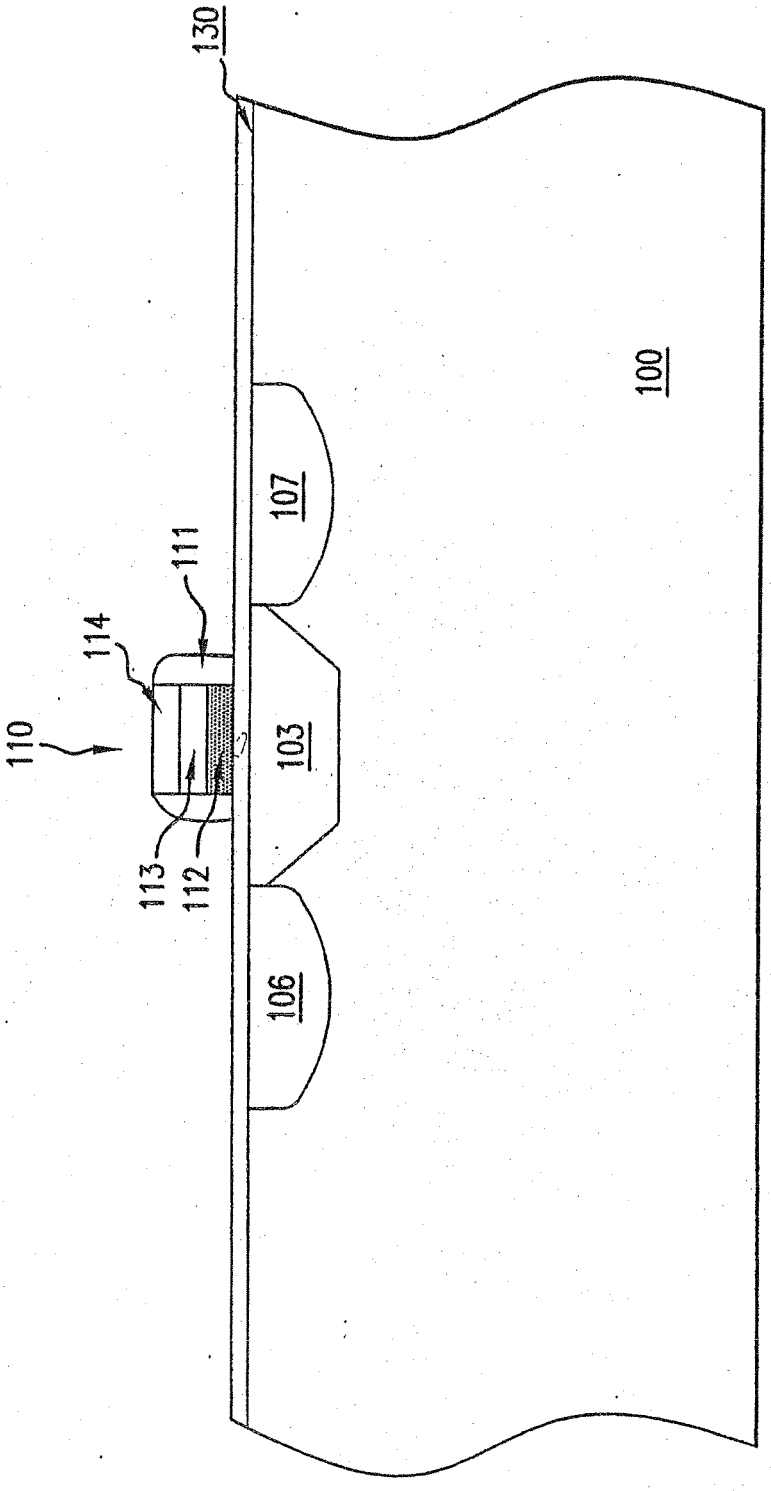


FIG. 7

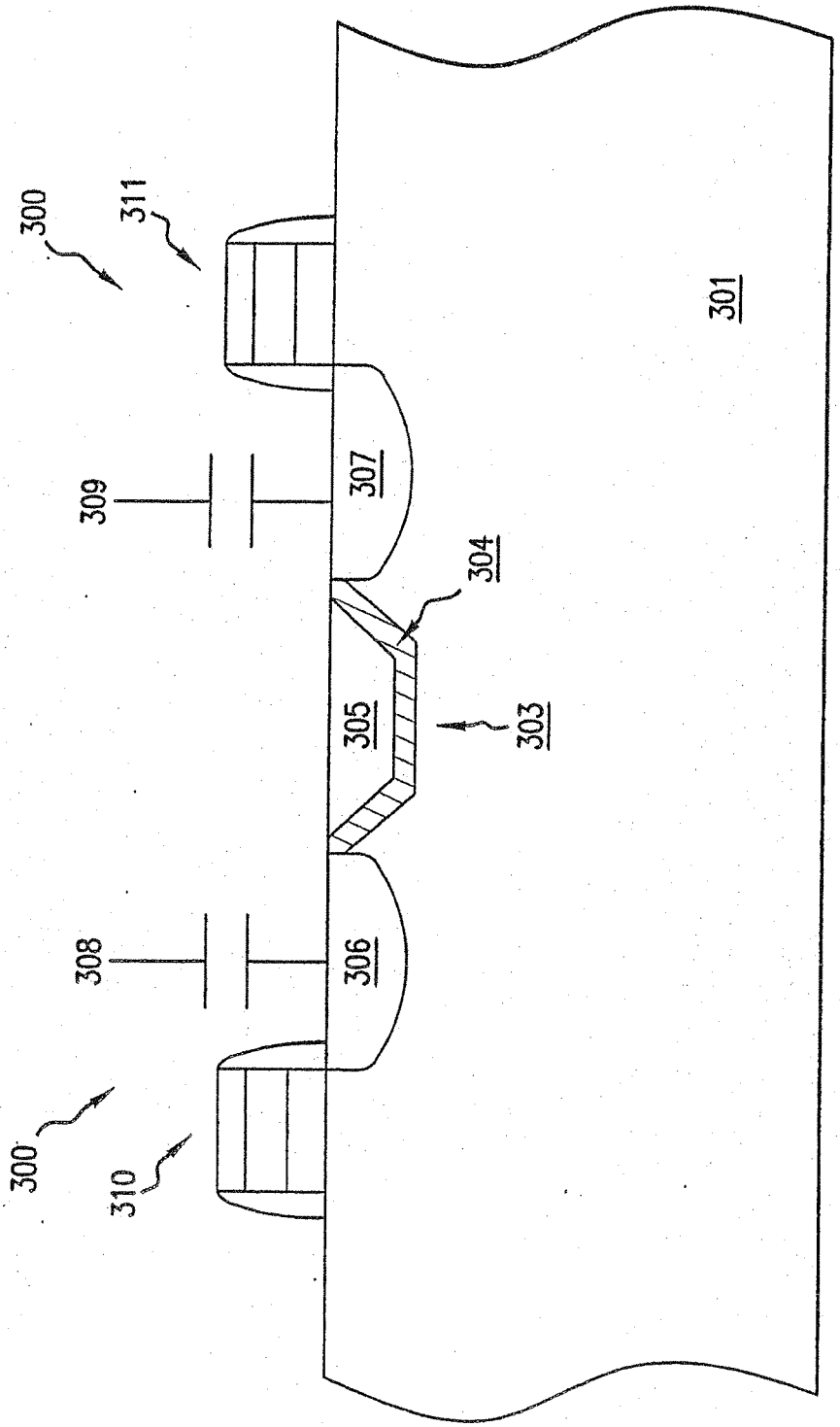


FIG.8

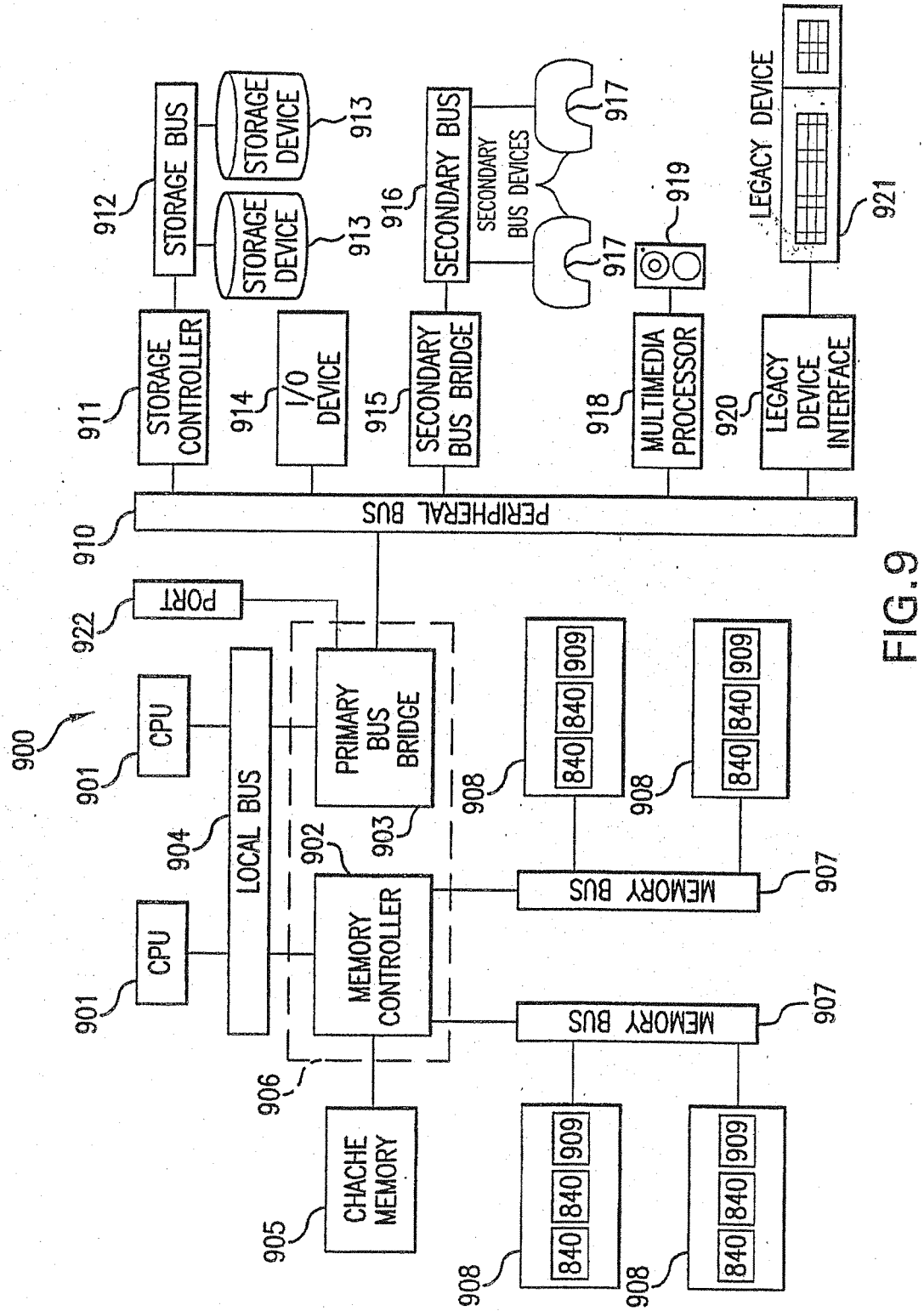

900
CPU
901
CPU
901
PORT
922
PERIPHERAL BUS
910
STORAGE CONTROLLER
911
I/O DEVICE
914
SECONDARY BUS BRIDGE
915
MULTIMEDIA PROCESSOR
918
LEGACY DEVICE INTERFACE
920
STORAGE BUS
912
STORAGE DEVICE
913
STORAGE DEVICE
913
SECONDARY BUS
916
SECONDARY BUS DEVICES
917
917
919
LEGACY DEVICE
921
LOCAL BUS
904
PRIMARY BUS BRIDGE
903
MEMORY CONTROLLER
902
CHACHE MEMORY
905
906
MEMORY BUS
907
MEMORY BUS
907
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840
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FIG.9