

PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO BATTERY VOLTAGE DETECTOR CIRCUITS

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese company of 3-4, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to battery voltage detector circuits and more specifically to battery voltage detector circuits of the type in which warning indication of the approach of the end of the useful life of a battery is given by comparing the battery voltage with the threshold voltage of a field effect transistor (FET) and utilising the result of comparison to give the required warning indication.

The primary application of the invention is to electronic timepieces though it can be applied with advantage to other electronic or electrical instruments driven by small batteries such as are used in electronic timepieces — notably to table calculators, and analog digital converters. Quartz and other high accuracy electronic timepieces are commonly driven by very small batteries which last quite a long time — somewhere about a year, usually — and it would be of considerable practical advantage to provide such a timepiece — especially a watch, in which there is room for only a very small battery with simple and compact means whereby warning would be given that the battery has been run down sufficiently to need to be changed. As will be seen later there are, however, considerable practical difficulties in the way of providing such means in a satisfactory manner and one object of the present invention is to overcome these difficulties.

According to this invention there is provided a battery voltage detecting circuit of the kind referred to, said circuit comprising at least two FET stages in a cascade of stages one of said stages being arranged to change its output state when the battery voltage falls to a predetermined value which is related to the threshold voltage of the FET in said one stage and one or more of the remaining FET stages being arranged to present a temperature characteristic such as substantially to compensate for the temperature characteristic of said one FET stage over a range of battery voltage between normal battery voltage and said predetermined value. The stages may comprise FETs of the MOS type or of the junction type.

As regards "threshold voltage" and "predetermined value" it should be pointed out that, because the pre-determined voltage is controllable by the value of the load resistance (or in some other way) the threshold voltage is not always equal thereto. For example, in an experimentally tested circuit in accordance with the invention, the absolute value of the threshold voltage was between 0.3 and 0.7V and the absolute value of the pre-determined voltage was approximately 1.45 V.

The compensating temperature coefficient may be presented by the FET stage immediately following said one stage in the cascade series and a number of arrangements are possible. In one arrangement there is employed in said one stage a P-channel FET having a drain current temperature coefficient which is negative over said range and an N-channel FET is employed in the immediately following stage. In another there is employed in said one stage an N-channel FET having a drain current temperature coefficient which is negative over said range and a P-channel FET is employed in the immediately following stage. In yet another there is employed in said one stage a P-channel FET having a drain current temperature coefficient which is positive over said range and a -channel FET is employed in the immediately following stage. And i yet another arrangement there is employed in said

one stage an N-channel FET having a drain current temperature coefficient which is positive over said range and an N-channel FET is employed in the immediately following stage. In any of these arrangements said immediately following stage may comprise a single FET with a load resistor which may be constituted by an MOS resistance presented by a MOS transistor.

In a further embodiment of the invention the compensating temperature characteristic is presented by a complementary MOS inverter stage.

Attention is directed to our co-pending specification Nos. 16589/75, Serial No. 1,475,841, and 33390/75, Serial No. 1,508,815, which describe inventions which are fairly closely related to the present invention. In particular the former specification 16589/75 should be referred to as regards the difference between the threshold voltage and the pre-determined voltage and 33390/75 (Serial No. 1,508,815) should be referred to as regards the relation between these two voltages.

The invention is illustrated in and further explained with reference to the accompanying drawings in which:—

Figure 1 which is provided for explanatory purposes is a basic circuit diagram of a known battery voltage detecting circuit,

Figure 2 graphically shows the relationship between the battery voltage E_1 and the output voltage E_2 of the transistor 2 in Figure 1,

Figure 3 shows graphically the relationship between the gate voltage — threshold voltage difference ($V_G - V_{TH}$) and the drain current (I_D) temperature coefficient of the transistor 2 of Figure 1,

Figure 4 is a circuit diagram of one embodiment of this invention,

Figure 5 shows graphically the nature of the improvement in temperature characteristic obtainable with this invention as compared with a known battery voltage detecting circuit as shown in Figure 1, and

Figure 6 is a circuit diagram of another embodiment of the invention.

The basic circuitry of a known battery voltage detecting circuit utilising the threshold voltage of a field effect transistor and as previously provided in electronic timepieces is shown in Figure 1. Here 1 is the power supply battery of the timepiece; 2 is an enhancement type P-channel MOS FET; 3 is a load resistance; 4 and 5 are complementary inverters of the P-channel MOS FET type; and 6 is the output terminal of the whole arrangement. For the sake of brevity, P-channel and N-channel MOS FETs will be hereinafter referred to by the commonly used abbreviations, P. MOS FET and N. MOS FET respectively. 1 is, as stated, in fact a battery but, for convenience in explanation, it is represented as a variable voltage source because, with continued use, its voltage E_1 falls. Figure 2 illustrates graphically the relation between the voltage E_1 and the output voltage E_2 set up across the load resistance 3 of the P. MOS FET 2 in Figure 1. If the resistance 3 is of sufficiently high value, the following statements apply, as will be seen from Figure 2; E_2 is larger than the threshold voltage V_{TH} of the P. MOS FET 2, E_2 will be equal to E_1 because the P. MOS FET 2 is conductive. The threshold voltage V_{TH} of the P. MOS FET 2 is minus, taking the source electrode potential as standard and, to take a practical case, it may be from -0.3 to -0.7 volts. However, the values of $|V_{TH}|$ and $|V_G|$ and $(|V_G - V_{TH}|)$ in Figures 2 and 3 are absolute (but not exact) values. When the voltage E_1 falls away and approaches the threshold voltage V_{TH} , voltage E_2 decreases rapidly because the P. MOS FET 2 is changing from the conductive to the non-conductive state. When E_1 becomes equal to or less than the threshold voltage V_{TH} , E_2 becomes zero.

When E_2 becomes equal to the threshold voltage of the inverter 4 the output at terminal 6 reverses and this indicates that the battery voltage has dropped. In practice, however, the P. MOS FET 2 is formed as part of an integrated circuit structure on the same substrate as the complementary MOS, inverters 4 and 5 and accordingly the threshold voltage V_{TH} approaches one-half of the battery voltage, the load resistance 3 has to be of relatively low value and the slope of the E_1/E_2 curve in Figure 2 has to be gentle in order that, as is required, in practice, a small drop of battery voltage — a drop to between 90 and 95 percent of normal battery voltage can be detected. The point at which the stage of conductivity of the P. MOS FET 2 switches over is somewhat vague — i.e. it is not a sharply defined point — but, nevertheless, the battery voltage value at which detection occurs is quite definite because the value of E_2 is detected by its relation to the threshold voltage of the inverter 4. In the manner above described, therefore, a circuit as shown in Figure 1 can utilise the threshold voltage of a field effect transistor to enable a drop in the voltage of a timepiece battery to a point at which the battery should be replaced, to be detected and, therefore, indicated. However the known circuit has a defect which very greatly reduces its practical utility and makes it far from satisfactory. This defect arises from the fact that it is markedly temperature conscious, a change in ambient temperature producing a change in the battery voltage value at which the P. MOS FET changes state. An arrangement as shown in Figure

1 is therefore liable to result in an indication that a battery is approaching the end of its useful life and should be replaced even though this is not the fact, the erroneous indication being produced merely as an effect of temperature change. Similarly a change in temperature may cause the circuit to fail to operate at a time when, in fact, the battery is near the end of its useful life.

The present invention seeks to provide improved battery voltage detecting circuits of the kind referred to and the temperature characteristics of which shall be such as to eliminate or reduce to acceptable proportions the defect above mentioned.

In the known battery voltage detecting circuit shown in Figure 1 it is the P. MOS. FET 2 in the first stage of the circuit which has most effect on the temperature characteristic of the circuit as a whole, the complementary inverters 4 and 5 being relatively unimportant from this point of view. The output voltage of a P. MOS. FET is substantially proportional to the drain current and the temperature coefficient of the drain current I_D can be expressed by the following equation if the drain voltage V_D is constant:—

$$\frac{1}{I_D} \cdot \frac{dI_D}{dT} = \frac{1}{\mu n} \cdot \frac{d\mu n}{dT} + \frac{-1}{V_G - V_{TH}} \cdot \frac{dV_{TH}}{dT} \quad \dots (1)$$

where V_G is the voltage between the gate and source (hereinafter called the gate voltage); V_{TH} is the threshold voltage; μn is the electron mobility within the inversion layer; and T is temperature.

In the case of the P. MOS. FET 2 of Figure 1,

$$\frac{d\mu n}{dT} \text{ and } \frac{dV_{TH}}{dT}$$

have negative values so that it is in theory possible to make the temperature dependence of the drain current I_D of the MOS. FET positive, negative or zero by suitably selecting the values of $(V_G - V_{TH})$ and

$$\frac{dV_{TH}}{dT}$$

Figure 3 shows graphically the relationship between $(V_G - V_{TH})$ and the drain current temperature coefficient

$$\frac{1}{I_D} \cdot \frac{dI_D}{dT}$$

Although theoretically it is possible to make the I_D temperature coefficient zero, it is practically very hard to achieve this. V_{TH} has to be raised to about 1.0 V in order to establish it at an optimum value and make the I_D temperature coefficient zero in the vicinity of $V_G = 1.5$ V. However, since in practice the battery voltage detecting circuit of Figure 1 is formed on the same integrated circuit (I.C.) with other circuits of the timepiece, the threshold voltage of all these must be correspondingly raised. This is undesirable and has many bad effects. One is that the voltage characteristic of the time standard oscillating circuit of the timepiece gets worse so that the time accuracy becomes less; another is that the driving current in the time display driving circuit of the timepiece is reduced; and a third is that there is apt to be more "noise" in the frequency divider of the timepiece. For these and other reasons it is desirable not to make the value of V_{TH} higher than can be helped. As will be seen later the present invention enables this requirement to be satisfied and to provide voltage detecting circuits of the kind referred to wherein the required temperature compensation is obtained without deterioration of efficiency in other respects. As will also be seen later the invention achieves its objects by a circuit in which fluctuation of output voltage from the first stage portion of the battery voltage detecting circuit due to the temperature variation is substantially cancelled out by the temperature characteristic of a field effect transistor (FET) or transistors in a following circuit or circuits.

In explaining the operation of this invention, the temperature dependences of the output voltage and the switching voltage of the complementary inverters in Figure 1 will first be described. The I_D temperature coefficients of both N. and P. MOS. FETs are expressible by equation 1 above. At that value of gate voltage at which the output reverses, i.e. in the vicinity of the switching voltage, the gate voltages of both P. and N. MOS. FETs have values near the threshold voltage. Accordingly at such gate voltages, the temperature coefficient is positive. For this reason, the drain-source resistance of either a P. or an N. MOS. FET changes in the same way as the temperature, with the result that there is little dependence on temperature as regards switching voltage or output voltage. On the other hand, in an inverter with a single MOS. FET in which the load is a resistance, the load resistance does

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not possess a temperature characteristic such as to compensate for the temperature characteristic of the MOS. FET, so that the temperature characteristic directly affects the switching voltage and the output voltage. The present invention takes advantage of these facts to improve the temperature characteristics of a voltage detecting circuit of the kind referred to by substantially cancelling out fluctuations of output voltage which would otherwise be caused by varying temperature effects at the first stage portion (2 of Figure 1) by compensating effects of a following MOS. FET inverter the load of which is the resistance of the next stage portion.

Figure 4 shows one embodiment of the invention. In this figure E_1 and E_2 have the same significance as in Figure 1 as do the references 1, 2 and 3. However, the next stage (that to which the voltage E_2 is applied) comprises an N. MOS. FET 7 with a load resistance 8. The rest of the circuit of Figure 4 is as in Figure 1. To quote practical figures for the circuit of Figure 4 the threshold voltage of the P. MOS. FET 2 is 0.7 V and the gate voltage at which the I_D temperature coefficient becomes zero is approximately 1.1 V. In a case in which the predetermined voltage to be detected is 1.5 V, the I_D temperature coefficient of the P. MOS. FET 2 is, as will be appreciated from Figure 3 negative within a range of battery voltage from a normal value of 1.58 V to the predetermined value (1.50 V) of voltage to be detected.

So long as voltage from the battery is between 1.58 V and 1.50 V the P. MOS. FET and the N. MOS. FET 7 will be ON i.e. conductive at the normal temperature. As described above, since the I_D temperature coefficient of a P. MOS. FET is negative within this range of supply voltage, the resistance between source and drain of the P. MOS. FET 2 will increase with rise of temperature and its output voltage E_2 will decrease. This voltage E_2 is the gate/source voltage of the N. MOS. FET 7 so that, as E_2 decreases with rise of temperature, there is an increase in the drain/source resistance of the N. MOS. FET 7. However ($V_G - V_{TH}$) is near zero because the voltage between the gate and source of N. MOS. FET 7 has a value near the threshold voltage. Accordingly, the I_D temperature coefficient of the N. MOS. FET 7 in itself is positive, and the resistance between the drain and the source decreases due to the rise of temperature.

Thus the influence on the drain/source resistance of the N. MOS. FET 7 by fluctuation of the voltage E_2 due to temperature variation is compensated by the temperature characteristic of the N. MOS. FET 7 itself, as the result of which the temperature dependence of the output voltage E_3 of the N. MOS. FET 7 is reduced and the temperature characteristic of the voltage detecting circuit as a whole is improved.

The above explanation has been given in terms of temperature rise but, as will now be apparent, there is also compensation if a fall in temperature occurs.

A few comments will now be given as regards the degree of temperature compensation obtained. Referring to Figure 3, the gate voltage operating points of the P. MOS. FET 2 and the N. MOS. FET 7 are the points a and c respectively. The absolute value of the temperature coefficient at point c is high because V_G is close to the threshold voltage V_{TH} . It is nearly ten times as high as at point a . If, therefore, it is assumed that the I_D temperature coefficient is reflected as it is on the output voltage, a variation ΔE_2 of the voltage E_2 by temperature will have an amplified influence of the output voltage of the N. MOS. FET 7 at the next stage due to the voltage amplification factor β of that stage. In other words the variation of output voltage from the N. MOS. FET 7 will be $\beta \Delta E_2$. Since the variation of the output voltage of the N. MOS. FET 7 due to temperature variation effects upon that transistor will be about 10 times as much as ΔE_2 , substantially complete compensation can be obtained by making the voltage amplification β of said N. MOS. FET about 10. An optimum value of β can readily be obtained and to facilitate adjustment of this the load resistance 8 can be made adjustable.

Figure 5 shows at A the temperature characteristic of a circuit in accordance with this invention and as shown in Figure 4 as compared with that (as shown at B) of an otherwise comparable known circuit as shown in Figure 1 using a complementary inverter (4 of Figure 1) in the second stage.

In the embodiment above described with reference to Figure 4 a P. MOS. FET 2 is used in the first stage and an N. MOS. FET 7 is used in the next stage. However this is not essential, for an N. MOS. FET having a negative I_D temperature coefficient within the range of battery voltage from normal voltage down to the predetermined voltage to be detected could be used in the first stage and temperature compensation obtained by using a P. MOS. FET in the next stage. This modification is shown in Figure 6 in which the N. MOS. FET and the P. MOS. FET are referenced 9 and 11 respectively and 10 and 12 are, respectively, the load resistances of these transistors.

In the case in which a MOS. FET with a positive temperature characteristic over the battery voltage range from normal battery voltage to the predetermined voltage to be

detected is used in the first stage portion, if the first stage contains a P. MOS. FET, temperature compensation is obtained by using a P. MOS. FET in the next portion, and, similarly if the first stage contains an N. MOS. FET, temperature compensation is obtained by using an N. MOS. FET in the next stage. In the circuits of Figures 4 and 6 load resistances of the FETs are shown as ordinary resistors (3 or 10 and 8 or 12). However, this is not necessary or even the most attractive way of carrying out the invention, for MOS resistances can be used and the invention will operate in the manner described if the load resistance (8 or 12) of the second stage is an MOS resistance.

As will now be seen the essence of the invention resides in obtaining compensation for output voltage variations produced by temperature variations in a first stage FET by means of the temperature characteristic of an FET in the next stage and/or in a subsequent stage in cascade with the first stage. Accordingly, the invention is not limited to the circuits already described and illustrated and numerous modifications are possible. For example the second stage could consist (as it does in the known circuit of Figure 1) complementary MOS inverter but with the P and N areas of the FETs in the said inverter made suitably different from each other so that the required compensating temperature coefficient is presented by the said complementary inverter which accordingly provides the required temperature compensation is made.

Again, although in the embodiments above described MOS FETs are used, FETs of the [con]junction type could be used.

Although an important practical application of the invention is to the battery voltage detecting circuits for electronic timepieces, the invention is not limited to this application. Other important applications of the invention are to battery voltage detecting circuits in electronic table calculators, analog/digital converters, electrical thermometers and, indeed, electronic and electric instruments generally.

Circuit arrangements in accordance with this invention lend themselves admirably to embodiments in monolithic integrated circuit structures. A considerable practical advantage of the invention, not previously mentioned, is that temperature compensation is obtained without having to resort to the use of temperature sensitive devices such as thermistors.

Any of the above described embodiments of the invention may be used to give warning that the battery should be replaced by providing an indicator (not shown) responsive to the logic state at the final output terminal (6 in Figures 4 and 6).

WHAT WE CLAIM IS:—

1. A battery voltage detecting circuit comprising at least two FET stages in a cascade series of stages, one of said FET stages being arranged to change its output state when the battery voltage falls to a predetermined value which is related to the threshold voltage of the FET in said one stage and one or more of the remaining FET stages being arranged to present a temperature characteristic such as substantially to compensate for the temperature characteristic of said one FET stage over a range of battery voltage between normal battery voltage and said predetermined value.

2. A circuit as claimed in claim 1 wherein the FET stages are MOS. FET stages.

3. A circuit as claimed in claim 1 wherein the FET stages are junction type FET stages.

4. A circuit as claimed in any of the preceding claims wherein the compensating temperature characteristic is presented by the FET stage immediately following said one FET stage in the cascade series.

5. A circuit as claimed in claim 4 wherein there is employed in said one FET stage a P-channel FET having a drain current temperature coefficient which is negative over said range and an N-channel FET is employed in the immediately following stage.

6. A circuit as claimed in claim 4 wherein there is employed in said one FET stage an N-channel FET having a drain current temperature coefficient which is negative over said range and a P-channel FET is employed in the immediately following stage.

7. A circuit as claimed in claim 4 wherein there is employed in said one FET stage a P-channel FET having a drain current temperature coefficient which is positive over said range and a P-channel FET is employed in the immediately following stage.

8. A circuit as claimed in claim 4 wherein there is employed in said one FET stage an N-channel FET having a drain current temperature coefficient which is positive over said range and an N-channel FET is employed in the immediately following stage.

9. A circuit as claimed in any of claims 5 to 8 wherein said immediately following stage



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detected is used in the first stage portion, if the first stage contains a P. MOS. FET, temperature compensation is obtained by using a P. MOS. FET in the next portion, and, similarly if the first stage contains an N. MOS. FET, temperature compensation is obtained by using an N. MOS. FET in the next stage. In the circuits of Figures 4 and 6 load resistances of the FETs are shown as ordinary resistors (3 or 10 and 8 or 12). However, this is not necessary or even the most attractive way of carrying out the invention, for MOS resistances can be used and the invention will operate in the manner described if the load resistance (8 or 12) of the second stage is an MOS resistance.

As will now be seen the essence of the invention resides in obtaining compensation for output voltage variations produced by temperature variations in a first stage FET by means of the temperature characteristic of an FET in the next stage and/or in a subsequent stage in cascade with the first stage. Accordingly, the invention is not limited to the circuits already described and illustrated and numerous modifications are possible. For example the second stage could consist (as it does in the known circuit of Figure 1) complementary MOS inverter but with the P and N areas of the FETs in the said inverter made suitably different from each other so that the required compensating temperature coefficient is presented by the said complementary inverter which accordingly provides the required temperature compensation is made.

Again, although in the embodiments above described MOS FETs are used, FETs of the [con]junction type could be used.

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Circuit arrangements in accordance with this invention lend themselves admirably to embodiments in monolithic integrated circuit structures. A considerable practical advantage of the invention, not previously mentioned, is that temperature compensation is obtained without having to resort to the use of temperature sensitive devices such as thermistors.

Any of the above described embodiments of the invention may be used to give warning that the battery should be replaced by providing an indicator (not shown) responsive to the logic state at the final output terminal (6 in Figures 4 and 6).

WHAT WE CLAIM IS:—

1. A battery voltage detecting circuit comprising at least two FET stages in a cascade series of stages, one of said FET stages being arranged to change its output state when the battery voltage falls to a predetermined value which is related to the threshold voltage of the FET in said one stage and one or more of the remaining FET stages being arranged to present a temperature characteristic such as substantially to compensate for the temperature characteristic of said one FET stage over a range of battery voltage between normal battery voltage and said predetermined value.

2. A circuit as claimed in claim 1 wherein the FET stages are MOS. FET stages.

3. A circuit as claimed in claim 1 wherein the FET stages are junction type FET stages.

4. A circuit as claimed in any of the preceding claims wherein the compensating temperature characteristic is presented by the FET stage immediately following said one FET stage in the cascade series.

5. A circuit as claimed in claim 4 wherein there is employed in said one FET stage a P-channel FET having a drain current temperature coefficient which is negative over said range and an N-channel FET is employed in the immediately following stage.

6. A circuit as claimed in claim 4 wherein there is employed in said one FET stage an N-channel FET having a drain current temperature coefficient which is negative over said range and a P-channel FET is employed in the immediately following stage.

7. A circuit as claimed in claim 4 wherein there is employed in said one FET stage a P-channel FET having a drain current temperature coefficient which is positive over said range and a P-channel FET is employed in the immediately following stage.

8. A circuit as claimed in claim 4 wherein there is employed in said one FET stage an N-channel FET having a drain current temperature coefficient which is positive over said range and an N-channel FET is employed in the immediately following stage.

9. A circuit as claimed in any of claims 5 to 8 wherein said immediately following stage

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comprises a single FET with a load resistor.

10. A circuit as claimed in claim 9 wherein said load resistor is constituted by an MOS resistance presented by a MOS transistor.

5 11. A circuit as claimed in any of claims 1 to 4 wherein the compensating temperature characteristic is presented by a complementary MOS inverter stage.

12. Battery voltage detecting circuits as claimed in any of the preceding claims and substantially as herein set forth.

10 13. Battery voltage detecting circuits substantially as illustrated in Figure 4 or Figure 6 of the accompanying drawing.

14. A battery powered electronic timepiece having a battery voltage detecting circuit as claimed in any of the preceding claims and an indicator actuated thereby.

15 15. A calculator having a battery voltage detecting circuit as claimed in any of the preceding claims and an indicator actuated thereby.

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