

PATENT SPECIFICATION (11)

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- (21) Application No. 41671/72 (22) Filed 7 Sep. 1972
(23) Complete Specification filed 6 Sep. 1973
(44) Complete Specification published 10 Dec. 1975
(51) INT. CL.² H04N 9/00
(52) Index at acceptance H4F D1B3 D1D1 D1K1 D26G D30Q
D70G1
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(54) WAVEFORM GENERATOR

(71) We, GRANADA T.V. RENTAL LIMITED, a British Company, of P.O. Box 31, Ampthill Road, Bedford, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:-

This invention relates to waveform generators and more particularly to such generators for generating a waveform which, when applied to a colour television receiver, will produce on the screen thereof a colour bar pattern comprising vertical strips. Normally, the generator produces eight vertical strips which are, in order, white, yellow, cyan, green, magenta, red, blue and black.

The invention provides a colour bar generator comprising an oscillator for generating oscillations at a frequency corresponding to a colour sub-carrier frequency, a first chain of frequency dividers connected to said oscillator to produce an oscillation at line frequency, a second chain of frequency dividers connected to the line frequency output of said first chain of frequency dividers to produce an oscillation at field frequency, a third chain of frequency dividers connected to an intermediate point in said first chain and arranged to provide an oscillation at a multiple of line frequency, said multiple being related to the number of vertical bars the generator is to produce, a plurality of logic circuits connected to said chains of dividers and arranged to receive said line frequency oscillation, said field frequency oscillation and oscillations from appropriate points in said chains to provide line synchronising, line blanking, field synchronising, field blanking, colour burst gating signals, and P.A.L. line switching signals, a fourth chain of frequency dividers comprising three binary stages connected to the output of said third chain of frequency

dividers, means for applying blanking signals to said fourth chain to inhibit counting thereby during blanking periods, said three binary stages thereby providing respectively, signals corresponding to the red, green and blue signals required to form the successive colour bars, and a matrix circuit arranged to derive from said red, green and blue signals, luminance signals, red colour difference signals and blue colour difference signals.

Preferred features and advantages of the invention will become apparent from the following description of an embodiment thereof, given by way of example, when taken in conjunction with the accompanying drawings, in which:-

Figure 1, divided into Figures 1A, 1B and 1C, is a block diagram of the waveform generator;

Figure 2 is a circuit diagram showing the power supplies for the generator;

Figure 3, divided into Figures 3A and 3B, illustrates waveforms present at the various points in the circuit shown in Figure 1 which are identified in Figure 1 by letters corresponding to those in Figure 3; and

Figure 4 is the circuit diagram of one of the integrated circuits used in the apparatus shown in Figure 1.

Referring to Figure 1A, a crystal 1 is associated with an integrated circuit amplifier 3 and a feedback network 2 generates oscillations at 4.43361875 MHz, the colour sub-carrier frequency. The integrated circuit amplifier 3, as are all the integrated circuit amplifiers in the apparatus, is of a type SN5404 or SN7404. The sub-carrier frequency oscillations are shown at A in Figure 3A. The oscillations are applied through a cascade of two integrated circuit amplifiers, 4 and 5, to the input terminal of a four-bit binary counter 7. The four-bit binary counter, as are all the four-bit binary counters in the apparatus, is of type SN7493.

The output of the first binary counter is shown as waveform B, the output of the second binary counter is shown as waveform B, the output of the second binary counter is shown at C, the output of the third binary counter is shown at D, and the output of the fourth binary counter is shown at E. The output of counter 7 is applied to a second four-bit binary counter 8, and the output of the respective binary counters are shown at F, G, H and I. The output of the counter 8 is applied to one-half of a dual J-K master slave flip-flop 9. The J-K flip-flop, as are all the J-K flip-flops in the apparatus, is of type SN7475. The Q output of this flip-flop is shown as waveform J.

A four-input NAND-gate 14, of type SN7420, has as its inputs waveforms D, E, F and J. It will be appreciated that gate 14 will be energised only when the count of the sub-carrier frequency oscillations A has reached 284, that is to say, after one line period. The output K of gate 14 is applied through an amplifier 6 to reset counter 7 and 8, and to J-K flip-flop 9 to reset the flip-flop. This enables the count to resume, the counter chain 7, 8 and 9 thus never being allowed to reach the full count of 512 of which it would otherwise be capable. The reset pulses K set the start of the line scan period.

Waveforms G and H from counter 8 are applied to a two-input NAND-gate 19, type SN7400. A signal will be present at the output of gate 19 21. 65886 us and 50.53734 us after the start of the count. The output of gate 19 is applied to the clock pulse input of a J-K flip-flop 28. The waveform I is applied as the J input to the flip-flop and the effect of this is to render the flip-flop insensitive to the first of the input signals from gate 19 and it accordingly provides an output 50.53734 us after the start of the scan which defines the beginning of the blanking period. The flip-flop 28 is cleared by the application of waveform K thereto so that the output of flip-flop 28 is a pulse commencing 50.53734 us after the start of the scan and terminating at the start of the next scan. The resultant blanking pulse is shown as waveform L.

The synchronising pulse M is produced in a similar manner from gate 19, utilising a J-K flip-flop 27. However, the pulses from gate 19 are delayed with respect to the pulses applied to flip-flop 28 by a delay circuit 47 comprising series resistance and shunt capacitance. The result of this is that the pulse generated by flip-flop 27 commences after the line blanking pulse L. The delay sets the length of the front porch. However, the termination of the line synchronising pulse is not intended to coincide, as in the case of the blanking pulse, with the start of the next line period, and the termination is set by means which will be described below, so as to

provide a 4.7 us line synchronising pulse.

The line blanking pulses L are applied to the J-K flip-flop forming the other half of integrated circuit 9 to provide half line-frequency pulses V, constituting the P.A.L. switching signals, at its output. The waveform V is applied to the chain of two four-bit binary counters 10 and 11. The output of the third binary counter and the output of the fourth binary counter of counter 10 are connected to serve as the two inputs of the AND-gate which resets counter 10. This causes counter 10 to divide by 12. The output of the divider 10 is shown at Z and the waveforms at the output of the first divider, the second divider and the third divider are shown at W, X and Y respectively. The waveform Z is applied to the second counter 11. The output of the first binary counter is connected as one of the inputs of the AND-gate included in the SN7493 device for resetting the counter. The output of the third counter and the output of the fourth counter are connected to a NAND-gate 22, the output of which is connected to both inputs of a NAND-gate 23, the output of which forms the other input of the resetting AND-gate. The effect of these feedback connections is to cause counter 11 to divide by 13. The waveforms at the output of the first, second, third and fourth counters are shown at A', B', C' and D', and the output of NAND-gate 23 at E'.

Field synchronising pulses are generated by the J-K flip-flop 31, the output pulses from NAND-gate 22, at 50 Hz, being applied thereto to serve as clock pulses. The waveform W is applied to both inputs of a NOR-gate 20, serving as an inverter, to clear the flip-flop 31, thereby defining the termination of the field synchronisation pulse two line periods after the clock pulse. The line synchronisation pulses from flip-flop 27 are combined with the field synchronisation pulses from flip-flop 31 by the diodes 32 and 33.

The half sub-carrier frequency pulses B from counter 7 are applied as clock pulses to a four-bit binary counter 12. The outputs of the second, third and fourth counters therein are applied to a four-input NAND-gate 15, the output of which serves as an input of two input NAND-gate 13. Because of the polarity inversion of the pulses, the NAND-gate 13 serves as an OR-gate and its output R is used to reset counter 12.

The other input of gate 13 is the line reset pulses K. The waveforms at the output of the second, third and fourth counters of counter 12 are shown at O, P and Q. The feedback connections of counter 12 serve to cause it to divide by 14, thus the output waveform Q has a frequency equal to the sub-carrier frequency divided by 28. The output of gate 15 is used as the clearing input of flip-flop 27

thereby setting the width of the line synchronisation pulse.

The colour burst timing pulse is generated by the J-K flip-flop 26. The clock pulses are provided by the Q output of the flip-flop in integrated circuit 9 and accordingly is the inverse of waveform J. The waveform Q from counter 12 is applied through an amplifier 16 to clear flip-flop 26. The waveform Z from counter 10 and the output of NAND-gate 22 are applied as the inputs of a NOR-gate 24, SN7402, the output of which serves as both inputs of a second NOR-gate 25. The output of gate 25 serves as the J input of flip-flop 26. The output of flip-flop 26 is shown at N and its inverse is also available.

To provide various forms of patterns, by suitable switching in the apparatus, terminals are provided from which suitable waveforms can be obtained. Thus the output E of counter 7 at 1/16 sub-carrier frequency can be switched to serve as the clock pulse input of a vertical bar generator 30, a J-K flip-flop. This is to provide the vertical lines of the cross hatch. Alternatively, the clock pulse input can be selected to be a pulse appearing at the centre of each line. This is obtained from a NAND-gate 17 having as one input the waveform F from counter 8 and as the other input the inverted output of gate 19. The inversion is produced by a NAND-gate 18, the output of gate 19 being connected to both inputs thereof. In addition, horizontal bars can be produced from the J-K flip-flop 29. The clock input of flip-flop 29 is either the waveform Z, to produce the horizontal lines of the cross-hatch or the output of NAND-gate 21 which has as its inputs the waveforms B' and C, from counter 11 to produce a single horizontal line. If only vertical bars are required, mixed blanking pulses are applied to the J input of vertical bar generator 30, but if a dot pattern is required, then the output of the horizontal bar generator 29 is applied to the J input of vertical bar generator 30.

The output of counter 12, at 1/28 colour sub-carrier frequency is applied as clock pulses to each of three J-K flip-flops 36, 37 and 38. It will be appreciated that these clock pulses are at 10 times line frequency and are used to generate the vertical bands of the colour bar pattern. The Q output of the flip-flop 36 is applied to the J₁ and the K₁ inputs of both flip-flops 37 and 38. The Q output of flip-flop 37 is applied to the J₂ and K₂ inputs of flip-flop 38. The three flip-flops are all cleared by the line start pulses K from NAND-gate 14 and all are preset by blanking pulses from gate 34. It will be appreciated that the effect of the blanking pulses is to render the three flip-flops inoperative during blanking periods and accordingly the lumi-

nance and colour difference signals, which it is their purpose to generate, are already blanked before mixing into the complete waveform. The Q outputs of the three flip-flops are shown at S, T and U.

The luminance signal provided at terminal 39 is obtained by mixing the Q outputs of the flip-flop 36, 37 and 38 in suitable proportions. The R-Y difference signal at terminal 40 is obtained by matrixing the Q outputs of flip-flops 36 and 38 and the Q output of flip-flop 37 in suitable proportions. The B-Y difference signal at terminal 41 is obtained by matrixing the Q output signals of flip-flops 37 and 38 and the Q output of 36 in suitable proportions.

The integrated circuit 43 is in the apparatus described, of type Mullard TBA520 and is one which is intended for use in television receivers for the decoding of colour signals. Other such integrated circuits are available and have the characteristic that when the chrominance signals U and V are applied to two respective terminals and reference carrier frequency signals are applied in quadrature to another two respective terminals, there can be obtained outputs corresponding to R-Y, B-Y and G-Y at these respective terminals. Such integrated circuits are referred to in the claims as chrominance demodulation chips. The circuit of the Mullard integrated circuit TBA520 is shown in Figure 4. However, it can be equally well used, as in the present case, for modulating the colour difference signals onto the sub-carrier frequency. Accordingly, the waveform N from the burst timing pulse generator 26 and the B-Y difference signal are applied to terminals 9 thereof, the inverse of waveform N from generator 26 is applied together with the R-Y difference signal to terminal 13 thereof, and the oscillations from crystal 1, respectively advanced in phase and retarded in phase to provide a 90° phase difference are applied to the terminals 2 and 8 thereof. The waveform V at half line frequency is applied in opposite phases to terminals 14 and 15 of the integrated circuit.

The output of this circuit at terminal 5 is applied as one input to the base of the transistor 44, the luminance signal from terminal 39 being also applied at terminal 48 to said base. The mixed synchronising pulses from the diodes 32 and 33 are applied to the emitter of said transistor and accordingly, a mixed video-waveform appears at the collector of said transistor 44. A RF oscillator 45 of conventional type generates the main television carrier oscillation which is modulated by the circuit 46 comprising a field-effect transistor to the control electrode of which is connected the mixed waveform from transistor 44. The complete RF signal appears at terminal 49.

Figure 2 shows the power supply circuit for the apparatus. It comprises a transformer 70 supplied from the mains, the primary being provided with a fuse and a neon indicator. The secondary is connected to a bridge rectifier assembly 71 which provides one output at terminal 75 which is stabilised merely by the Zener diode 77. Another output is obtained at terminal 76, and this is stabilised with the load, having a reference potential applied to the control electrode thereof, derived from the Zener diode 72.

WHAT WE CLAIM IS:-

1. A colour bar generator comprising an oscillator for generating oscillations at a frequency corresponding to a colour sub-carrier frequency, a first chain of frequency dividers connected to said oscillator to produce an oscillation at line frequency, a second chain of frequency dividers connected to the line frequency output of said first chain of frequency dividers to produce an oscillation at field frequency, a third chain of frequency dividers connected to an intermediate point in said first chain and arranged to provide an oscillation at a multiple of line frequency, said multiple being related to the number of vertical bars the generator is to produce, a plurality of logic circuits connected to said chains of dividers and arranged to receive said line frequency oscillation, said field frequency oscillation and oscillations from appropriate points in said chains to provide line synchronising, line blanking, field synchronising, field blanking, colour burst gating signals, and P.A.L. line switching signals, a fourth chain of frequency dividers comprising three binary stages connected to the output of said third chain of frequency dividers, means for applying blanking signals to said fourth chain to inhibit counting thereby during blanking periods, said three binary stages thereby providing

respectively, signals corresponding to the red, green and blue signals required to form the successive colour bars, and a matrix circuit arranged to derive from said red, green and blue signals, luminance signals, red colour difference signals and blue colour difference signals.

2. A colour bar generator in accordance with claim 1, including a chrominance demodulation chip as herein defined, the red colour difference signal and blue colour difference signals being applied to the V and U inputs of said chip respectively, the colour burst gating signal being applied in respective opposite phases also to the V and U inputs, the colour sub-carrier frequency oscillation being applied in quadrature to the respective reference oscillation terminals of said chip, and the P.A.L. line switching signals being applied to their intended terminals of said chip, whereby there is produced by said chip the chrominance signal.

3. A colour bar generator in accordance with claim 2 including a radio frequency oscillator, an amplitude modulator therefor, said chrominance signal, said luminance signal and line and field synchronising signals being applied to said modulator.

4. A colour bar generator in accordance with any of the preceding claims including further logic circuits connected to appropriate points in said divider chains to provide signals for producing predetermined patterns on the screen of a receiver to which the generator is connected.

5. A colour bar generator substantially as herein described with reference to the accompanying drawings.

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