CLAIMS

What is claimed is:

1. A semiconductor structure comprising:

at least one FET gate stack 18 located on an upper surface of a semiconductor substrate 12, the at least one FET gate stack including a source extension region 28 and a drain extension region 28 located within the semiconductor substrate at a footprint of the at least one FET gate stack, and a device channel 40 located between the source extension region and the drain extension region and beneath the at least one gate stack;

embedded stressor elements 33 located on opposite sides of the at least one FET gate stack and within the semiconductor substrate, wherein each embedded stressor element includes, from bottom to top, a first layer of a first epitaxy doped semiconductor material 35 having a lattice constant that is different from a lattice constant of the semiconductor substrate and imparts a strain in the device channel, a second layer of a second epitaxy doped semiconductor material 36 located atop the first layer, wherein the first layer of the first epitaxy doped semiconductor material has a lower content of dopant as compared to the second layer of the second epitaxy doped semiconductor material, and a delta monolayer of dopant 37 located on the upper surface of the second layer of the second epitaxy dopant semiconductor material; and

a metal semiconductor alloy 45 located on an upper surface of the delta monolayer of dopant.

2. The semiconductor structure of Claim 1 wherein the semiconductor substrate 12 is made of bulk Si or silicon-on-insulator.

3. The semiconductor structure of Claim 1 wherein the at least one FET gate stack is a pFET gate stack 18', and wherein the first layer of each embedded stressor element 33' includes SiGe or SiGe:C.

4. The semiconductor structure of Claim 1 wherein the at least one FET gate stack is an nFET gate stack 18", and wherein the first layer of each embedded stressor element 33" includes Si:C.

5. The semiconductor structure of Claim 3 wherein the first and second epitaxy doped semiconductor materials include a p-type dopant and the delta monolayer of dopant is also p-type.

6. The semiconductor structure of Claim 4 wherein the first and second epitaxy doped semiconductor materials include an n-type dopant and the delta monolayer of dopant is also n-type.

7. The semiconductor structure of Claim 1 further comprising a silicide spacer 26 that is located adjacent the at least one FET gate stack 18 and atop a third layer of a third epitaxy doped semiconductor material 38.

8. A semiconductor structure comprising:

at least one pFET gate stack 18' and at least one nFET gate stack 18" located on an upper surface of a semiconductor substrate 12, each of the at least one pFET gate stack and the at least one nFET gate stack includes a source extension region 28 and a drain extension region 28 located within the semiconductor substrate at a footprint of both the at least one pFET gate stack and the at least one nFET gate stack, and a device channel 40 located between the source extension region and the drain extension region and beneath each of the gate stacks;

pFET embedded stressor elements 33' located on opposite sides of the at least one pFET gate stack 18' and within the semiconductor substrate, and nFET embedded stressor elements 33" located on opposite sides of the at least one nFET gate stack 18" and within the semiconductor substrate 12, wherein each of the embedded stressor elements includes, from bottom to top, a first layer of a first epitaxy doped semiconductor material 35', 35" having a lattice constant that is different from a lattice constant of the semiconductor substrate and imparts a strain in the device channel, a second layer of a second epitaxy doped semiconductor material 36', 36" located atop the first layer, wherein the first layer of the first epitaxy doped

semiconductor material has a lower content of dopant as compared to the second layer of the second epitaxy doped semiconductor material, and a monolayer of dopant 37', 37" located on an upper surface of the second layer of each of the embedded stressor elements; and

a metal semiconductor alloy 45 located on an upper surface of the delta monolayer of dopant 37.

9. The semiconductor structure of Claim 8 wherein the first layer of each of the pFET embedded stressor elements 33' includes SiGe or SiGe:C.

10. The semiconductor structure of Claim 8 wherein the first layer of each of the nFET embedded stressor 33" elements includes Si:C.

11. The semiconductor structure of Claim 9 wherein the first and second epitaxy doped semiconductor materials of the pFET stressor elements include a p-type dopant and the monolayer of dopant is also p-type.

12. The semiconductor structure of Claim 10 wherein the first and second epitaxy doped semiconductor materials of the nFET stressor elements include an n-type dopant and the monolayer of dopant is also n-type.

13. The semiconductor structure of Claim 9 further comprising a silicide spacer 26 that is located adjacent each of FET gate stacks and atop a third layer of a third epitaxy doped semiconductor material.

14. A method of fabricating a structure comprising:

forming at least one FET gate stack 18 on an upper surface of a semiconductor substrate;

forming a source extension region 28 and a drain extension region 28 within the semiconductor substrate 12 at the footprint of the at least one FET gate stack;

forming recessed regions on opposite sides of the at least one FET gate stack and within the semiconductor substrate;

forming pre-embedded stressor elements 33 substantially within the recessed regions, wherein each of the pre-embedded stressor elements includes, from bottom to top, a first layer of a first epitaxy doped semiconductor material 35 having a lattice constant that is different from a lattice constant of the semiconductor substrate and imparts a strain in the device channel, a second layer of a second epitaxy doped semiconductor material 36 located atop the first layer, wherein the first layer of the first epitaxy doped semiconductor material has a lower content of dopant as compared to the second layer of the second epitaxy doped semiconductor material, a delta monolayer of dopant 37 located on an upper surface of the second layer, and a third layer of epitaxy doped semiconductor layer 38 located atop the delta monolayer; and

converting a portion of the third layer of the pre-embedded stressor element into a metal semiconductor alloy contact 45, wherein said metal semiconductor alloy contact is located directly an upper surface of the delta monolayer 37.

15. The method of Claim 14 wherein the first, second and third layers of each pre-embedded stressor element are formed by an *in-situ* doped epitaxial growth process.

16. The method of Claim 14 wherein the delta monolayer of dopant is formed by atomic layer deposition, the atomic layer deposition occurs by interrupting growth of the second layer of the second epitaxy doped semiconductor material.

17. The method of Claim 14 wherein said converting includes a silicidation process.

18. The method of Claim 14 wherein the at least one FET gate stack is a pFET gate stack, the first layer of each of the embedded stressor elements includes SiGe or SiGe:C, the first and second epitaxy doped semiconductor materials include a p-type dopant, and the delta monolayer of dopant includes a p-type dopant.

19. The method of Claim 14 wherein the at least one FET gate stack is an nFET gate stack, the first layer of each of the embedded stressor elements includes Si:C, the first and second epitaxy

doped semiconductor materials include an n-type dopant, and the delta monolayer of dopant includes an n-type dopant.

20. The method of Claim 14 further comprising forming a silicide spacer adjacent to said at least one gate stack, wherein a bottom surface of said silicide spacer is located atop a remaining portion of the third layer of the third epitaxy doped semiconductor material, said silicide spacer is formed prior to said converting.

CLAIMS

1. A semiconductor structure comprising:

at least one FET gate stack located on an upper surface of a semiconductor substrate, the at least one FET gate stack including a source extension region and a drain extension region located within the semiconductor substrate at a footprint of the at least one FET gate stack, and a device channel located between the source extension region and the drain extension region and beneath the at least one gate stack;

embedded stressor elements located on opposite sides of the at least one FET gate stack and within the semiconductor substrate, wherein each embedded stressor element includes, from bottom to top, a first layer of a first epitaxy doped semiconductor material having a lattice constant that is different from a lattice constant of the semiconductor substrate and imparts a strain in the device channel, a second layer of a second epitaxy doped semiconductor material located atop the first layer, wherein the first layer of the first epitaxy doped semiconductor material has a lower content of dopant as compared to the second layer of the second epitaxy doped semiconductor material, and a delta monolayer of dopant located on the upper surface of the second layer of the second epitaxy dopant semiconductor material; and

a metal semiconductor alloy located on an upper surface of the delta monolayer of dopant.

2. The semiconductor structure of claim 1 wherein the semiconductor substrate is bulk Si or a silicon-on-insulator.

3. The semiconductor structure of claim 1 wherein the at least one FET gate stack is a pFET gate stack, and wherein the first layer of each embedded stressor element includes SiGe or SiGe:C.

4. The semiconductor structure of claim 1 wherein the at least one FET gate stack is an nFET gate stack, and wherein the first layer of each embedded stressor element includes Si:C.

5. The semiconductor structure of claim 3 wherein the first and second epitaxy doped semiconductor materials include a p-type dopant and the delta monolayer of dopant is also p-type.

6. The semiconductor structure of claim 4 wherein the first and second epitaxy doped semiconductor materials include an n-type dopant and the delta monolayer of dopant is also n-type.

7. The semiconductor structure of claim 1 further comprising a silicide spacer that is located adjacent the at least one FET gate stack and atop a third layer of a third epitaxy doped semiconductor material.

8. A semiconductor structure comprising:

at least one pFET gate stack and at least one nFET gate stack located on an upper surface of a semiconductor substrate, each of the at least one pFET gate stack and the at least one nFET gate stack includes a source extension region and a drain extension region located within the semiconductor substrate at a footprint of both the at least one pFET gate stack and the at least one nFET gate stack, and a device channel located between the source extension region and the drain extension region and beneath each of the gate stacks;

pFET embedded stressor elements located on opposite sides of the at least one pFET gate stack and within the semiconductor substrate, and nFET embedded stressor elements located on opposite sides of the at least one nFET gate stack and within the semiconductor substrate, wherein each of the embedded stressor elements includes, from bottom to top, a first layer of a first epitaxy doped semiconductor material having a lattice constant that is different from a lattice constant of the semiconductor substrate and imparts a strain in the device channel, a second layer of a second epitaxy doped semiconductor material located atop the first layer, wherein the first layer of the first epitaxy doped semiconductor material has a lower content of dopant as compared to the second layer of the second epitaxy doped semiconductor material, and a monolayer of dopant located on an upper surface of the second layer of each of the embedded stressor elements; and

a metal semiconductor alloy located on an upper surface of the delta monolayer of dopant.

9. The semiconductor structure of claim 8 wherein the first layer of each of the pFET embedded stressor elements includes SiGe or SiGe:C.

10. The semiconductor structure of claim 8 wherein the first layer of each of the nFET embedded stressor elements includes Si:C.

11. The semiconductor structure of claim 9 wherein the first and second epitaxy doped semiconductor materials of the pFET stressor elements include a p-type dopant and the monolayer of dopant is also p-type.

12. The semiconductor structure of claim 10 wherein the first and second epitaxy doped semiconductor materials of the nFET stressor elements include an n-type dopant and the monolayer of dopant is also n-type.

13. The semiconductor structure of claim 9 further comprising a silicide spacer that is located adjacent each of FET gate stacks and atop a third layer of a third epitaxy doped semiconductor material.

14. A method of fabricating a structure comprising:

forming at least one FET gate stack on an upper surface of a semiconductor substrate;

forming a source extension region and a drain extension region within the semiconductor substrate at the footprint of the at least one FET gate stack;

forming recessed regions on opposite sides of the at least one FET gate stack and within the semiconductor substrate;

forming pre-embedded stressor elements substantially within the recessed regions, wherein each of the pre-embedded stressor elements includes, from bottom to top, a first layer of a first epitaxy doped semiconductor material having a lattice constant that is different from a lattice constant of the semiconductor substrate and imparts a strain in the device channel, a second layer of a second epitaxy doped semiconductor material located atop the first layer, wherein the first layer of the first epitaxy doped semiconductor material has a lower content of dopant as compared to the second layer of the second epitaxy doped semiconductor material, a delta monolayer of dopant located on an upper surface of the second layer, and a third layer of epitaxy doped semiconductor layer located atop the delta monolayer; and

converting a portion of the third layer of the pre-embedded stressor element into a metal semiconductor alloy contact, wherein said metal semiconductor alloy contact is located directly an upper surface of the delta monolayer.

15. The method of claim 14 wherein the first, second and third layers of each pre-embedded stressor element are formed by an in-situ doped epitaxial growth process.

16. The method of claim 14 wherein the delta monolayer of dopant is formed by atomic layer deposition, the atomic layer deposition occurs by interrupting growth of the second layer of the second epitaxy doped semiconductor material.

17. The method of claim 14 wherein said converting includes a silicidation process.

18. The method of claim 14 wherein the at least one FET gate stack is a pFET gate stack, the first layer of each of the embedded stressor elements includes SiGe or SiGe:C, the first and second epitaxy doped semiconductor materials include a p-type dopant, and the delta monolayer of dopant includes a p-type dopant.

19. The method of claim 14 wherein the at least one FET gate stack is an nFET gate stack, the first layer of each of the embedded stressor elements includes Si:C, the first and second epitaxy doped semiconductor materials include an n-type dopant, and the delta monolayer of dopant includes an n-type dopant.

20. The method of claim 14 further comprising forming a silicide spacer adjacent to said at least one gate stack, wherein a bottom surface of said silicide spacer is located atop a remaining portion of the third layer of the third epitaxy doped semiconductor material, said silicide spacer is formed prior to said converting.