

**Motor controller for electronically commutated DC motors in
order to compensate for torque drops**

The invention relates to a motor controller having
5 electronic commutation which is connected to the windings
of a motor, a predetermined additional current being
connected to that coil of the motor which is active at that
moment, from the commutation instant, in order to prevent
torque drops.

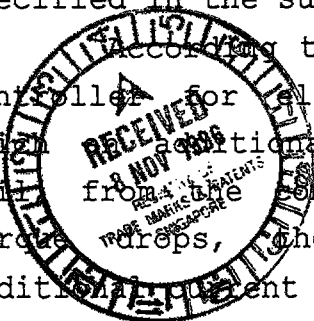
10 US-4,511,827 discloses a controller which drives an
electronically commutated motor such that torque
fluctuations are suppressed. This device in this case
comprises a sensor for determining the rotor position, in
other words the commutation instant, and a controller which
15 processes this signal so that the corresponding coil is
supplied, from the commutation instant, with additional
current in order to prevent a torque drop.

However, it has been found in the case of the known
solution that the supply of a predetermined current to the
20 coil compensates for the torque drops only within a
specific motor current range. However, for example, in a
video recorder, the known method does not provide
satisfactory results since, in an operating mode (for
example play or long-play), the currents may be very
25 different because of different mechanical loads, for
example in the case of different temperatures or cassettes.

The invention is thus based on the object of
providing a motor controller in which torque drops are
avoided even in the event of different motor loads.

30 The object is achieved by the features of
Claim 1. Preferred refinements of the invention are
specified in the subclaims.

According to the invention, in the case of a motor
controller for electronically commutated DC motors, in
35 which an additional current is connected to the active
coil from the commutation instant, in order to prevent
torque drops, the duration and/or amplitude of the
additional current pulse are/is determined as a function of
the motor load. In other words, the duration and/or



amplitude of the additional current pulse are/is variable and are/is derived from the load on the motor, the additional current pulse being longer (greater) the higher the motor load, as is self-evident.

5 This advantageously results in torque drops being compensated for automatically and optimally, irrespective of the production scatter between motors, the temperature ranges and ageing.

10 The motor controller according to the invention normally controls the motor by means of so-called pulse-width modulation (CPWM or PWM) of the control pulses. The PWM signal of the motor controller is held at "1" for the duration of the additional current. The commutation instant, from which the additional current is applied, can
15 be determined by a sensor.

 The motor load is determined from the motor current drawn, it being possible to determine the motor current, for example, by means of a measurement resistor which is connected in the motor circuit or from the ratio of the
20 pulse duration to the pulse pause of the PWM signal.

 Furthermore, the controller according to the invention may have an integrator which produces a control signal (S) from the duty ratio of the CPWM signal. The start of the integration of the CPWM control signals is
25 likewise brought about by the occurrence of the commutation signal.

 The controller advantageously has a flipflop whose Q output is connected to the CPWM control signals via an "OR" gate, so that the Q output is switched to logic "1" on
30 the occurrence of the commutation signal, the Q output of the flipflop being reset again when the control signal corresponds with a reference voltage. The comparison between the reference voltage and the control signal is preferably carried out by means of a differential
35 amplifier. This also brings about the end of the integration of the CPWM signals.

 A preferred embodiment of the invention will be explained in the following text with reference to the figures, in which:



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Fig. 1 shows a circuit diagram of the compensation section, according to the invention, of the motor controller,

5 Figs. 2a and 2b show timing diagrams of the input and output signals required for control purposes, and

Figures 3a and 3b show the current waveform in an electronically commutated motor, respectively without and with compensation.

Fig. 1 shows the logic circuit for compensating for
10 torque drops in digitally driven, electronically commutated motors. A digital motor control signal CPWM, in which the motor load can be derived from the duty ratio, is passed to the input of the compensation circuit 1. A control signal S is derived from this signal CPWM by means of an integrator
15 2. The integrator 2 preferably comprises three serial resistors R_1 , R_2 and R_3 , as well as two capacitors C_1 and C_2 , C_1 being arranged electrically between earth (reference-earth potential) and the junction of R_1 and R_2 , and C_2 being arranged electrically between earth and the junction of R_2
20 and R_3 , and the control signal S being formed on C_2 . The control signal CPWM for controlling the motor, which is not illustrated, is furthermore passed to an input of an OR gate 3, so that a PWM control signal appears at the output of the OR gate 3 and is supplied to PWM power stages, which
25 are likewise not illustrated, in order to provide the motor current in the individual motor coils or windings.

The control signal S which is produced by the integrator 2 is supplied to the inverting input of a differential amplifier which is designed as a comparator 4
30 and to whose non-inverting input a reference voltage U_{REF} is applied, which is defined via a voltage divider composed of resistors R_4 , R_5 . The output of the comparator 4 is passed to the reset input of a flipflop 5, which is formed by a D flipflop. The D input of the flipflop 5 is at positive
35 potential which can be derived, for example, from an operating voltage U_b . The occurrence of the commutation signal I for the motor drive activates the flipflop 5 via the clock input, so that a logic "1" appears at the Q output. The Q output of the flipflop 5 is passed to the



other input of the OR gate 3. As a result of the CPWM signal being linked to the Q output by means of this OR circuit, the PWM signal for the power stages is in consequence held at logic "1" or at the "High" level, so
5 that an additional current is supplied to the motor windings. The Q output of the flipflop 5 remains at logic "1" until logic "1" appears at the output of the comparator 4, so that the flipflop is reset via the reset input R of the flipflop 5 and, in consequence, a logic "0" appears at
10 the Q output or the Q output is held at the "low" level. An npn transistor T is connected between the inverting input of the comparator 4 (control signal S) and the Q output of the flipflop 5, such that the base is connected to the Q output via a resistor R_6 . The emitter of the transistor T,
15 which is at the positive potential of the operating voltage U_b , is connected to the base via a resistor R_7 , while the collector of transistor T is connected to the inverting input of the comparator 4. When the Q output of the flipflop 5 switches up to logic "1", the transistor T is
20 switched off, while a logic "0" at the Q output of the flipflop 5 opens the transistor T, or switches it on.

The transistor T thus acts as an electronic switch by means of which the capacitor C_2 on which the control signal S is formed can be charged to the positive potential
25 of the operating voltage U_b , depending on the logic signal state at the Q output of the flipflop 5, or, when the Q output is switched to logic "0" or the "low" level, can be discharged to the potential which results on the capacitor C_1 as a result of the continuous integration of the CPWM
30 signals which are continuously supplied via the resistor R_1 . The discharge time constant of the capacitor C_2 is in this case essentially determined by the parallel circuit formed by the resistor R_3 and the resistor R_2 , the latter of which forms a series circuit with the capacitor C_1 for
35 discharging. The charging time constant of the capacitor C_2 is determined by the resistance of the switched-on emitter-collector path through the transistor T.

Figures 2a and 2b show the waveform of the various control signals with respect to time, Fig. 2a illustrating



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the case when the motor load is low, and Fig. 2b illustrating the case when the motor load is high. The upper clock waveform in Fig. 2a shows the motor control signal CPWM, the duty ratio being relatively low. When the
5 commutation signal I occurs, the Q output of the flipflop 5 is switched to the "High" level, so that the transistor T is switched off and defines the start of production of the control signal S. This means that the voltage on the capacitor C_2 , which corresponds to the control signal S, in
10 consequence falls until the flipflop 5 is reset via the R input. This results in the lower clock waveform at the output of the OR gate 3, that is to say the output of the OR gate 3 is logic "1" for the duration of the current control signal S, which means a positive potential with
15 respect to the reference-earth potential in the present case, while logic "0" is, for example, the reference-earth potential.

Fig. 2b shows the same situation as Fig. 2a, but with the motor control signal CPWM having a higher duty ratio. As a result of the higher duty ratio of the motor
20 control signal CPWM, the capacitor C_1 is charged to a higher voltage in comparison with the situation according to Fig. 2a. The consequence of this is that the capacitor C_2 is discharged more slowly and the waveform of the current
25 control signal S also lasts for a longer time, so that the time period for which the output of the OR gate 3 remains at logic "1" is significantly longer.

Fig. 3a shows the current waveform in one of the motor windings without the compensation according to the
30 invention for torque drops. The upper part illustrates the instants of commutation. The lower part shows the current waveform as a function of time. It can clearly be seen that drops occur in the current waveform and thus also in the torque waveform of a motor at the commutation instants.

35 In contrast to this, Fig. 3b shows the current waveform in one of the motor windings where current and/or voltage compensation are/is used in order to avoid torque drops. The current waveform, and thus the torque waveform



of the motor, is approximately constant at the commutation instants.

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Patent Claims



* C L M S *

1. Motor controller for electronically commutated DC
5 motors, in which an additional current and/or voltage is
connected to the active motor winding from the commutation
instant in order to prevent torque drops, **characterized in**
that the duration and/or amplitude of the additional
current and/or voltage pulse is derived from the motor
10 load.
2. Motor controller according to Claim 1,
characterized in that the motor is driven by pulse-width
modulation (PWM).
3. Motor controller according to Claim 2,
15 **characterized in that** the PWM signal is held at logic "1"
for the duration of the additional current and/or voltage.
4. Motor controller according to one of the preceding
claims, **characterized in that** the commutation instant is
determined by a sensor.
- 20 5. Motor controller according to one of the preceding
claims, **characterized in that** the motor load is determined
from the motor current drawn.
6. Motor controller according to Claim 5,
characterized in that the motor current is determined by a
25 measurement resistor in the motor circuit.
7. Motor controller according to Claim 4,
characterized in that the motor current is determined from
the ratio of the pulse duration to the pulse pause in the
PWM signal and/or from the motor rotation speed.
- 30 8. Motor controller according to Claim 7,
characterized in that the controller has an integrator (2)
which produces a control signal (S) from the duty ratio of
the PWM signal.
9. Motor controller according to Claim 8,
35 **characterized in that** the controller furthermore has a
flipflop (5) whose Q output together with the PWM control
signal form the inputs of an OR gate, so that the Q output
is switched to logic "1" on the arrival of the commutation
signal (I), and the Q output is reset again when the

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control signal (S) corresponds with a reference voltage (U_{REF}).

10. Motor controller according to Claim 9, characterized in that the comparison between the reference
5 voltage (U_{REF}) and the control signal (S) is carried out by means of a differential amplifier (4).



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